

NUP4114HMR6

Ultra Low Capacitance Diode-TVS Array for High Speed Data Line Protection

The NUP4114HMR6 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra-low capacitance and high level of ESD protection makes this device well suited for use in HDMI and DVI applications.

Features

- Low Capacitance (0.8 pF Typical Between I/O Lines)
- ESD Rating of Class 3B (Exceeding 8 kV) per Human Body model and Class C (Exceeding 400 V) per Machine Model
- Protection for the Following IEC Standards:
IEC 61000-4-2 13 kV (contact)
- UL Flammability Rating of 94 V-0
- This is a Pb-Free Device

Typical Applications

- High Speed Communication Line Protection
- Digital Video Interface (DVI) and HDMI
- Monitors and Flat Panel Displays
- Gigabit Ethernet
- Notebook Computers
- USB 2.0 High Speed Data Line and Power Line Protection

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	-40 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 Seconds)	T_L	260	$^\circ\text{C}$
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Contact (ESD)	ESD	16000 400 13000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



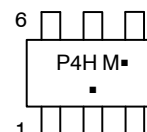
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM

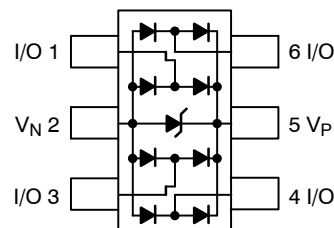


TSOP-6
CASE 318G
STYLE 12



P4H = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

Device	Package	Shipping
NUP4114HMR6T1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

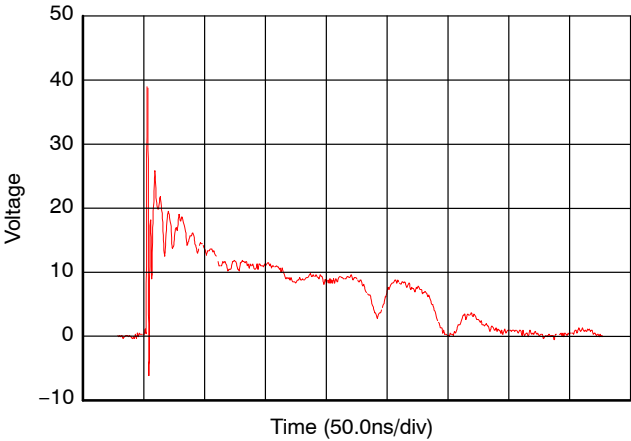
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NUP4114HMR6

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V _{RWM}	(Note 1)			5.0	V
Breakdown Voltage	V _{BR}	I _T = 1 mA, (Note 2)	6.0	7.5		V
Reverse Leakage Current	I _R	V _{RWM} = 5 V			1.0	μA
Clamping Voltage	V _C	I _{PP} = 5 A (Note 3)			9.0	V
Clamping Voltage	V _C	I _{PP} = 8 A (Note 3)			10	V
Maximum Peak Pulse Current	I _{PP}	8x20 μs Waveform			19	A
Junction Capacitance	C _J	V _R = 0 V, f = 1 MHz between I/O Pins and GND		0.8	1.0	pF
Junction Capacitance	C _J	V _R = 0 V, f = 1 MHz between I/O Pins			0.5	pF

1. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
2. V_{BR} is measured at pulse test current I_T.
3. Nonrepetitive current pulse (Pin 5 to Pin 2)



**Figure 1. ESD Clamping Voltage
(8 kV Contact per IEC61000-4-2)**

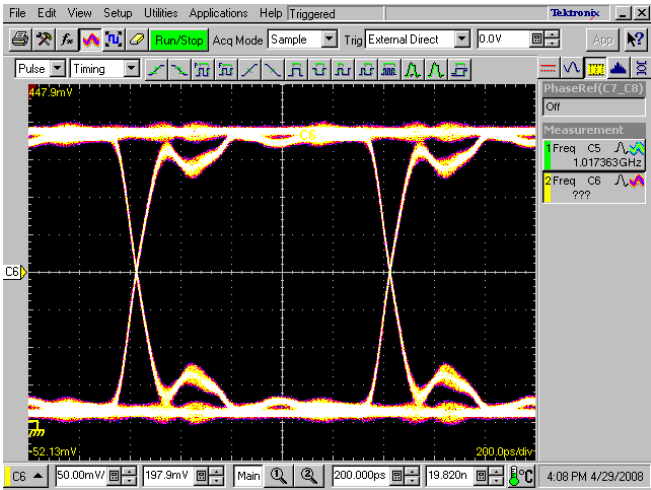


Figure 2. 500 MHz Data Pattern

APPLICATIONS INFORMATION

The new NUP4114HMR6 is a low capacitance TVS diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines. The integrated design of the NUP4114HMR6 offers low capacitance steering diodes and a TVS diode integrated in a single package (SC-74). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. The TVS device protects the power line against overvoltage conditions to avoid damage to the power supply and any downstream components.

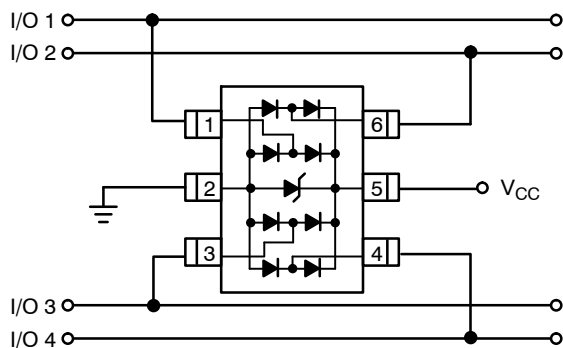
NUP4114HMR6 Configuration Options

The NUP4114HMR6 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (V_f or $V_{CC} + V_f$). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 2. This pin must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductances.

Option 1

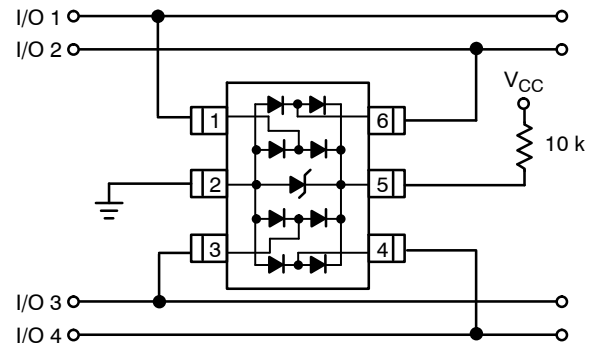
Protection of four data lines and the power supply using V_{CC} as reference.



For this configuration, connect pin 5 directly to the positive supply rail (V_{CC}), the data lines are referenced to the supply voltage. The internal TVS diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

Option 2

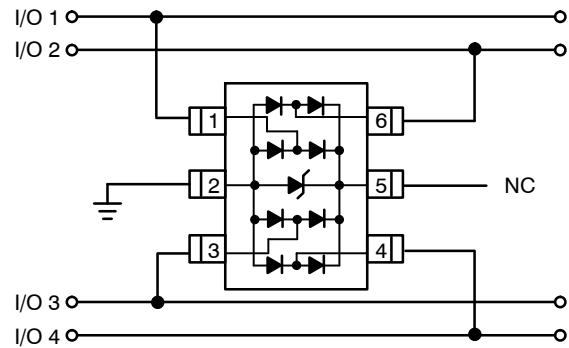
Protection of four data lines with bias and power supply isolation resistor.



The NUP4114HMR6 can be isolated from the power supply by connecting a series resistor between pin 5 and V_{CC} . A 10 kΩ resistor is recommended for this application. This will maintain a bias on the internal TVS and steering diodes, reducing their capacitance.

Option 3

Protection of four data lines using the internal TVS diode as reference.

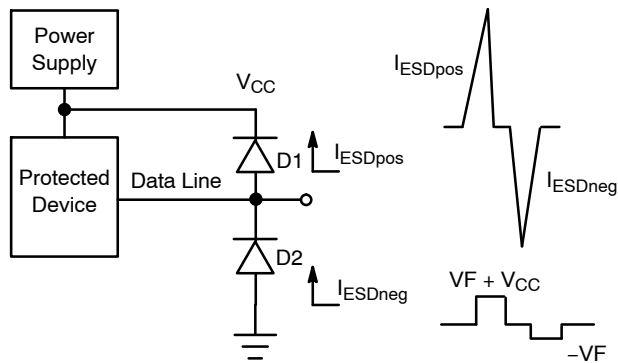


In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the internal TVS can be used as the reference. For these applications, pin 5 is not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the TVS plus one diode drop ($V_C = V_f + V_{TVS}$).

ESD Protection of Power Supply Lines

When using diodes for data line protection, referencing to a supply rail provides advantages. Biasing the diodes reduces their capacitance and minimizes signal distortion.

Implementing this topology with discrete devices does have disadvantages. This configuration is shown below:



Looking at the figure above, it can be seen that when a positive ESD condition occurs, diode D1 will be forward biased while diode D2 will be forward biased when a negative ESD condition occurs. For slower transient conditions, this system may be approximated as follows:

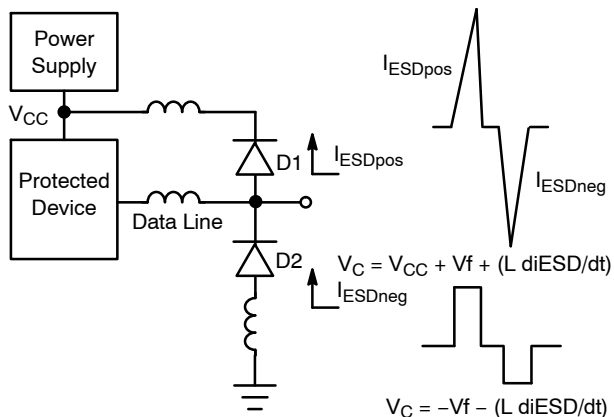
For positive pulse conditions:

$$V_c = V_{CC} + V_{fD1}$$

For negative pulse conditions:

$$V_c = -V_{fD2}$$

ESD events can have rise times on the order of some number of nanoseconds. Under these conditions, the effect of parasitic inductance must be considered. A pictorial representation of this is shown below.



An approximation of the clamping voltage for these fast transients would be:

For positive pulse conditions:

$$V_c = V_{CC} + V_f + (L \, di_{ESD}/dt)$$

For negative pulse conditions:

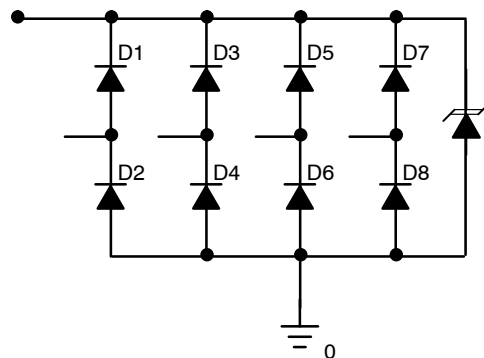
$$V_c = -V_f - (L \, di_{ESD}/dt)$$

As shown in the formulas, the clamping voltage (V_c) not only depends on the V_f of the steering diodes but also on the $L \, di_{ESD}/dt$ factor. A relatively small trace inductance can result in hundreds of volts appearing on the supply rail. This endangers both the power supply and anything attached to that rail. This highlights the importance of good board layout. Taking care to minimize the effects of parasitic

inductance will provide significant benefits in transient immunity.

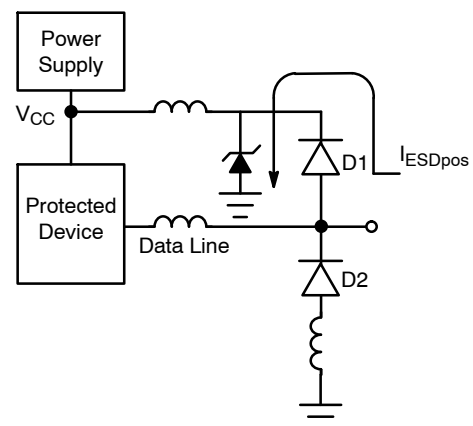
Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor NUP4114HMR6 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a TVS diode within a network of steering diodes.



NUP4114HMR6 Equivalent Circuit

During an ESD condition, the ESD current will be driven to ground through the TVS diode as shown below.



The resulting clamping voltage on the protected IC will be:

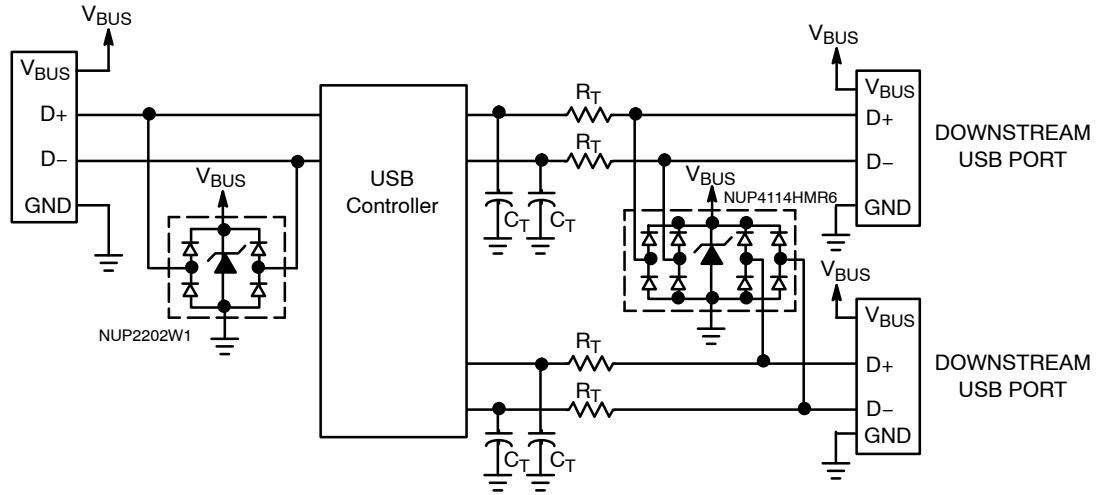
$$V_c = V_f + V_{TVS}$$

The clamping voltage of the TVS diode depends on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.

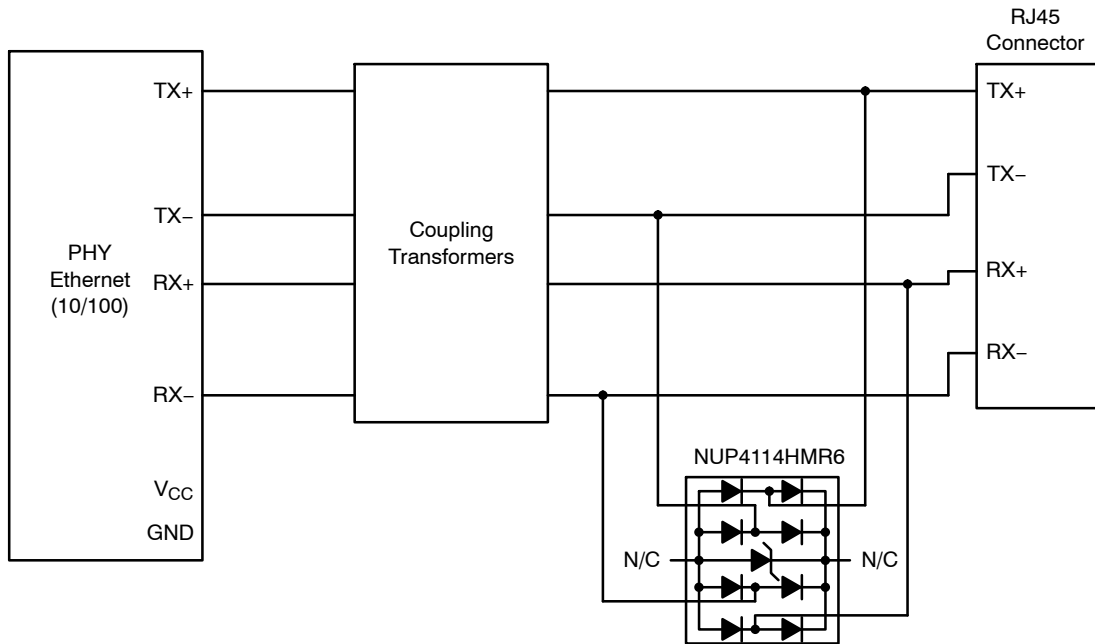
NUP4114HMR6

TYPICAL APPLICATIONS

UPSTREAM
USB PORT

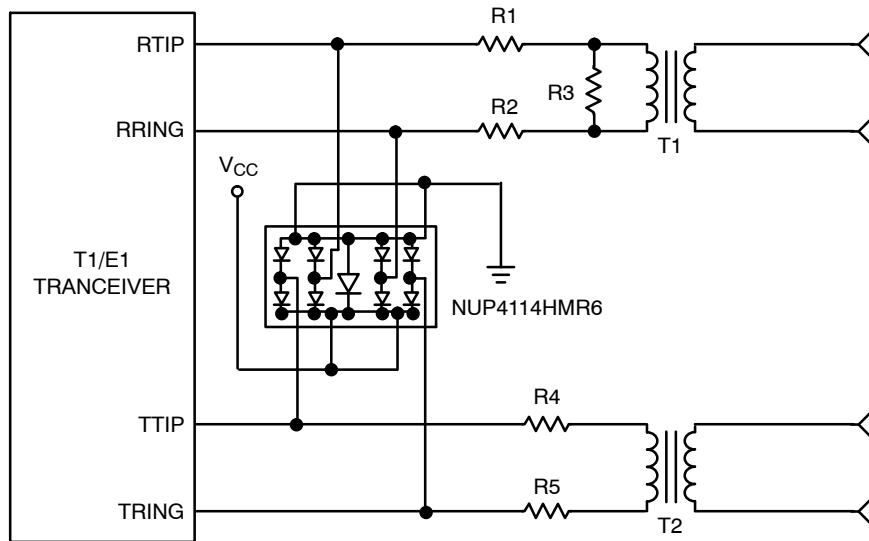


ESD Protection for USB Port



Protection for Ethernet (Differential mode)

NUP4114HMR6

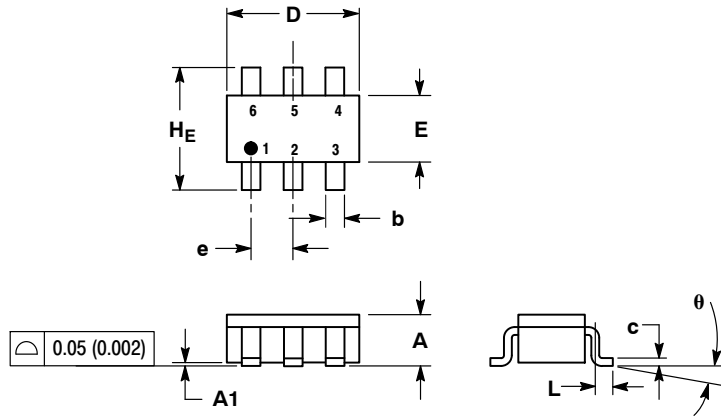


TI/E1 Interface Protection

NUP4114HMR6

PACKAGE DIMENSIONS

TSOP-6
CASE 318G-02
ISSUE T



NOTES:

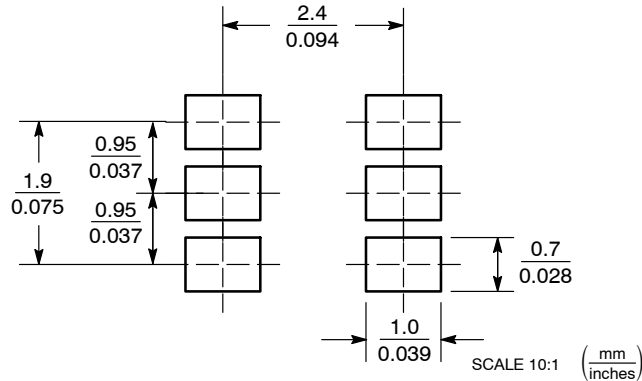
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	—	10°	0°	—	10°


STYLE 12:

- PIN 1: I/O
2: GROUND
3: I/O
4: I/O
5: VCC
6: I/O

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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