Power MOSFET 30 V, 35 A, Single N-Channel, DPAK/IPAK

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Low R_G
- These are Pb-Free Devices

Applications

- CPU Power Delivery
- DC-DC Converters
- High Side Switching

MAXIMUM RATINGS (T_J = 25° C unless otherwise stated)

Para	ameter		Symbol	Value	Unit
Drain-to-Source Vo	ltage		V _{DSS}	30	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain		$T_A = 25^{\circ}C$	۱ _D	8.5	А
Current R _{θJA} (Note 1)		T _A = 85°C		6.5	
Power Dissipation $R_{\theta JA}$ (Note 1)		T _A = 25°C	PD	1.92	W
Continuous Drain Current R _{0JA}		T _A = 25°C	ID	6.9	Α
(Note 2)	Steady State	T _A = 85°C		5.3	
Power Dissipation $R_{\theta JA}$ (Note 2)	Sidle	T _A = 25°C	P _D	1.26	W
Continuous Drain Current R _{0JC}		T _C = 25°C	Ι _D	35	A
(Note 1)		T _C = 85°C	1	27	
Power Dissipation $R_{\theta JC}$ (Note 1)		T _C = 25°C	PD	32.6	W
Pulsed Drain Current	t _p =10μs	T _A = 25°C	I _{DM}	87	A
Current Limited by P	ackage	T _A = 25°C	I _{DmaxPkg}	35	А
Operating Junction a Temperature	ind Storage		T _J , T _{STG}	-55 to +175	°C
Source Current (Boo	ly Diode)		۱ _S	27	А
Drain to Source dV/dt			dV/dt	6	V/ns
$ Single Pulse Drain-to-Source Avalanche \\ Energy (V_{DD} = 24 V, V_{GS} = 10 V, \\ I_L = 15.4 A_{pk}, L = 0.3 mH, R_G = 25 \Omega) $		EAS	35.6	mJ	
Lead Temperature for (1/8" from case for 1		Purposes	ΤL	260	°C

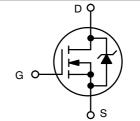
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



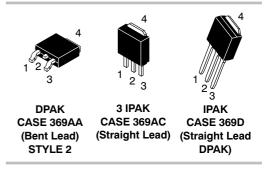
ON Semiconductor®

http://onsemi.com

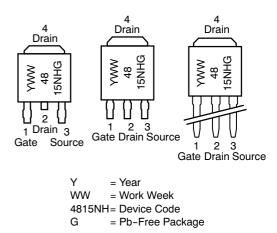
V _{(BR)DSS}	R _{DS(ON)} MAX	I _D MAX
30 V	$15~m\Omega @ 10~V$	05.4
30 V	27.7 mΩ @ 4.5 V	35 A



N-CHANNEL MOSFET







ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

Semiconductor Components Industries, LLC, 2008 January, 2008 – Rev. 2

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{ ext{ heta}JC}$	4.6	°C/W
Junction-to-TAB (Drain)	$R_{\thetaJC-TAB}$	3.5	
Junction-to-Ambient – Steady State (Note 1)	R_{\thetaJA}	78	
Junction-to-Ambient – Steady State (Note 2)	$R_{ hetaJA}$	119	

Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
 Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25° C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS						-	
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V_{GS} = 0 V, I _D =	= 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} / T _J				25		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V	T _J = 25 °C			1	
		v _{DS} = 24 v	T _J = 125°C			10	μΑ
Gate-to-Source Leakage Current	I _{GSS}	V_{DS} = 0 V, V_{GS}	= ±20 V			±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}, I_{D} = 250 \ \mu A$		1.5		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				5.6		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 V to$	I _D = 30 A		12	15	
		11.5 V	I _D = 15 A		11.5		
		V _{GS} = 4.5 V	I _D = 20 A		21.5	27.7	mΩ
			I _D = 15 A		20.1		
Forward Transconductance	g fs	V _{DS} = 15 V, I _D = 10 A			6.0		S
CHARGES AND CAPACITANCES	-						
Input Capacitance	C _{ISS}				845		
Output Capacitance	C _{OSS}	V _{GS} = 0 V, f = 1.0 MH	Hz, V _{DS} = 12 V		183		pF
Reverse Transfer Capacitance	C _{RSS}				103		1

Reverse Transfer Capacitance	CRSS		103		
Total Gate Charge	Q _{G(TOT)}		6.4	6.8	
Threshold Gate Charge	Q _{G(TH)}	\/ _ 4 5 \/ \/ _ 15 \/ \ _ 20 A	1.5		nC
Gate-to-Source Charge	Q _{GS}	V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 30 A	2.9		ne
Gate-to-Drain Charge	Q _{GD}		2.7		
Total Gate Charge	Q _{G(TOT)}	V_{GS} = 11.5 V, V_{DS} = 15 V; I _D = 30 A	15.2		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}		11.3	
Rise Time	t _r	V _{GS} = 4.5 V, V _{DS} = 15 V,	17.6	
Turn-Off Delay Time	t _{d(OFF)}	$I_{\rm D}$ = 15 A, $R_{\rm G}$ = 3.0 Ω	11	ns
Fall Time	t _f		2.8	

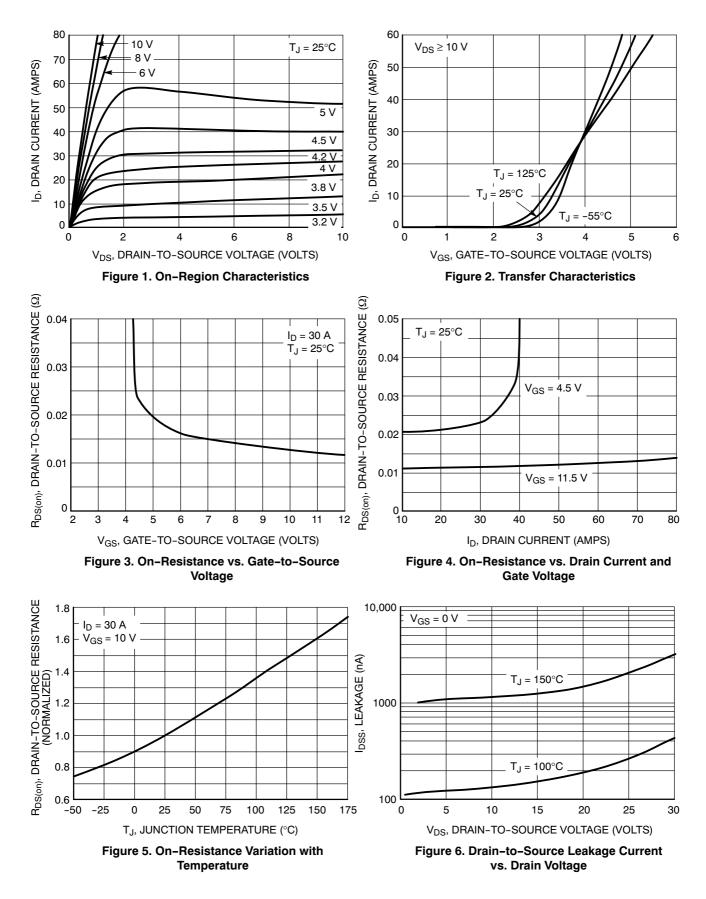
3. Pulse Test: pulse width \leq 300 µs, duty cycle \leq 2%.

4. Switching characteristics are independent of operating junction temperatures.

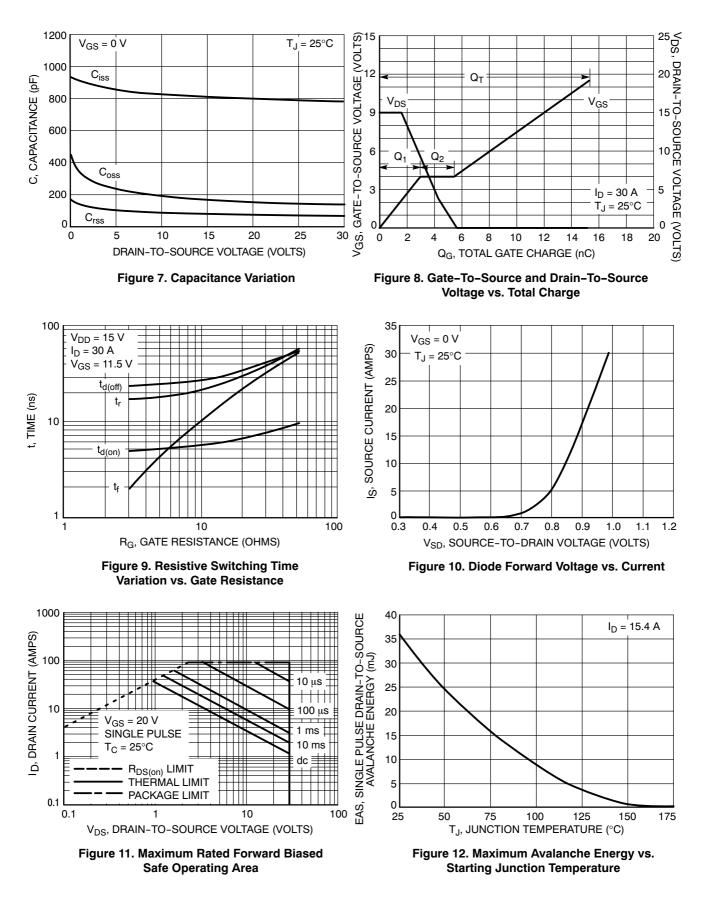
ELECTRICAL CHARACTERISTICS (T_J = 25° C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
SWITCHING CHARACTERISTICS (N	lote 4)						
Turn-On Delay Time	t _{d(ON)}				6.7		
Rise Time	t _r	V _{GS} = 11.5 V, V	ns = 15 V,	14.7	17.6		
Turn-Off Delay Time	t _{d(OFF)}	V _{GS} = 11.5 V, V I _D = 15 A, R _G	= 3.0 Ω	17.8	18.4		ns
Fall Time	t _f			1.8	2.3		
DRAIN-SOURCE DIODE CHARACT	ERISTICS			-			
Forward Diode Voltage	V _{SD}	$ \begin{array}{c} V_{GS} = 0 \ V, \\ I_{S} = 30 \ A \end{array} \qquad \begin{array}{c} T_{J} = 25^{\circ}C \\ T_{J} = 125^{\circ}C \end{array} $		0.98	1.2	N	
			T _J = 125°C		0.92		V
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dIS/dt = 100 A/µs, I _S = 30 A			18.1		
Charge Time	t _a				11.3		ns
Discharge Time	t _b	I _S = 30	A		6.8		
Reverse Recovery Charge	Q _{RR}				8.2		nC
PACKAGE PARASITIC VALUES		• •		-			
Source Inductance	L _S	T _A = 25°C			2.49		nH
Drain Inductance, DPAK	L _D				0.0164		
Drain Inductance, IPAK	L _D				1.88		
Gate Inductance	L _G				3.46		
Gate Resistance	R _G				0.6		Ω

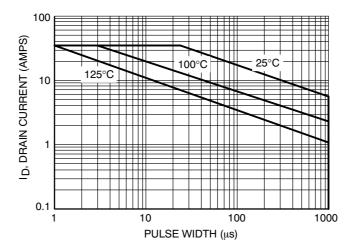
TYPICAL PERFORMANCE CURVES



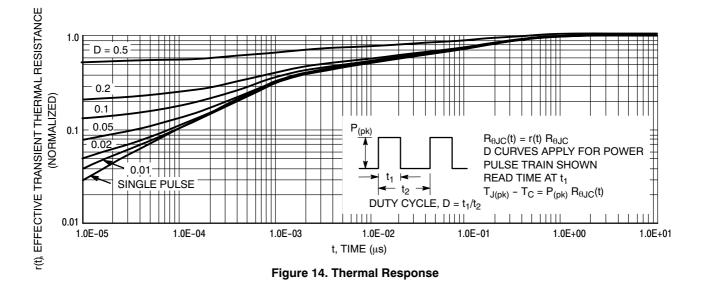
TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES







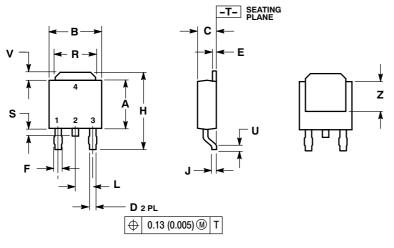
ORDERING INFORMATION

Device	Package	Shipping [†]
NTD4815NHT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD4815NH-1G	IPAK 75 Units / Rail (Pb-Free)	
NTD4815NH-35G	IPAK Trimmed Lead (3.5 ± 0.15 mm) (Pb-Free)	75 Units / Rail

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369AA-01 ISSUE A

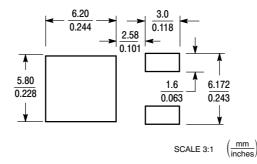


NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INC	HES	MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.22
в	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.89
Е	0.018	0.024	0.46	0.61
F	0.030	0.045	0.77	1.14
н	0.386	0.410	9.80	10.40
J	0.018	0.023	0.46	0.58
L	0.090	BSC	2.29 BSC	
R	0.180	0.215	4.57	5.45
s	0.024	0.040	0.60	1.01
U	0.020		0.51	
V	0.035	0.050	0.89	1.27
Z	0.155		3.93	

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

SOLDERING FOOTPRINT*

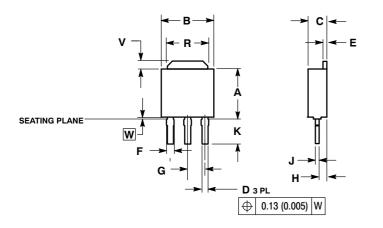


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

3 IPAK, STRAIGHT LEAD CASE 369AC-01

ISSUE O



DIMENSION A DOES NOT INCLUDE 4. DAMBAR POSITION OR MOLD GATE. INCHES MILLIMETERS DIM MIN MAX MIN MAX A 0.235 0.245 5.97 6.22 **B** 0.250 0.265 6.35 6.73 C 0.086 0.094 2.19 2.38 D 0.027 0.035 0.69 0.88 E 0.018 0.023 0.46 0.58 0.94 1.09 **F** 0.037 0.043 G 0.090 BSC 2.29 E H 0.034 0.040 0.87 2.29 BSC 1.01 J 0.018 0.023 0.46 0.58 0.134 0.142 3.40 3.60 R 0.180 0.215 4.57 5.46 V 0.035 0.050 0.89 1.27

W 0.000 0.010 0.000 0.25

1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: INCH.

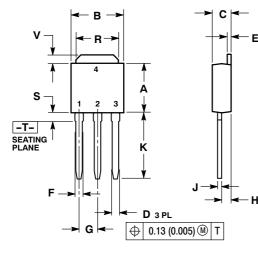
SEATING PLANE IS ON TOP OF DAMBAR POSITION.

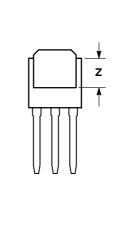
NOTES

2

З.

IPAK (STRAIGHT LEAD DPAK) CASE 369D-01 **ISSUE B**





- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	ETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.235	0.245	5.97	6.35	
В	0.250	0.265	6.35	6.73	
С	0.086	0.094	2.19	2.38	
D	0.027	0.035	0.69	0.88	
Е	0.018	0.023	0.46	0.58	
F	0.037	0.045	0.94	1.14	
G	0.090	BSC	2.29 BSC		
н	0.034	0.040	0.87	1.01	
J	0.018	0.023	0.46	0.58	
κ	0.350	0.380	8.89	9.65	
R	0.180	0.215	4.45	5.45	
S	0.025	0.040	0.63	1.01	
V	0.035	0.050	0.89	1.27	
Ζ	0.155		3.93		
STYLE 2: PIN 1. GATE					

2 DRAIN SOURCE 3. 4. DRAIN

ON Semiconductor and 💷 are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC observed on the paper of the provided in the evaluation of the rights of others. SCILLC products are not designed, intended, or authorized for use a components in systems intended for surgical implant into the body, or other applications. bit intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NTD4815NH/D