NSCT2222ALT1G

General Purpose Transistor

NPN Silicon

Features

- These are Pb−Free Devices

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	40	Vdc
Collector−Base Voltage	V_{CBO}	75	Vdc
Emitter−Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	600	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate (Note 2) T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

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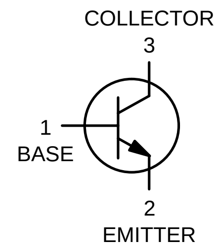
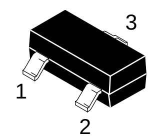
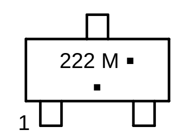
http://onsemi.com





SOT−23
CASE 318
STYLE 6

MARKING DIAGRAM



222 = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
NSCT2222ALT1G	SOT−23 (Pb−Free)	3000 Tape & Reel
NSCT2222ALT3G	SOT−23 (Pb−Free)	10000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

May, 2006 − Rev. 0

Publication Order Number:
NSCT2222ALT1/D

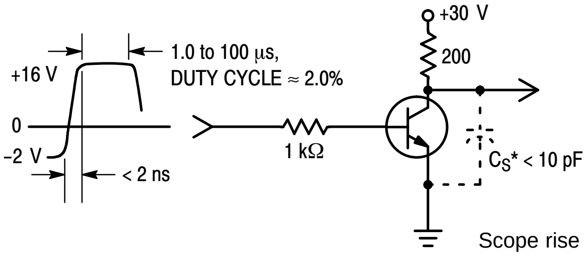
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

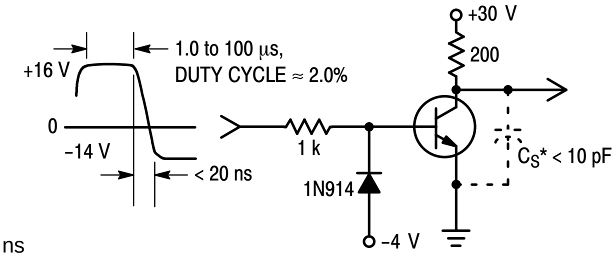
Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)		$V_{(BR)CEO}$	40	−	Vdc
Collector−Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)		$V_{(BR)CBO}$	75	−	Vdc
Emitter−Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	6.0	−	Vdc
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)		I_{CEX}	−	10	nAdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 60 Vdc, I_E = 0, T_A = 125°C)		I_{CBO}	 − −	 0.01 10	μAdc
Emitter Cutoff Current (V_{EB} = 3.0 Vdc, I_C = 0)		I_{EBO}	−	100	nAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)		I_{BL}	−	20	nAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.1 mAdc, V_{CE} = 10 Vdc) (I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = −55°C) (I_C = 150 mAdc, V_{CE} = 10 Vdc) (Note 3) (I_C = 150 mAdc, V_{CE} = 1.0 Vdc) (Note 3) (I_C = 500 mAdc, V_{CE} = 10 Vdc) (Note 3)		h_{FE}	 35 50 75 35 100 50 40	 − − − − 300 − −	−
Collector−Emitter Saturation Voltage (Note 3) (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{CE(sat)}$	 − −	 0.3 1.0	Vdc
Base−Emitter Saturation Voltage (Note 3) (I_C = 150 mAdc, I_B = 15 mAdc) (I_C = 500 mAdc, I_B = 50 mAdc)		$V_{BE(sat)}$	 0.6 −	 1.2 2.0	Vdc
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product (Note 4) (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)		f_T	 300	 −	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	−	8.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	−	25	pF
Input Impedance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{ie}	 2.0 0.25	 8.0 1.25	kΩ
Voltage Feedback Ratio (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{re}	 − −	 8.0 4.0	X 10^{-4}
Small−Signal Current Gain (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{fe}	 50 75	 300 375	−
Output Admittance (I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz) (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		h_{oe}	 5.0 25	 35 200	μmhos
Collector Base Time Constant (I_E = 20 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)		rb, C_c	 −	 150	ps
Noise Figure (I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 1.0 kΩ, f = 1.0 kHz)		NF	 −	 4.0	dB
SWITCHING CHARACTERISTICS					
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = −0.5 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc)	t_d	−	10	ns
Rise Time		t_r	−	25	
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc)	t_s	−	225	ns
Fall Time		t_f	−	60	

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

4. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

SWITCHING TIME EQUIVALENT TEST CIRCUITS





Scope rise time < 4 ns
*Total shunt capacitance of test jig, connectors, and oscilloscope.

Figure 1. Turn−On Time

Figure 2. Turn−Off Time

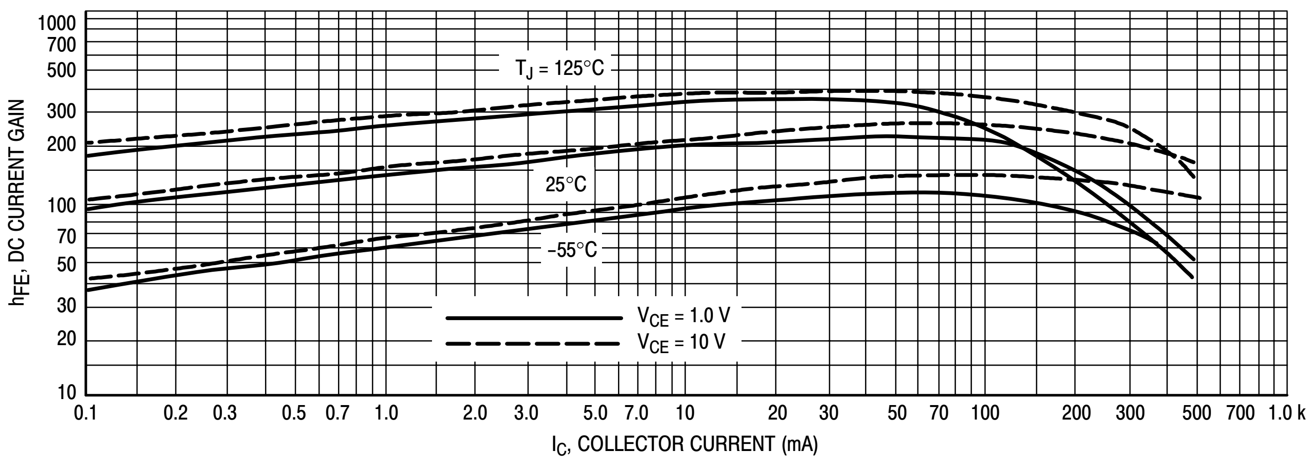


Figure 3. DC Current Gain

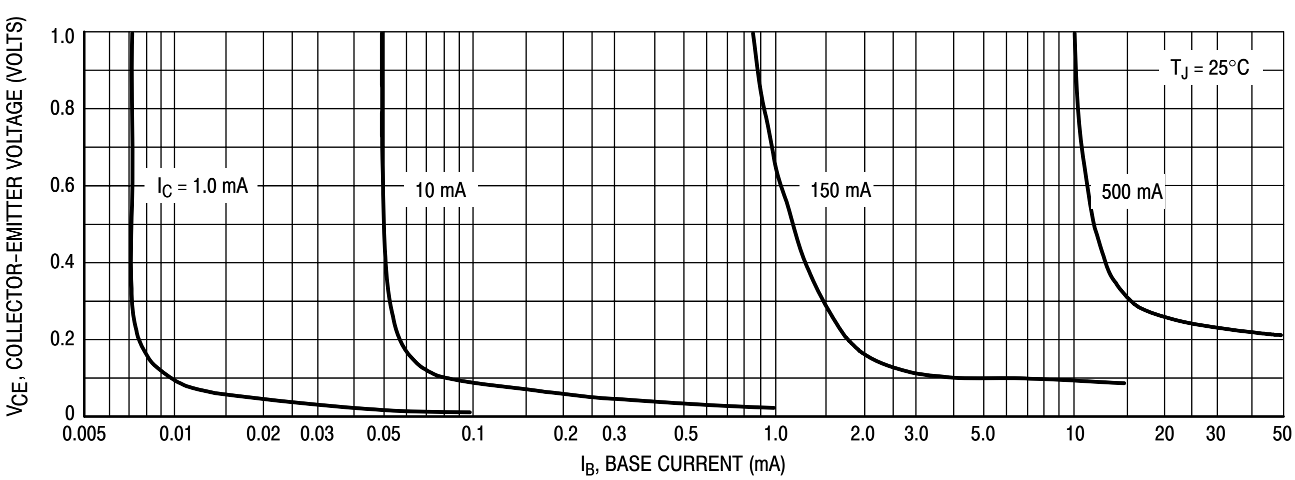


Figure 4. Collector Saturation Region

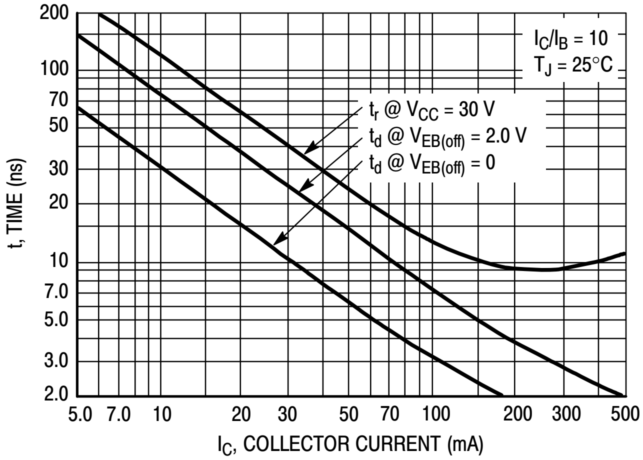


Figure 5. Turn−On Time

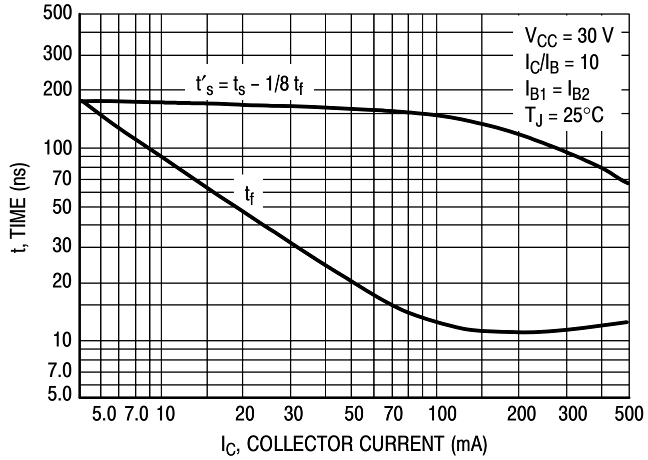


Figure 6. Turn−Off Time

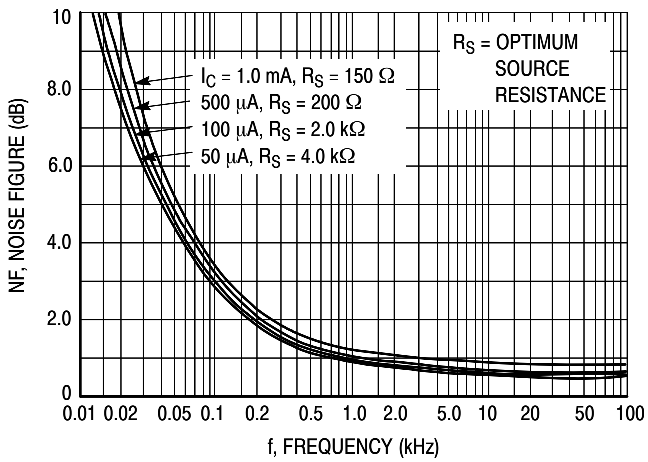


Figure 7. Frequency Effects

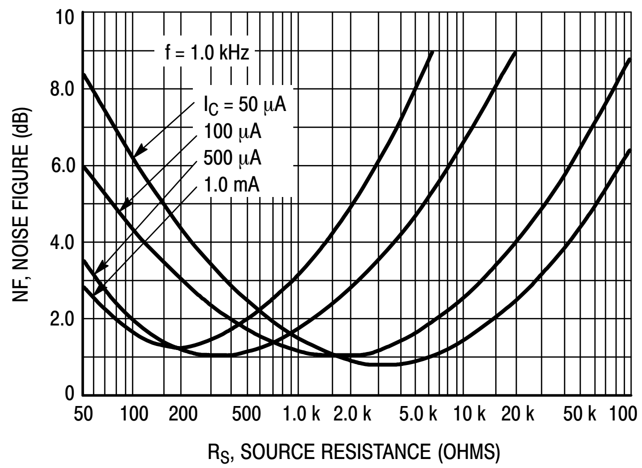


Figure 8. Source Resistance Effects

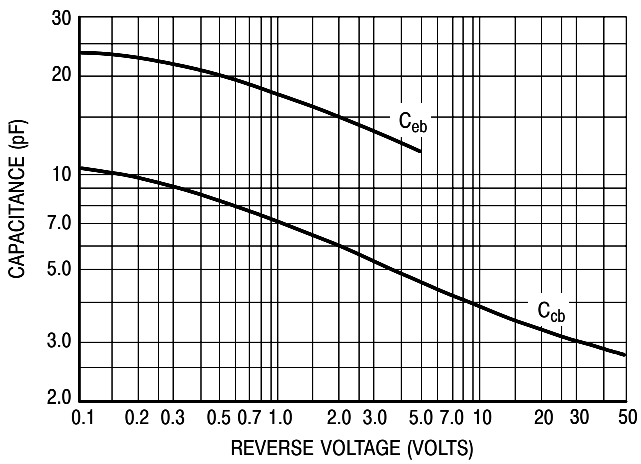


Figure 9. Capacitances

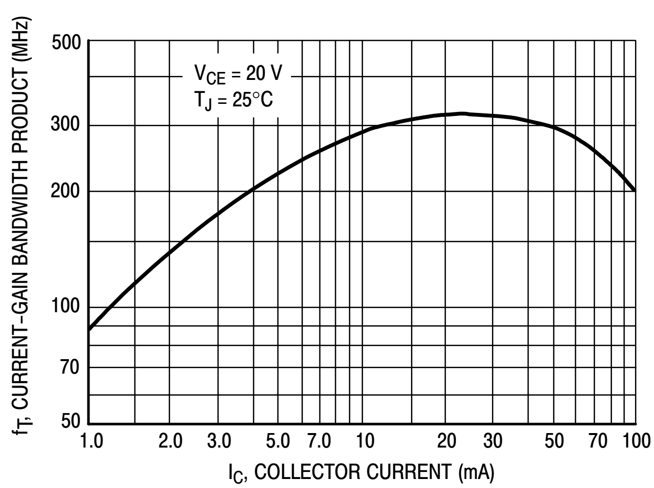


Figure 10. Current−Gain Bandwidth Product

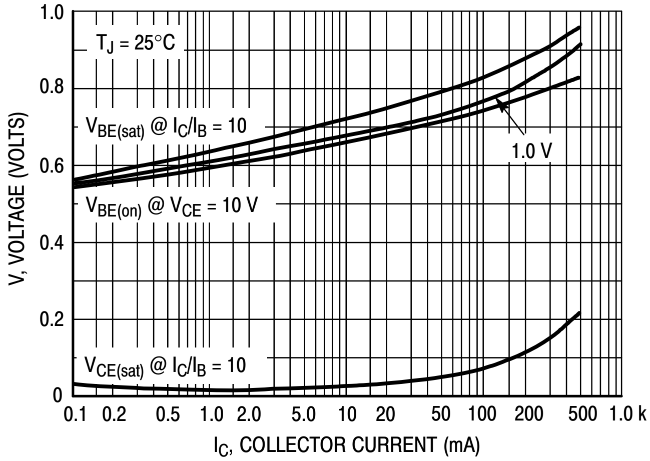


Figure 11. "On" Voltages

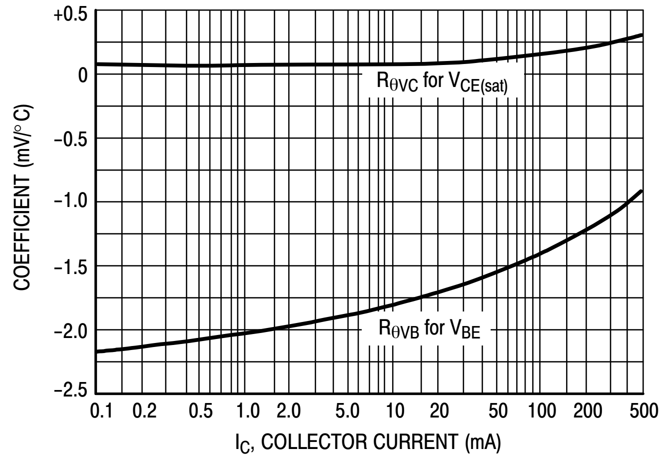
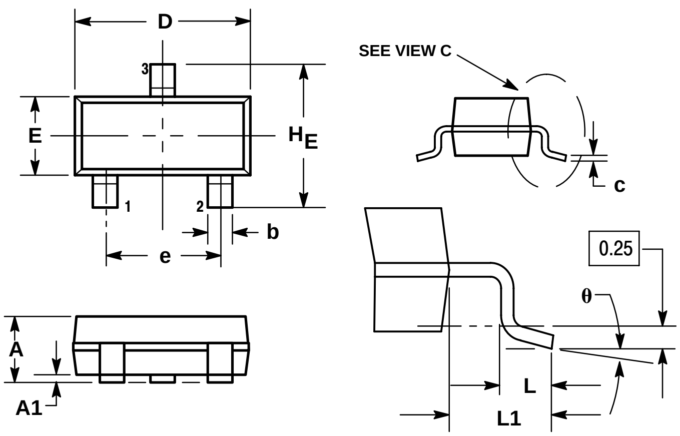


Figure 12. Temperature Coefficients

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AN



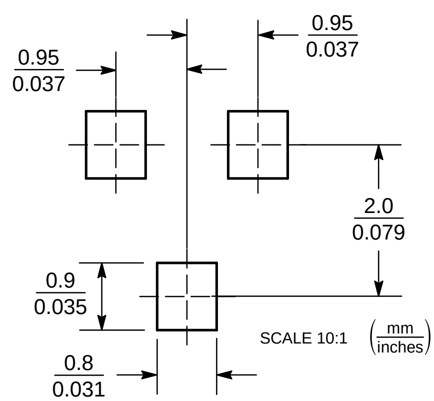
VIEW C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318−01 THRU −07 AND −09 OBSOLETE, NEW STANDARD 318−08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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