

NP0A456

Silicon PNP epitaxial planar type

For High speed switching

■ Features

- Suitable for high-density mounting and downsizing of the equipment
- Automatic insertion with the taping is possible

■ Basic Part Number

- 2SA2082 × 2

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

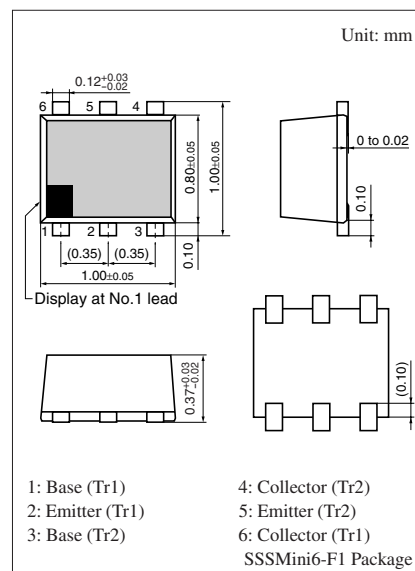
Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	-15	V
Collector-emitter voltage (Base open)	V_{CEO}	-15	V
Emitter-base voltage (Collector open)	V_{EBO}	-4	V
Collector current	I_C	-50	mA
Peak collector current	I_{CP}	-100	mA
Total power dissipation *	P_T	125	mW
Junction temperature	T_j	125	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Note) *: Measuring on substrate at 17 mm × 10 mm × 1 mm

■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

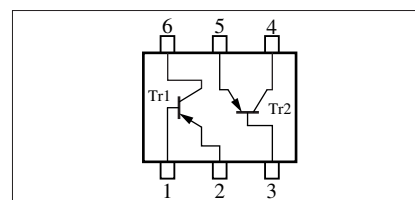
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = -8\text{ V}, I_E = 0$			- 0.1	μA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = -3\text{ V}, I_C = 0$			- 0.1	μA
Forward current transfer ratio	h_{FE1}	$V_{CE} = -1\text{ V}, I_C = -10\text{ mA}$	50		150	—
	h_{FE2}	$V_{CE} = -1\text{ V}, I_C = -1\text{ mA}$	30			
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10\text{ mA}, I_B = -1\text{ mA}$		- 0.1	- 0.2	V
Transition frequency	f_T	$V_{CB} = -10\text{ V}, I_E = 10\text{ mA}, f = 200\text{ MHz}$	800	1 500		MHz
Collector output capacitance (Common base, input open circuited)	C_{ob}	$V_{CB} = -5\text{ V}, I_E = 0, f = 1\text{ MHz}$		1		pF
Turn-on time	t_{on}	Refer to the switching time measurement circuit		12		ns
Turn-off time	t_{off}			20		ns
Storage time	t_{stg}			19		ns

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

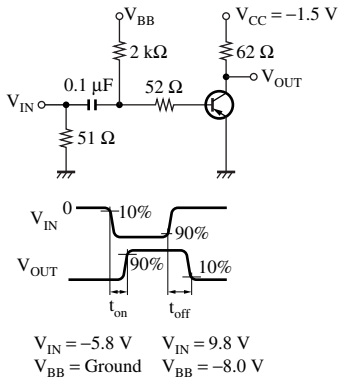
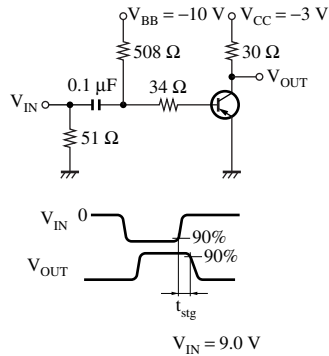
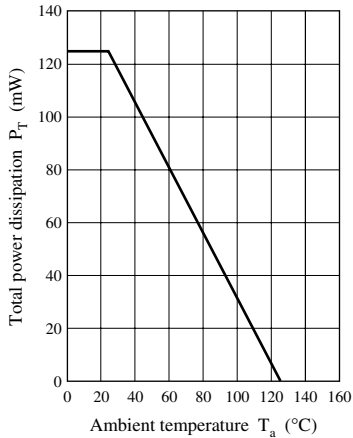
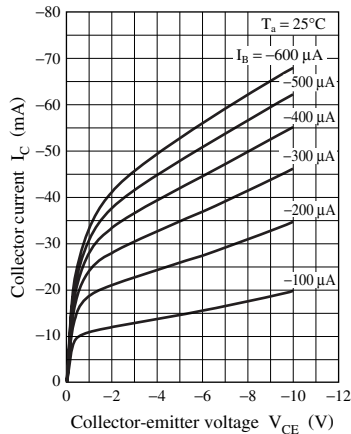
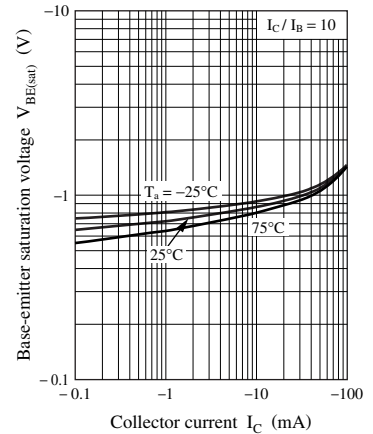
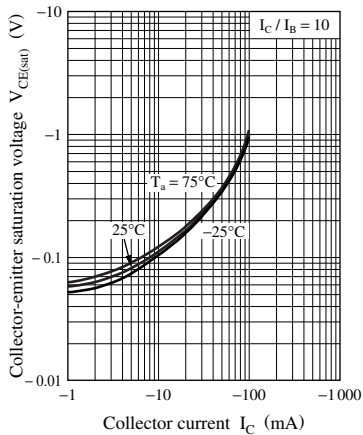
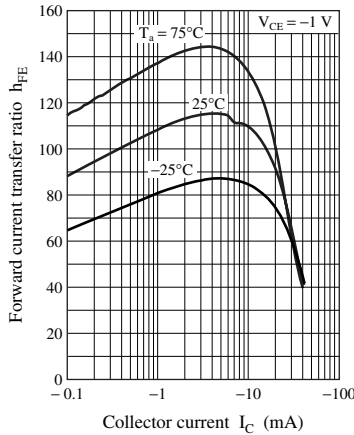
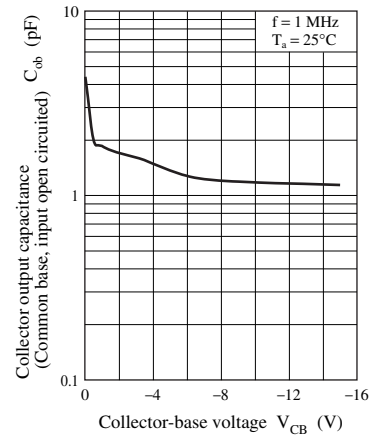


Marking Symbol: 3E

Internal Connection



Switching time measurement circuit

 t_{on} , t_{off} test circuit t_{stg} test circuit $P_T - T_a$  $I_C - V_{CE}$  $V_{BE(sat)} - I_C$  $V_{CE(sat)} - I_C$  $h_{FE} - I_C$  $C_{ob} - V_{CB}$ 

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