3.3 V 1:2 AnyLevel™ Input to LVDS Fanout Buffer / Translator

Description

The NB6N11S is a differential 1:2 Clock or Data Receiver and will accept AnyLevel input signals: LVPECL, CML, LVCMOS, LVTTL, or LVDS. These signals will be translated to LVDS and two identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6N11S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The NB6N11S has a wide input common mode range from GND + 50 mV to V_{CC} – 50 mV. Combined with the 50 Ω internal termination resistors at the inputs, the NB6N11S is ideal for translating a variety of differential or single-ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6N11S is functionally equivalent to the EP11, LVEP11, SG11 or 7L11M devices and is offered in a small, 3 mm X 3 mm, 16-QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB6N11S is a member of the ECLinPS MAX[™] family of high performance products.

Features

- Maximum Input Clock Frequency > 2.0 GHz
- Maximum Input Data Rate > 2.5 Gb/s
- 1 ps Maximum of RMS Clock Jitter
- Typically 10 ps of Data Dependent Jitter
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- Functionally Compatible with Existing 3.3 V LVEL, LVEP, EP, and SG Devices
- These are Pb-Free Devices

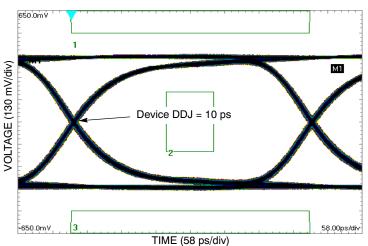


Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS 2^{23-1} (V_{INPP} = 400 mV; Input Signal DDJ = 14 ps)



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MARKING DIAGRAM*



QFN-16 MN SUFFIX CASE 485G



A = Assembly Location

L = Wafer Lot

Y = Year

W = Work Week

■ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

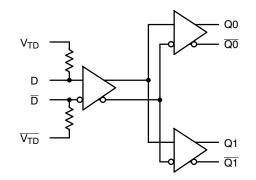


Figure 1. Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

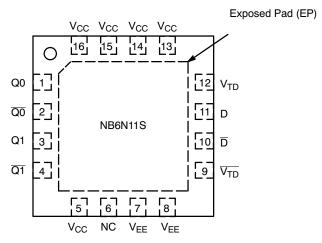


Figure 3. NB6N11S Pinout, 16-pin QFN (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	Q0	LVDS Output	Non-inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
2	Q0	LVDS Output	Inverted D output. Typically loaded with 10 Ω receiver termination resistor across differential pair.
3	Q1	LVDS Output	Non-inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
4	Q1	LVDS Output	Inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
5	V _{CC}	-	Positive Supply Voltage
6	NC		No Connect
7	V _{EE}		Negative Supply Voltage
8	V _{EE}		Negative Supply Voltage
9	$\overline{V_{TD}}$	-	Internal 50 Ω termination pin for \overline{D}
10	D	LVPECL, CML, LVDS, LVCMOS, LVTTL	Inverted Differential Clock/Data Input (Note 1)
11	D	LVPECL, CML, LVDS, LVCMOS, LVTTL	Non-inverted Differential Clock/Data Input (Note 1)
12	V_{TD}	-	Internal 50 Ω termination pin for \overline{D}
13	V _{CC}	-	Positive Supply Voltage
14	V _{CC}	-	Positive Supply Voltage
15	V _{CC}	-	Positive Supply Voltage
16	V _{CC}	-	Positive Supply Voltage
EP			Exposed pad. The exposed pad (EP) on the package bottom must be attached to a heat-sinking conduit. The exposed pad may only be electrically connected to V_{EE} .

^{1.} In the differential configuration when the input termination pins (VTD/VTD) are connected to a common termination voltage or left open, and if no signal is applied on D/D inputs, then the device will be susceptible to self oscillation.

Table 2. ATTRIBUTES

Charact	Value				
ESD Protection	> 2 kV > 200 V > 1 kV				
Moisture Sensitivity, Indefinite	Pb Pkg	Pb-Free Pkg			
	QFN-16	-	1		
Flammability Rating	UL 94 V-0	@ 0.125 in			
Transistor Count	225 D	evices			
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test					

^{2.} For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		3.8	V
V _{IN}	Positive Input	GND = 0 V	$V_{IN} \leq V_{CC}$	3.8	V
I _{IN}	Input Current Through R _T (50 Ω Resistor)	Static Surge		35 70	mA mA
I _{OSC}	Output Short Circuit Current Line-to-Line (Q to $\overline{\mathbf{Q}}$) Line-to-End (Q or $\overline{\mathbf{Q}}$ to GND)	Q or Q Q to Q to GND	Continuous Continuous	12 24	mA
T _A	Operating Temperature Range	QFN-16		-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN-16 QFN-16	41.6 35.2	°C/W
θЈС	Thermal Resistance (Junction-to-Case)	1S2P (Note 3)	QFN-16	4.0	°C/W
T _{sol}	Wave Solder Pb Pb-Free			265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

^{3.} JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

 $\textbf{Table 4. DC CHARACTERISTICS, CLOCK INPUTS, LVDS OUTPUTS} \ \ V_{CC} = 3.0 \ \ V \ \ to \ 3.6 \ \ V, \ GND = 0 \ \ V, \ T_{A} = -40 \ \ C \ \ to \ +85 \ \ C \$

Symbol	Characteristic	Min	Тур	Max	Unit
I _{CC}	Power Supply Current (Note 8)		35	50	mA
DIFFERE	NTIAL INPUTS DRIVEN SINGLE-ENDED (Figures 11, 12, 16, and 18)	•	•	•	•
V _{th}	Input Threshold Reference Voltage Range (Note 7)	GND +100		V _{CC} - 100	mV
V _{IH}	Single-ended Input HIGH Voltage	V _{th} + 100		V _{CC}	mV
V _{IL}	Single-ended Input LOW Voltage	GND	GND		mV
DIFFERE	ENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7, 8, 9, 10, 17, and 19)				
V_{IHD}	Differential Input HIGH Voltage	100		V _{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V _{CC} - 100	mV
V_{CMR}	Input Common Mode Range (Differential Configuration)	GND + 50		V _{CC} - 50	mV
V_{ID}	Differential Input Voltage (V _{IHD} - V _{ILD})	100		V _{CC}	mV
R _{TIN}	Internal Input Termination Resistor	40	50	60	Ω
LVDS OL	JTPUTS (Note 4)				
V _{OD}	Differential Output Voltage	250		450	mV
ΔV_{OD}	Change in Magnitude of V _{OD} for Complementary Output States (Note 9)	0	1	25	mV
Vos	Offset Voltage (Figure 15)	1125		1375	mV
ΔV_{OS}	Change in Magnitude of V _{OS} for Complementary Output States (Note 9)	0	1	25	mV
V _{OH}	Output HIGH Voltage (Note 5)		1425	1600	mV
V _{OL}	Output LOW Voltage (Note 6)	900	1075		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 4. LVDS outputs require 100 Ω receiver termination resistor between differential pair. See Figure 14.

- V_{OH}max = V_{OS}max + ½ V_{OD}max.
 V_{OL}max = V_{OS}min ½ V_{OD}max.
 V_{th} is applied to the complementary input when operating in single-ended mode.
- 8. Input termination pins open, D/ \overline{D} at the DC level within V_{CMR} and output pins loaded with R_L = 100 Ω across differential.
- 9. Parameter guaranteed by design verification not tested in production.

Table 5. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0 V; (Note 10)

		-40°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V _{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \le 1.0$ GHz (Figure 4) $f_{in} = 1.5$ GHz $f_{in} = 2.0$ GHz	220 200 170	350 300 270		250 200 170	350 300 270		250 200 170	350 300 270		mV
f _{DATA}	Maximum Operating Data Rate	1.5	2.5		1.5	2.5		1.5	2.5		Gb/s
t _{PLH} , t _{PHL}	Differential Input to Differential Output Propagation Delay	270	370	470	270	370	470	270	370	470	ps
t _{SKEW}	Duty Cycle Skew (Note 11) Within Device Skew (Note 16) Device-to-Device Skew (Note 15)		8 5 30	45 25 100		8 5 30	45 25 100		8 5 30	45 25 100	ps
UITTER	RMS Random Clock Jitter (Note 13) $ \begin{aligned} &f_{\text{in}} = 1.0 \text{ GHz} \\ &f_{\text{in}} = 1.5 \text{ GHz} \end{aligned} $ Deterministic Jitter (Note 14) $ \begin{aligned} &f_{\text{DATA}} = 622 \text{ Mb/s} \\ &f_{\text{DATA}} = 1.5 \text{ Gb/s} \\ &f_{\text{DATA}} = 2.488 \text{ Gb/s} \end{aligned} $		0.5 0.5 6 7 10	1 1 20 20		0.5 0.5 6 7 10	1 1 20 20		0.5 0.5 6 7 10	1 1 20 20	ps
V _{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 12)	100		V _{CC} - GND	100		V _{CC} - GND	100		V _{CC} - GND	mV
t _r t _f	Output Rise/Fall Times @ 250 MHz $$ Q, \overline{Q} (20% – 80%)	70	120	170	70	120	170	70	120	170	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

^{16.} The worst case condition between $Q0/\overline{Q0}$ and $Q1/\overline{Q1}$ from either $D0/\overline{D0}$ or $D1/\overline{D1}$, when both outputs have the same transition.

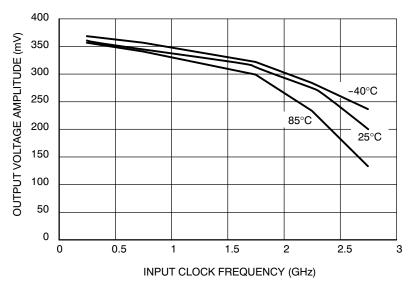


Figure 4. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) and Temperature (@ V_{CC} = 3.3 V)

^{10.} Measured by forcing $V_{INPPmin}$ with 50% duty cycle clock source and V_{CC} – 1400 mV offset. All loading with an external R_L = 100 Ω across "D" and "D" of the receiver. Input edge rates 150 ps (20%–80%).

^{11.} See Figure 13 differential measurement of t_{skew} = |t_{PLH} - t_{PHL}| for a nominal 50% differential clock input waveform @ 250 MHz.

^{12.} Input voltage swing is a single-ended measurement operating in differential mode.

^{13.} RMS jitter with 50% Duty Cycle clock signal at 750 MHz.

^{14.} Deterministic jitter with input NRZ data at PRBS 2²³-1 and K28.5.

^{15.} Skew is measured between outputs under identical transition @ 250 MHz.

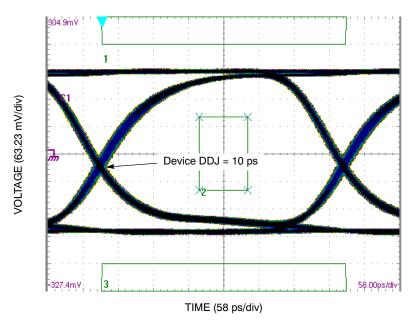


Figure 5. Typical Output Waveform at 2.488 Gb/s with PRBS 2^{23-1} and OC48 mask ($V_{INPP} = 100$ mV; Input Signal DDJ = 14 ps)

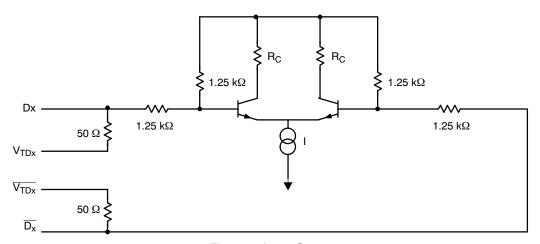


Figure 6. Input Structure

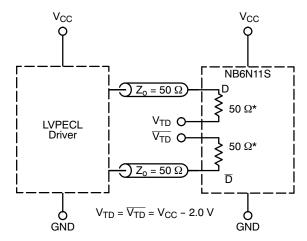


Figure 7. LVPECL Interface

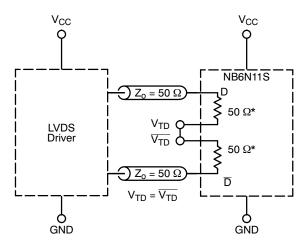


Figure 8. LVDS Interface

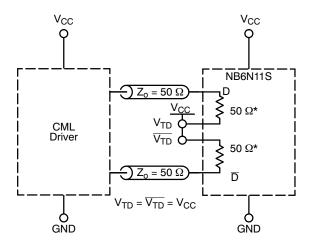


Figure 9. Standard 50 Ω Load CML Interface

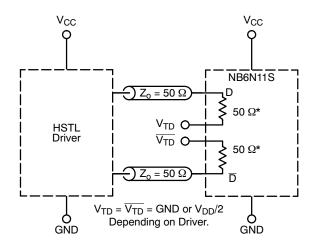


Figure 10. HSTL Interface

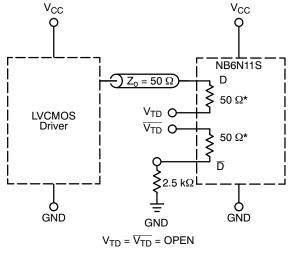


Figure 11. LVCMOS Interface

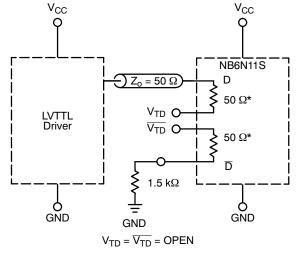


Figure 12. LVTTL Interface

^{*} R_{TIN} , Internal Input Termination Resistor.

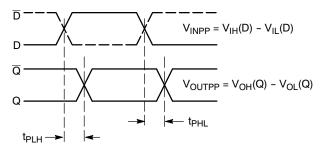


Figure 13. AC Reference Measurement

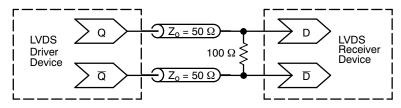
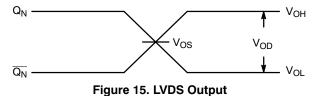


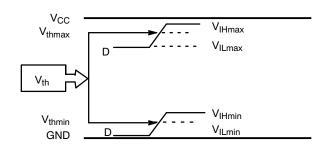
Figure 14. Typical LVDS Termination for Output Driver and Device Evaluation

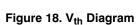


V_{IH}
V_{IL}
V_{th}
D
V_{th}

Figure 16. Differential Input Driven Single-Ended

Figure 17. Differential Inputs Driven Differentially





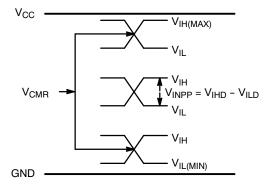


Figure 19. $V_{\rm CMR}$ Diagram

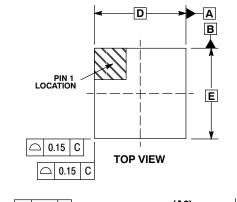
ORDERING INFORMATION

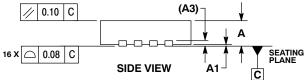
Device	Package	Shipping [†]		
NB6N11SMNG	QFN-16, 3 X 3 mm (Pb-Free)	123 Units / Rail		
NB6N11SMNR2G	QFN-16, 3 X 3 mm (Pb-Free)	3000 / Tape & Reel		

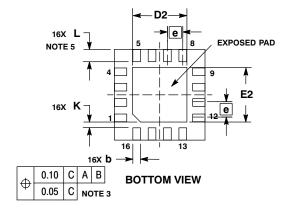
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS







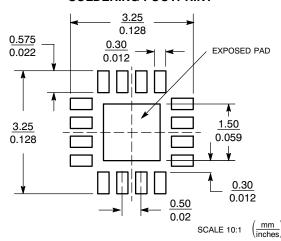


NOTES

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN
- 125 AND 0.30 MM FROM TERMINAL.
 COPLANARITY APPLIES TO THE EXPOSED
 PAD AS WELL AS THE TERMINALS.
 LIMB CONDITION CAN NOT VIOLATE 0.2 MM
 MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS					
DIM	MIN	MAX				
Α	0.80	1.00				
A1	0.00	0.05				
A3	0.20 REF					
b	0.18	0.30				
D	3.00 BSC					
D2	1.65	1.85				
E	3.00	BSC				
E2	1.65	1.85				
е	0.50 BSC					
K	0.18 TYP					
L	0.30	0.50				

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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