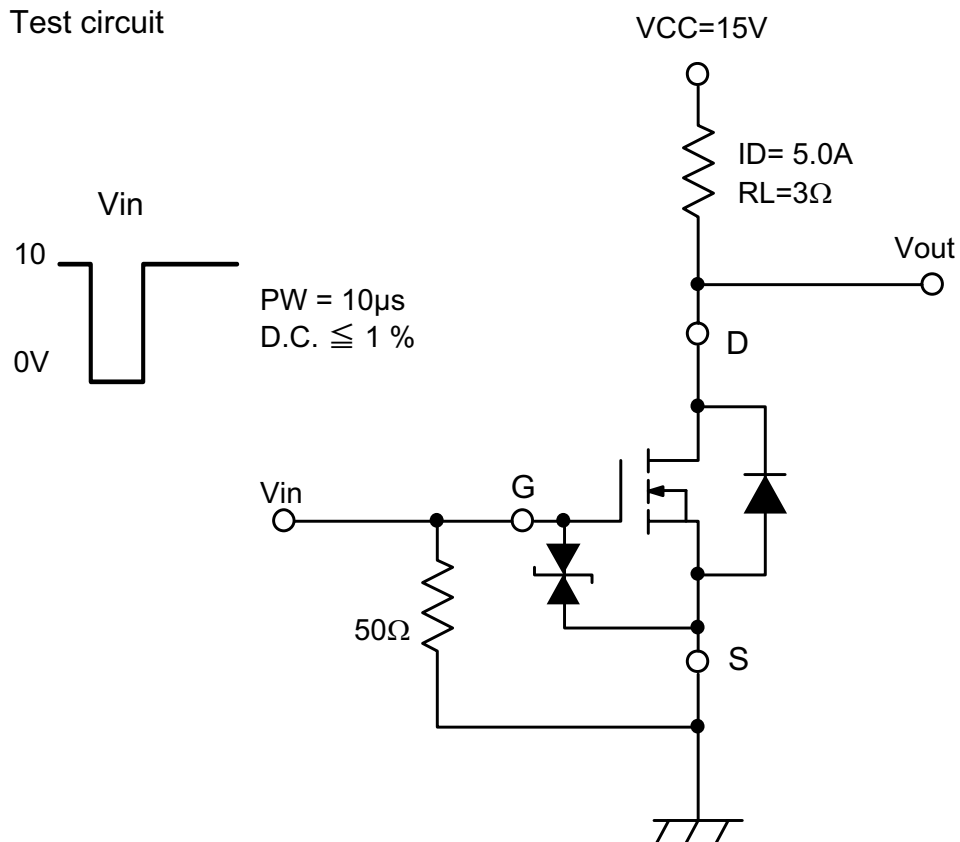


Product Specification TYPE NUMBER : M T M F 8 2 3 1 0 B B F *2					Prepared by S.Miyata	Checked by M.Fujisawa	Applied by H.Shidooka	Established by K.Kemichi	
Type	Silicon Field Effect Transistors								
Application	Li-ion battery								
Structure	N-Channel MOS Type								
Outline	SO8-F1-B					Marking		AA	
Absolute Maximum Ratings	VDSS 30 (V)	VGSS ±20 (V)	ID 18 (A)	IDp 72 (A)	PD ^{*3} 1.0 (W)	Tch 150 (°C)	Tstg -55 to +150 (°C)	Avalanche Current 18 (A)	
Electrical characteristics (Ta=25 °C ±3 °C)									
Item	Symbol	Measuring condition	Limit			Unit			
			min.	typ.	max.				
Drain-Source Voltage	VDSS	ID=1mA, VGS=0V	30			V			
Drain-Source Cutoff Current	IDSS	VDS=30V, VGS=0V			10	μA			
Gate-Source Cutoff Current	IGSS	VGS=±16V, VDS=0V			±10	μA			
Gate Threshold Voltage	Vth	ID=1.0mA, VDS=10.0V	1.4		2.5	V			
Drain Resistance (ON)	RDS(ON)	ID=5.0A, VGS=4.5V		6.5	9.8	mΩ			
Drain Resistance (ON)	RDS(ON)	ID=5.0A, VGS=10V		3.0	4.2	mΩ			
Forward Transfer Admittance	Yfs	ID=5.0A, VDS=10V	10			S			
Small-Signal Short-Circuit Input Capacitance	Ciss	VDS=10V, VGS=0V, f=1MHz		6000		pF			
Small-Signal Short-Circuit Output Capacitance	Coss	VDS=10V, VGS=0V, f=1MHz		690		pF			
Small-Signal Reverse Transfer Capacitance	Crss	VDS=10V, VGS=0V, f=1MHz		420		pF			
Single-pulse Avalanche Energy	Eas	VDD=24V, VGS=10→0V, ID=18A L=0.5mH,Rg=25Ω,Tch=25° C(initial)		162		mJ			
Turn-on Delay Time	td(on) *1	VDD=15V, VGS=0 to 10V, ID=5.0A		20		ns			
Rise Time	tr *1	VDD=15V, VGS=0 to 10V, ID=5.0A		30		ns			
Turn-off Delay Time	td(off) *1	VDD=15V, VGS=10 to 0V, ID=5.0A		400		ns			
Fall Time	tf *1	VDD=15V, VGS=10 to 0V, ID=5.0A		420		ns			
Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors. *1 See test circuit *2 Packing Embossed type (thermo-compressioon sealing) *3 Measuring on glass epoxy board at 25.4×25.4×0.8mm. Absolute maximum rating PD without heat sink shall be made 500mW.							Internally connected circuit 1.Source 2.Source 3.Source 4.Gate 5.Drain 6.Drain 7.Drain 8.Drain		
2008.01.31									
Established	Revised								

TYPE NUMBER

: M T M F 8 2 3 1 0 B B F
*2

Test circuit



2008.01.31

Established

Revised