DDR2 SDRAM Unbuffered DIMM (UDIMM)

MT9HTF3272A – 256MB

MT9HTF6472A – 512MB

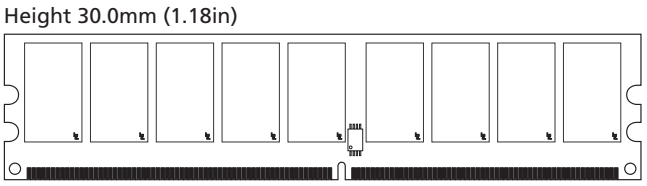
MT9HTF12872A – 1GB

For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400
- 256MB (32 Meg x 72), 512MB (64 Meg x 72), and 1GB (128 Meg x 72)
- $V_{DD} = V_{DD}Q = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Single rank
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts

Figure 1: 240-Pin DIMM (MO-237 R/C A/F)



Options — Marking

- Operating temperature[1]
  - Commercial ($0°C \le T_C \le +85°C$) — None
- Package
  - 240-pin DIMM (Pb-free) — Y
- Frequency/CAS latency
  - 2.5ns @ CL = 5 (DDR2-800)[2, 3] — -80E
  - 2.5ns @ CL = 6 (DDR2-800)[2, 3] — -800
  - 3.0ns @ CL = 5 (DDR2-667) — -667
  - 3.75ns @ CL = 4 (DDR2-533) — -53E
  - 5.0ns @ CL = 3 (DDR2-400) — -40E
- PCB height
  - 30mm (1.18in)

Notes: 1. Contact Micron for industrial temperature module offerings.
2. Contact Micron for product availability.
3. Not available in 256MB module density.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–	–	533	400	15	15	55
-40E	PC2-3200	–	–	400	400	15	15	55

Table 2: Addressing

	256MB	512MB	1GB
Refresh count	8K	8K	8K
Row address	8K (A0–A12)	16K (A0–A13)	16K (A0–A13)
Device bank address	4 (BA0, BA1)	4 (BA0, BA1)	8 (BA0, BA1, BA2)
Device page size per bank	1KB	1KB	1KB
Device configuration	256Mb (32 Meg x 8)	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)	1K (A0–A9)
Module rank address	1 (S0#)	1 (S0#)	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 256MB Modules

Base device: MT47H32M8[2], 256Mb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL-^{t}RCD-^{t}RP)
MT9HTF3272AY-667__	256MB	32 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF3272AY-53E__	256MB	32 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF3272AY-40E__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 512MB Modules

Base device: MT47H64M8[2], 512Mb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL-^{t}RCD-^{t}RP)
MT9HTF6472AY-80E__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF6472AY-800__	512MB	64 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF6472AY-667__	512MB	64 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF6472AY-53E__	512MB	64 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF6472AY-40E__	512MB	64 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 5: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT47H128M8[2], 1Gb DDR2 SDRAM

Part Number[1]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL-^{t}RCD-^{t}RP)
MT9HTF12872AY-80E__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT9HTF12872AY-800__	1GB	128 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT9HTF12872AY-667__	1GB	128 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT9HTF12872AY-53E__	1GB	128 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT9HTF12872AY-40E__	1GB	128 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Notes:
1. All part numbers end with a two-place code (not shown) designating component and PCB revisions. Consult factory for current revision codes. Example: MT9HTF6472AY-667C2.
2. Data sheets for the base devices can be found at www.micron.com.

Pin Assignments and Descriptions

Table 6: Pin Assignments

240-Pin UDIMM Front								240-Pin UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5
2	VSS	32	VSS	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	65	VSS	95	DQ42	125	DM0	155	DM3	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	VSS	96	DQ43	126	NC	156	NC	186	CK0#	216	VSS
7	DQS0	37	DQS3	67	VDD	97	VSS	127	VSS	157	VSS	187	VDD	217	DQ52
8	VSS	38	VSS	68	NC	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	VSS
10	DQ3	40	DQ27	70	A10/AP	100	VSS	130	VSS	160	VSS	190	BA1	220	CK2
11	VSS	41	VSS	71	BA0	101	SA2	131	DQ12	161	CB4	191	VDDQ	221	CK2#
12	DQ8	42	CB0	72	VDDQ	102	NC	132	DQ13	162	CB5	192	RAS#	222	VSS
13	DQ9	43	CB1	73	WE#	103	VSS	133	VSS	163	VSS	193	S0#	223	DM6
14	VSS	44	VSS	74	CAS#	104	DQS6#	134	DM1	164	DM8	194	VDDQ	224	NC
15	DQS1#	45	DQS8#	75	VDDQ	105	DQS6	135	NC	165	NC	195	ODT0	225	VSS
16	DQS1	46	DQS8	76	NC	106	VSS	136	VSS	166	VSS	196[2]	NC/A13	226	DQ54
17	VSS	47	VSS	77	NC	107	DQ50	137	CK1	167	CB6	197	VDD	227	DQ55
18	NC	48	CB2	78	VDDQ	108	DQ51	138	CK1#	168	CB7	198	VSS	228	VSS
19	NC	49	CB3	79	VSS	109	VSS	139	VSS	169	VSS	199	DQ36	229	DQ60
20	VSS	50	VSS	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	NC	201	VSS	231	VSS
22	DQ11	52	CKE0	82	VSS	112	VSS	142	VSS	172	VDD	202	DM4	232	DM7
23	VSS	53	VDD	83	DQS4#	113	DQS7#	143	DQ20	173	NC	203	NC	233	NC
24	DQ16	54[1]	NC/BA2	84	DQS4	114	DQS7	144	DQ21	174	NC	204	VSS	234	VSS
25	DQ17	55	NC	85	VSS	115	VSS	145	VSS	175	VDDQ	205	DQ38	235	DQ62
26	VSS	56	VDDQ	86	DQ34	116	DQ58	146	DM2	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC	177	A9	207	VSS	237	VSS
28	DQS2	58	A7	88	VSS	118	VSS	148	VSS	178	VDD	208	DQ44	238	VDDSPD
29	VSS	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	VSS	240	SA1

Notes: 1. Pin 54 is NC for 256MB and 512MB or BA2 for 1GB.
2. Pin 196 is NC for 256MB or A13 for 512MB and 1GB.

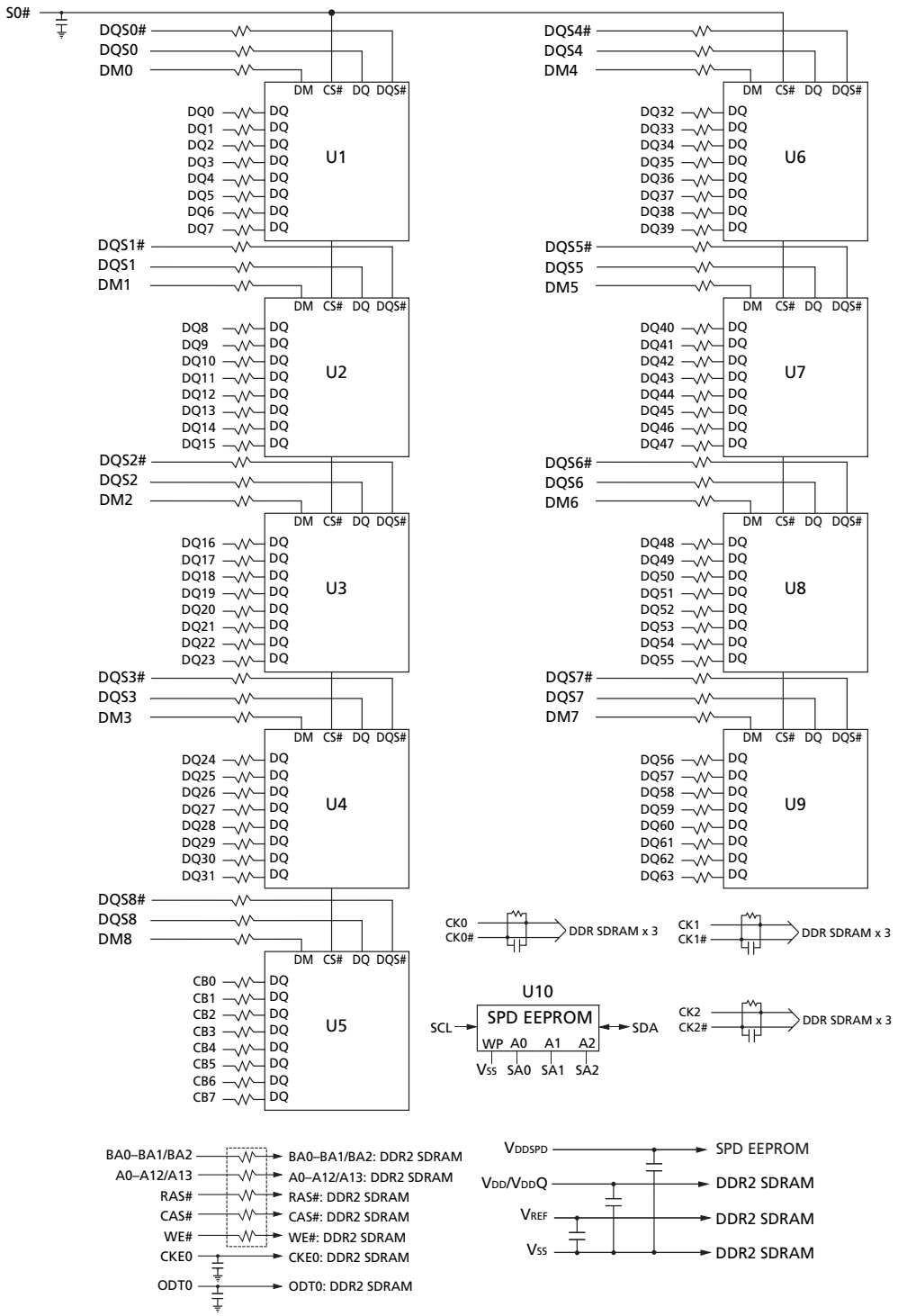
Table 7: Pin Descriptions

Pin numbers may not correlate with symbols; refer to Table 6 on page 3 for more information

Symbol	Type	Description
ODT0	Input (SSTL_18)	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, and DQS#. The ODT input will be ignored if disabled via the LOAD MODE command.
CK0, CK0#, CK1, CK1#, CK2, CK2#	Input (SSTL_18)	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input (SSTL_18)	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
S0#	Input (SSTL_18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
RAS#, CAS#, WE#	Input (SSTL_18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
BA0, BA1 (256MB, 512MB) BA0, BA1, BA2 (1GB)	Input (SSTL_18)	**Bank address inputs:** BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
A0–A12 (256MB) A0–A13 (512MB, 1GB)	Input (SSTL_18)	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0–SA2	Input	**Presence-detect address inputs:** These pins are used to configure the presence-detect device.
DQS0–DQS8, DQS0#–DQS8#	I/O (SSTL_18)	**Data strobe:** Output with read data, input with write data for source-synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
DM0–DM8 (DQS9–DQS17)	I/O (SSTL_18)	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. If RDQS is disabled, DQS0–DQS17 become DM0–DM8 and DQS9#–DQS17# are not used.
DQ0–DQ63	I/O (SSTL_18)	**Data input/output:** Bidirectional data bus.
CB0–CB7	I/O (SSTL_18)	ECC check bits.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
V_{DD}/$V_{DD}Q$	Supply	**Power supply:** 1.8V ±0.1V.
V_{REF}	Supply	SSTL_18 reference voltage.
V_{SS}	Supply	Ground.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +1.7V to +3.6V.
NC	–	No connect.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT9HTF3272A, MT9HTF6472A, and MT9HTF12872A DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 256MB, 512MB, and 1GB memory modules organized in a x72 configuration. These DDR2 SDRAM modules use internally configured 4-bank (256Mb, 512Mb) or 8-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to V_{SS} on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 8 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
V_{DD}/V_{DDQ}	V_{DD}/V_{DDQ} supply voltage relative to V_{SS}		–0.5	+2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		–0.5	+2.3	V
I_I	Input leakage current; Any input $0V \le V_{IN} \le V_{DD}$; V_{REF} input $0V \le V_{IN} \le 0.95V$; (All other pins not under test = 0V)	Command/address RAS#, CAS#, WE#, S#, CKE, ODT, BA	–45	+45	µA
		CK, CK#	–15	+15	
		DM	–5	+5	
I_{OZ}	Output leakage current; $0V \le V_{OUT} \le V_{DDQ}$; DQs and ODT are disabled	DQ, DQS, DQS#	–5	+5	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–18	+18	µA
T_C[2]	DDR2 SDRAM device operating temperature[1]	Commercial	0	+85	°C

Notes:
1. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site: www.micron.com/technotes.
2. Refresh rate is required to double when T_C exceeds 85°C.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site: www.micron.com. Module speed grades correlate with component speed grades, as shown in Table 9.

Table 9: Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-5E

IDD Specifications

Table 10: DDR2 IDD Specifications and Conditions – 256MB

Values shown for MT47H32M8 DDR2 SDRAM only and are computed from values specified in the 256Mb (32 Meg x 8) component data sheet

Parameter/Condition		Symbol	-667	-53E	-40E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	810	720	675	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	900	810	765	mA
Precharge power-down current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	45	45	45	mA
Precharge quiet standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	360	315	225	mA
Precharge standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	360	315	270	mA
Active power-down current: All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P	270	225	180	mA
	Slow PDN exit MR[12] = 1		54	54	54	mA
Active standby current: All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	450	360	270	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,710	1,440	1,125	mA
Operating burst read current: All device banks open; Continuous burst reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,620	1,350	1,035	mA
Burst refresh current: ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	1,620	1,530	1,485	mA
Self refresh current: CK and CK# at 0V; CKE ≤0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	45	45	45	mA
Operating bank interleave read current: All device banks interleaving reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 x ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching		IDD7	2,250	2,160	2,070	mA

Table 11: DDR2 IDD Specifications and Conditions – 512MB

Values shown for MT47H64M8 DDR2 SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	900	810	720	720	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	1,035	945	855	810	mA
Precharge power-down current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	63	63	63	63	mA
Precharge quiet standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	450	405	360	315	mA
Precharge standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	495	450	405	360	mA
Active power-down current: All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P	360	315	270	225	mA
	Slow PDN exit MR[12] = 1		108	108	108	108	mA
Active standby current: All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	630	58	495	405	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,755	1,530	1,260	1,035	mA
Operating burst read current: All device banks open; Continuous burst reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,845	1,620	1,305	1,035	mA
Burst refresh current: ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,070	1,620	1,530	1,485	mA
Self refresh current: CK and CK# at 0V; CKE ≤0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	63	63	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 x ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching		IDD7	2,700	2,160	2,025	1,980	mA

Table 12: DDR2 IDD Specifications and Conditions (Die Revision A) – 1GB

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	900	810	720	630	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	990	900	855	720	mA
Precharge power-down current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	63	63	63	63	mA
Precharge quiet standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	585	495	369	315	mA
Precharge standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	630	540	405	360	mA
Active power-down current: All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P	405	360	315	315	mA
	Slow PDN exit MR[12] = 1		126	126	126	126	mA
Active standby current: All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	675	630	495	405	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,665	1,440	1,170	990	mA
Operating burst read current: All device banks open; Continuous burst reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,710	1,440	1,305	990	mA
Burst refresh current: ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,520	2,340	2,250	1,980	mA
Self refresh current: CK and CK# at 0V; CKE ≤0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	63	63	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 x ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching		IDD7	3,015	2,700	2,610	2,340	mA

Table 13: DDR2 IDD Specifications and Conditions (Die Revision E) – 1GB

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/ -800	-667	-53E	-40E	Units
Operating one bank active-precharge current: ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD0	810	765	630	630	mA
Operating one bank active-read-precharge current: IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RAS = ^{t}RAS MIN (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W		IDD1	990	900	855	810	mA
Precharge power-down current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2P	63	63	63	63	mA
Precharge quiet standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		IDD2Q	450	360	360	315	mA
Precharge standby current: All device banks idle; ^{t}CK = ^{t}CK (IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		IDD2N	450	360	360	315	mA
Active power-down current: All device banks open; ^{t}CK = ^{t}CK (IDD); CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P	360	270	270	270	mA
	Slow PDN exit MR[12] = 1		90	90	90	90	mA
Active standby current: All device banks open; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD3N	540	495	405	360	mA
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4W	1,440	1,215	1,125	945	mA
Operating burst read current: All device banks open; Continuous burst reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = 0; ^{t}CK = ^{t}CK (IDD), ^{t}RAS = ^{t}RAS MAX (IDD), ^{t}RP = ^{t}RP (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		IDD4R	1,440	1,215	1,125	945	mA
Burst refresh current: ^{t}CK = ^{t}CK (IDD); REFRESH command at every ^{t}RFC (IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		IDD5	2,115	1,935	1,890	1,845	mA
Self refresh current: CK and CK# at 0V; CKE ≤0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		IDD6	63	63	63	63	mA
Operating bank interleave read current: All device banks interleaving reads; IOUT = 0mA; BL = 4, CL = CL (IDD), AL = ^{t}RCD (IDD) - 1 x ^{t}CK (IDD); ^{t}CK = ^{t}CK (IDD), ^{t}RC = ^{t}RC (IDD), ^{t}RRD = ^{t}RRD (IDD), ^{t}RCD = ^{t}RCD (IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during DESELECTs; Data bus inputs are switching		IDD7	3,015	2,520	2,430	2,340	mA

Serial Presence-Detect

Table 14: Serial Presence-Detect EEPROM DC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} × 0.7	V_{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} × 0.3	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.10	3	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	3	µA
Standby current	I_{SB}	1.6	4	µA
Power supply current, READ: SCL clock frequency = 100 KHz	ICC_R	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 KHz	ICC_W	2	3	mA

Table 15: Serial Presence-Detect EEPROM AC Operating Conditions
All voltages referenced to V_{SS}; V_{DDSPD} = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^tAA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^tBUF	1.3	–	µs	
Data-out hold time	^tDH	200	–	ns	
SDA and SCL fall time	^tF	–	300	ns	2
Data-in hold time	$^tHD:DAT$	0	–	µs	
Start condition hold time	$^tHD:STA$	0.6	–	µs	
Clock HIGH period	^tHIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^tI	–	50	ns	
Clock LOW period	^tLOW	1.3	–	µs	
SDA and SCL rise time	^tR	–	0.3	µs	2
SCL clock frequency	^fSCL	–	400	KHz	
Data-in setup time	$^tSU:DAT$	100	–	ns	
Start condition setup time	$^tSU:STA$	0.6	–	µs	3
Stop condition setup time	$^tSU:STO$	0.6	–	µs	
WRITE cycle time	^tWRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^tWRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

Table 16: Serial Presence-Detect Matrix

Byte	Description	Entry (Version)	256MB[1]	512MB	1GB
0	Number of SPD bytes used by Micron	128	80	80	80
1	Total number of bytes in SPD device	256	08	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08	08
3	Number of row addresses on SDRAM	13 or 14	0D	0E	0E
4	Number of column addresses on SDRAM	10	0A	0A	0A
5	DIMM height and module ranks	30mm, single rank	60	60	60
6	Module data width	72	48	48	48
7	Reserved	0	00	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05	05
9	SDRAM cycle time, ^{t}CK (CL = MAX value, see byte 18)	-80E/-800 -667 -53E -40E	– 30 3D 50	25 30 3D 50	25 30 3D 50
10	SDRAM access from clock, ^{t}AC (CL = MAX value, see byte 18)	-80E/-800 -667 -53E -40E	– 45 50 60	40 45 50 60	40 45 50 60
11	Module configuration type	ECC	02	02	02
12	Refresh rate/type	7.81µs/SELF	82	82	82
13	SDRAM device width (primary SDRAM)	8	08	08	08
14	Error-checking SDRAM data width	8	08	08	08
15	Reserved	–	00	00	00
16	Burst lengths supported	4, 8	0C	0C	0C
17	Number of banks on SDRAM device	4 or 8	04	04	08
18	CAS latencies supported	-80E (5, 4) -800 (6, 5, 4) -667 (5, 4, 3) -53E/-40E (4, 3)	– – 38 18	30 70 38 18	30 70 38 18
19	Module thickness	–	01	01	01
20	DDR2 DIMM type	Unbuffered DIMM	02	02	02
21	SDRAM module attributes	No PLL or Reg	00	00	00
22	SDRAM device attributes: weak driver (01), or weak driver and 50Ω ODT (03)	-80E/-800/-667 -53E/-40E	– /– /3D 01	03 01	03 01
23	SDRAM cycle time, ^{t}CK, MAX CL - 1	-80E/-667 -800 -53E/-40E	– /3D – 50	3D 30 50	3D 30 50
24	SDRAM access from CK, ^{t}AC, MAX CL - 1	-80E/-800 -667 -53E -40E	– 45 50 60	40 45 50 60	40 45 50 60
25	SDRAM cycle time, ^{t}CK, MAX CL - 2	-80E/-800 -667 -53E/-40E	– 50 00	3D/00 50 00	3D/00 50 00
26	SDRAM access from CK, ^{t}AC, MAX CL - 2	-80E/-800 -667 -53E/-40E	– 45 00	40/00 45 00	40/00 45 00

Table 16: Serial Presence-Detect Matrix (Continued)

Byte	Description	Entry (Version)	256MB[1]	512MB	1GB
27	MIN row precharge time, ^{t}RP	-80E -800/-667 -53E/-40E	– –/3C 3C	32 3C 3C	32 3C 3C
28	MIN row active to row active, ^{t}RRD	–	1E	1E	1E
29	MIN RAS# to CAS# delay, ^{t}RCD	-80E -800/-667 -53E/-40E	– –/3C 3C	32 3C 3C	32 3C 3C
30	MIN active-to-precharge time, ^{t}RAS	-80E/-800 -667/-53E -40E	– 2D 28	2D 2D 28	2D 2D 28
31	Module rank density	256MB, 512MB,1GB	40	80	01
32	Address and command setup time, $^{t}IS_{b}$	-80E/-800 -667 -53E -40E	– 20 25 35	17 20 25 35	17 20 25 35
33	Address and command hold time, $^{t}IH_{b}$	-80E/-800 -667 -53E -40E	– 27 37 47	25 27 37 47	25 27 37 47
34	Data/data mask input setup time, $^{t}DS_{b}$	-80E/-800 -667/-53E -40E	– 10 15	05 10 15	05 10 15
35	Data/data mask input hold time, $^{t}DH_{b}$	-80E/-800 -667 -53E -40E	– 17 22 27	12 17 22 27	12 17 22 27
36	Write recovery time, ^{t}WR	–	3C	3C	3C
37	WRITE-to-READ command delay, ^{t}WTR	-80E/-667/-53E -800/-40E	– /1E/1E 28	1E 28	1E 28
38	READ-to-PRECHARGE command delay, ^{t}RTP	–	1E	1E	1E
39	Memory analysis probe	–	00	00	00
40	Extension for bytes 41 and 42	-80E -800/-667 -53E/-40E	– –/00 00	30 00 00	36 06 06
41	MIN active-to-active/refresh time, ^{t}RC[2]	-80E -800/-667/-53E -40E	– –/3C/3C 37	39 3C 37	39 3C 37
42	MIN AUTO REFRESH-to-ACTIVE/AUTO REFRESH command period, ^{t}RFC	–	4B	69	7F
43	SDRAM device MAX cycle time, ^{t}CK (MAX)	–	80	80	80
44	SDRAM device MAX DQS–DQ skew time, ^{t}DQSQ	-80E/-800 -667 -53E -40E	– 18 1E 23	14 18 1E 23	14 18 1E 23
45	SDRAM device MAX read data hold skew factor, ^{t}QHS	-80E/-800 -667 -53E -40E	– 22 28 2D	1E 22 28 2D	1E 22 28 2D

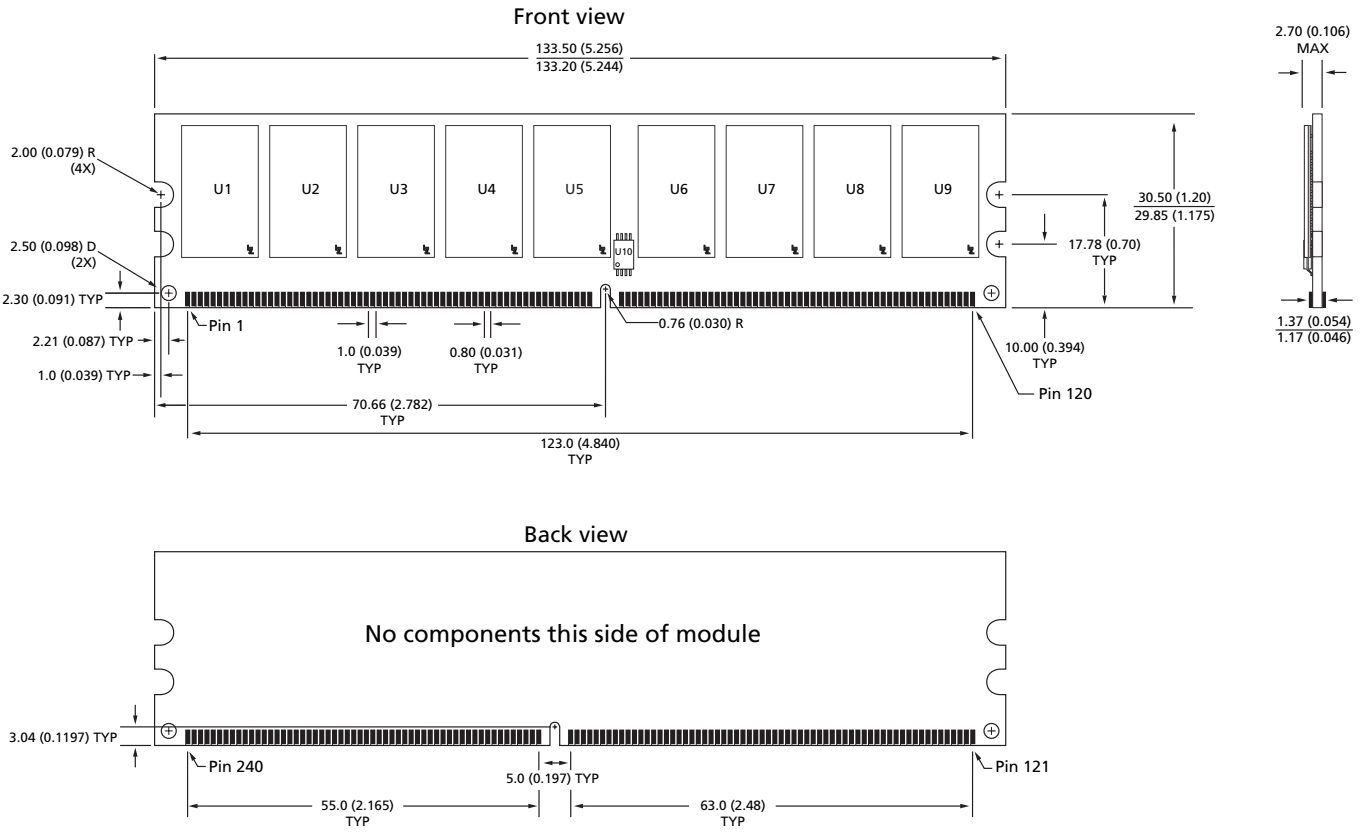
Table 16: Serial Presence-Detect Matrix (Continued)

Byte	Description	Entry (Version)	256MB[1]	512MB	1GB
46	PLL relock time	n/a	00	00	00
47–61	Optional features, not supported	–	00	00	00
62	SPD revision	Release 1.2	12	12	12
63	Checksum for bytes 0–62	-80E -800 -667 -53E -40E	– – FE A9 10	A1 42 5D 08 6F	42 E3 FE A9 10
64	Manufacturer's JEDEC ID code	MICRON	2C	2C	2C
65–71	Manufacturer's JEDEC ID code	(continued)	FF	FF	FF
72	Manufacturing location	01–12	01–0C	01–0C	01–0C
73–90	Module part number (ASCII)	–	Variable data	Variable data	Variable data
91	PCB identification code	1–9	01–09	01–09	01–09
92	Identification code (continued)	0	00	00	00
93	Year of manufacture in BCD	–	Variable data	Variable data	Variable data
94	Week of manufacture in BCD	–	Variable data	Variable data	Variable data
95–98	Module serial number	–	Variable data	Variable data	Variable data
99–127	Reserved for manufacturer-specific data	–	00	00	00
128–255	Reserved for customer-specific data	–	FF	FF	FF

Notes: 1. The 256MB module is not available in -80E and -800 speed grades.
2. The ^{t}RC SPD values shown are JEDEC DDR2 device specification values. The actual Micron DDR2 device specification is ^{t}RC = 55ns for all speed grades.

Module Dimensions

Figure 3: 240-Pin DDR2 UDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for complete design dimensions.

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