Mobile LPSDR

MT48H32M16LF – 8 Meg x 16 x 4 banks

MT48H16M32LF/LG – 4 Meg x 32 x 4 banks

Features

- Vdd/Vddq = 1.7–1.95V
- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Four internal banks for concurrent operation
- Programmable burst lengths: 1, 2, 4, 8, and continuous
- Auto precharge, includes concurrent auto precharge
- Auto refresh and self refresh modes
- LVTTL-compatible inputs and outputs
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive strength (DS)

Table 1: Configuration Addressing

Architecture	32 Meg x 16	16 Meg x 32	16 Meg x 32 Reduced Page-Size Option[1]
Number of banks	4	4	4
Bank address balls	BA0, BA1	BA0, BA1	BA0, BA1
Row address balls	A[12:0]	A[12:0]	A[13:0]
Column address balls	A[9:0]	A[8:0]	A[7:0]

Table 2: Key Timing Parameters
CL = CAS (READ) latency

Speed Grade	Clock Rate (MHz)		Access Time	
	CL = 2	CL = 3	CL = 2	CL = 3
-6	104	166	8ns	5ns
-75	104	133	8ns	5.4ns

Options	Marking
• Vdd/Vddq	
– 1.8V/1.8V	H
• Row size option	
– Standard addressing option	LF
– Reduced page-size option	LG[1]
• Configuration	
– 32 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
– 16 Meg x 32 (4 Meg x 32 x 4 banks)	16M32
• Plastic “green” packages	
– 54-ball VFBGA (8mm x 9mm)	BF[2]
– 90-ball VFBGA (10mm x 13mm)	CM[3]
• Timing – cycle time	
– 6ns at CL = 3	-6
– 7.5ns at CL = 3	-75
• Power	
– Standard Idd2/Idd7	None
– Low-power Idd2/Idd7	L[1]
• Operating temperature range	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
• Design revision	:B

Notes: 1. Contact factory for availability.
2. Only available for x16 configuration.
3. Only available for x32 configuration.

Products and specifications discussed herein are subject to change by Micron without notice.

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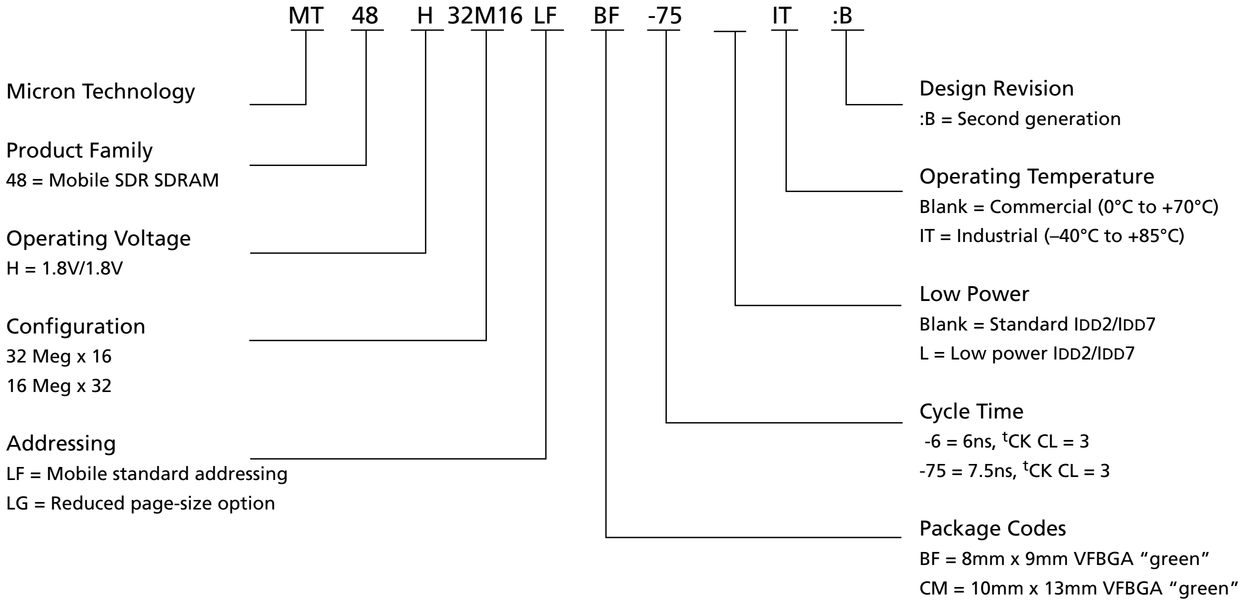
Figure 1: 512Mb Mobile LPSDR Part Numbering


MT 48 H 32M16 LF BF -75 IT :B
Micron Technology
Product Family
48 = Mobile SDR SDRAM
Operating Voltage
H = 1.8V/1.8V
Configuration
32 Meg x 16
16 Meg x 32
Addressing
LF = Mobile standard addressing
LG = Reduced page-size option
Design Revision
:B = Second generation
Operating Temperature
Blank = Commercial (0°C to +70°C)
IT = Industrial (–40°C to +85°C)
Low Power
Blank = Standard IDD2/IDD7
L = Low power IDD2/IDD7
Cycle Time
-6 = 6ns, tCK CL = 3
-75 = 7.5ns, tCK CL = 3
Package Codes
BF = 8mm x 9mm VFBGA "green"
CM = 10mm x 13mm VFBGA "green"

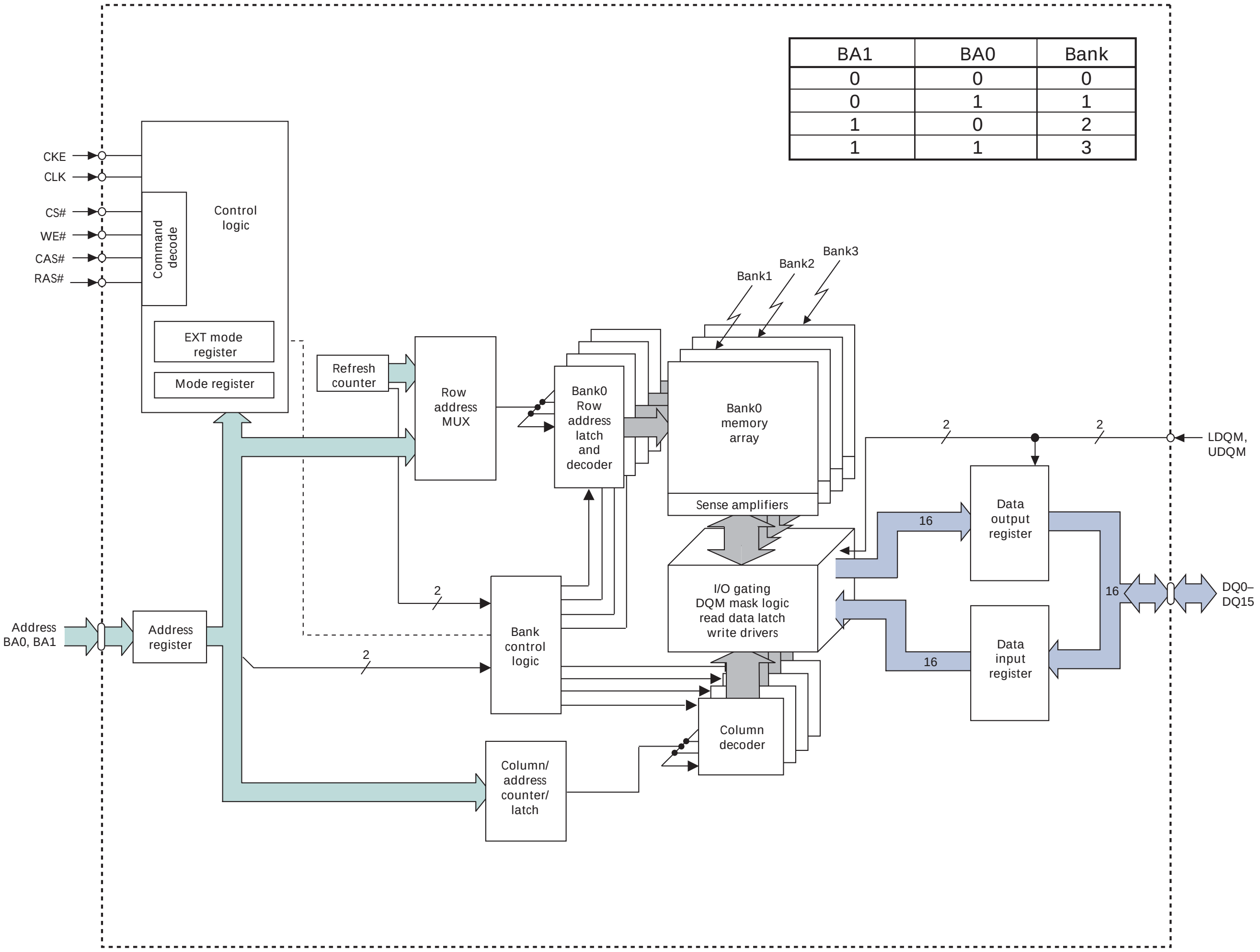
General Description

The Micron® 512Mb Mobile LPSDR is a high-speed CMOS, dynamic random-access memory containing 536,870,912-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 134,217,728-bit banks is organized as 8192 rows by 1K columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8192 rows by 512 columns by 32 bits. In a reduced page-size option, each of the x32's 134,217,728-bit banks is organized as 16,384 rows by 256 columns x32 bits.

Mobile LPSDR offers substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Functional Block Diagrams

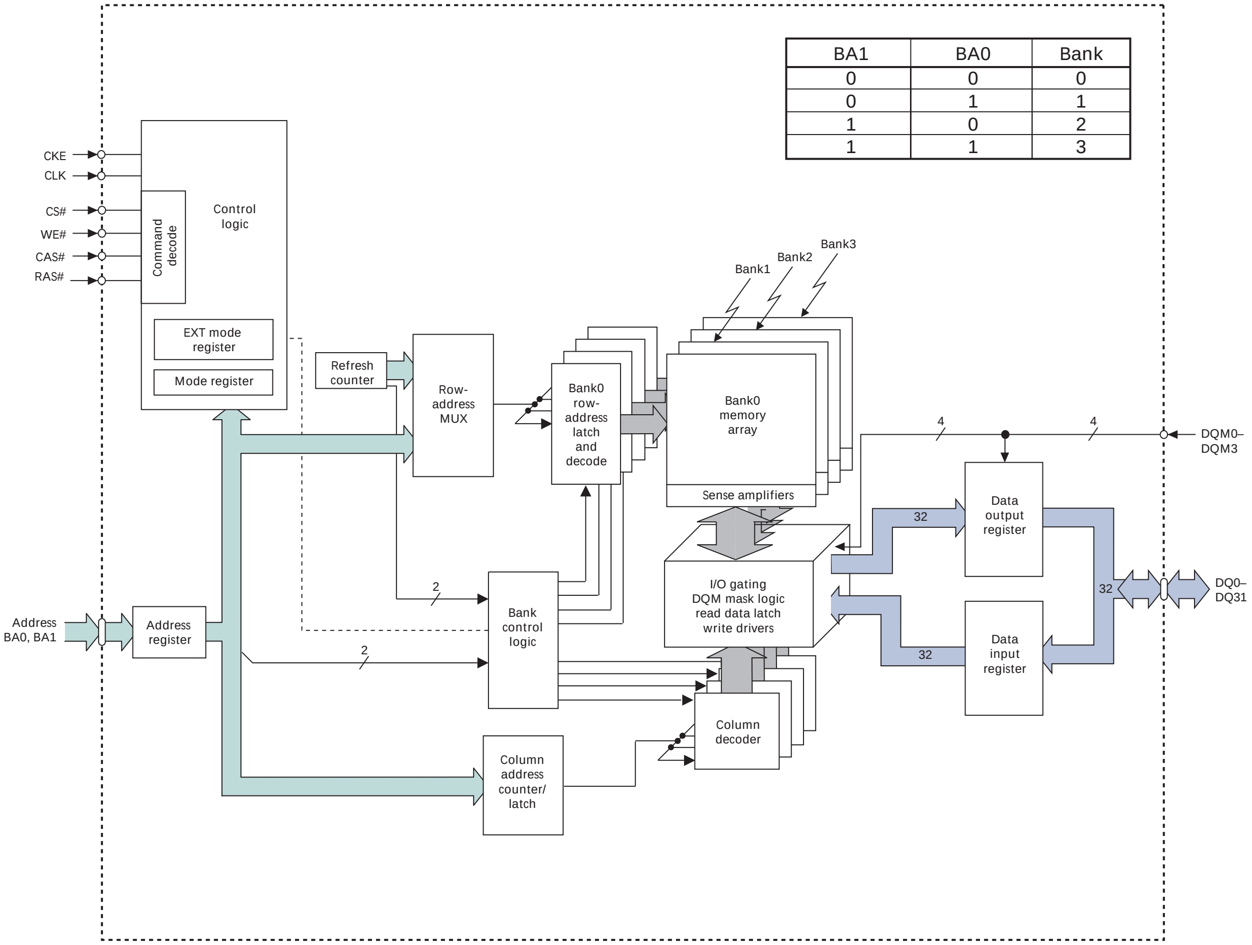
Figure 2: 32 Meg x 16 SDRAM



BA1	BA0	Bank
0	0	0
0	1	1
1	0	2
1	1	3

CKE
CLK
CS#
WE#
CAS#
RAS#
Command decode
Control logic
EXT mode register
Mode register
Refresh counter
Row address MUX
Bank0 Row address latch and decoder
Bank1
Bank2
Bank3
Bank0 memory array
Sense amplifiers
I/O gating DQM mask logic read data latch write drivers
Data output register
Data input register
LDQM, UDQM
DQ0–DQ15
2
2
16
16
16
2
2
Address BA0, BA1
Address register
Bank control logic
Column/ address counter/ latch
Column decoder

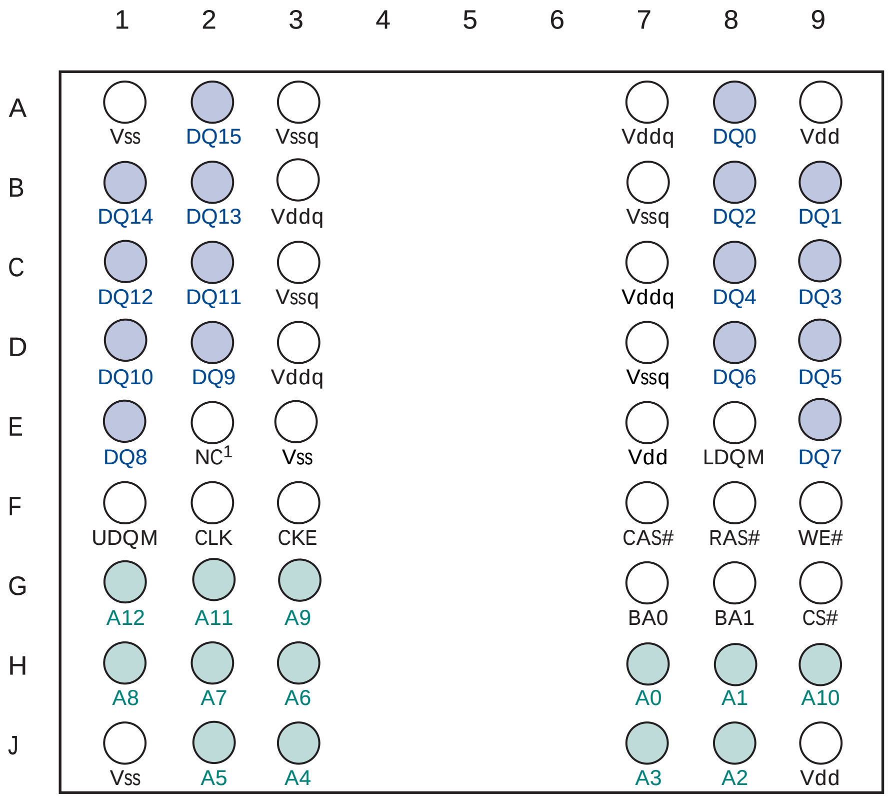
Figure 3: 16 Meg x 32 SDRAM


CKE
CLK
CS#
WE#
CAS#
RAS#
Command decode
Control logic
EXT mode register
Mode register
Refresh counter
Row-address MUX
Bank0 row-address latch and decode
Bank1
Bank2
Bank3
Bank0 memory array
Sense amplifiers
I/O gating DQM mask logic read data latch write drivers
Data output register
Data input register
DQM0–DQM3
DQ0–DQ31
4
4
32
32
32
2
2
Bank control logic
Address BA0, BA1
Address register
Column address counter/ latch
Column decoder

BA1	BA0	Bank
0	0	0
0	1	1
1	0	2
1	1	3

Ball Assignments

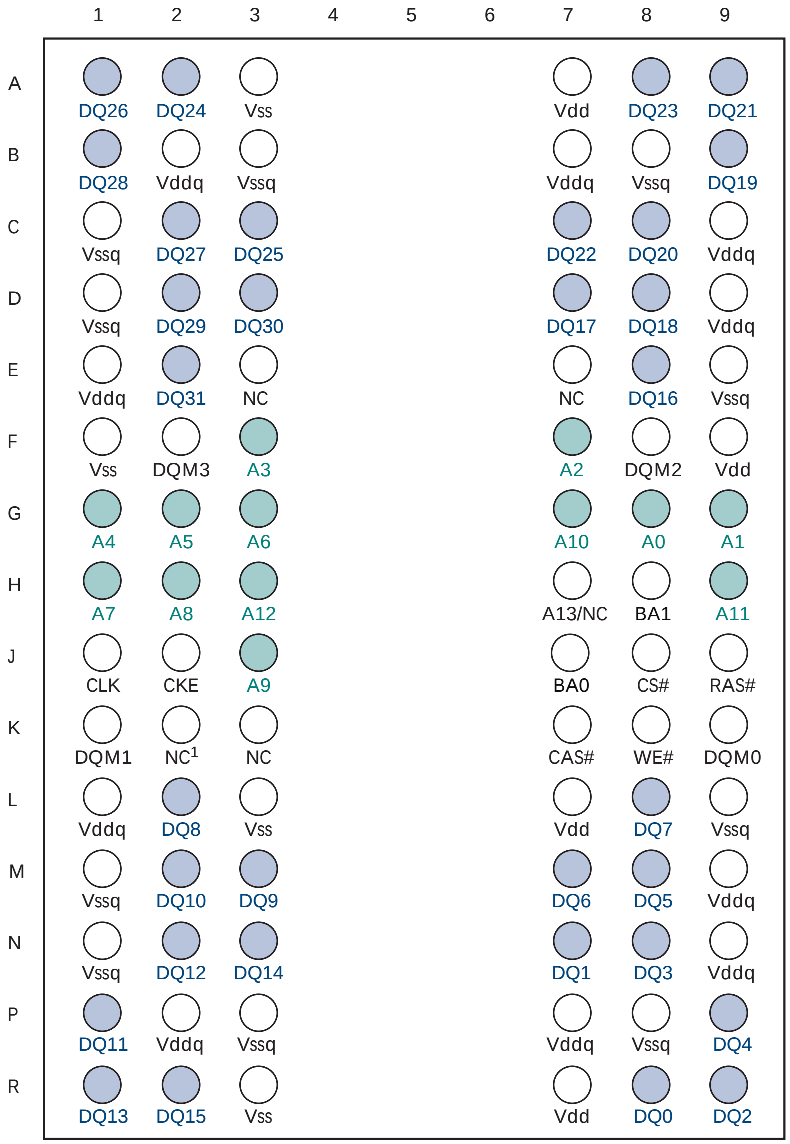
Figure 4: 54-Ball VFBGA (Top View)



	1	2	3	4	5	6	7	8	9
A	Vss	DQ15	Vssq				Vddq	DQ0	Vdd
B	DQ14	DQ13	Vddq				Vssq	DQ2	DQ1
C	DQ12	DQ11	Vssq				Vddq	DQ4	DQ3
D	DQ10	DQ9	Vddq				Vssq	DQ6	DQ5
E	DQ8	NC[1]	Vss				Vdd	LDQM	DQ7
F	UDQM	CLK	CKE				CAS#	RAS#	WE#
G	A12	A11	A9				BA0	BA1	CS#
H	A8	A7	A6				A0	A1	A10
J	Vss	A5	A4				A3	A2	Vdd

Notes: 1. The E2 pin must be connected to Vss, Vssq, or left floating.

Figure 5: 90-Ball VFBGA (Top View)



	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	Vss				Vdd	DQ23	DQ21
B	DQ28	Vddq	Vssq				Vddq	Vssq	DQ19
C	Vssq	DQ27	DQ25				DQ22	DQ20	Vddq
D	Vssq	DQ29	DQ30				DQ17	DQ18	Vddq
E	Vddq	DQ31	NC				NC	DQ16	Vssq
F	Vss	DQM3	A3				A2	DQM2	Vdd
G	A4	A5	A6				A10	A0	A1
H	A7	A8	A12				A13/NC	BA1	A11
J	CLK	CKE	A9				BA0	CS#	RAS#
K	DQM1	NC[1]	NC				CAS#	WE#	DQM0
L	Vddq	DQ8	Vss				Vdd	DQ7	Vssq
M	Vssq	DQ10	DQ9				DQ6	DQ5	Vddq
N	Vssq	DQ12	DQ14				DQ1	DQ3	Vddq
P	DQ11	Vddq	Vssq				Vddq	Vssq	DQ4
R	DQ13	DQ15	Vss				Vdd	DQ0	DQ2

Notes: 1. The K2 pin must be connected to Vss, Vssq, or left floating.

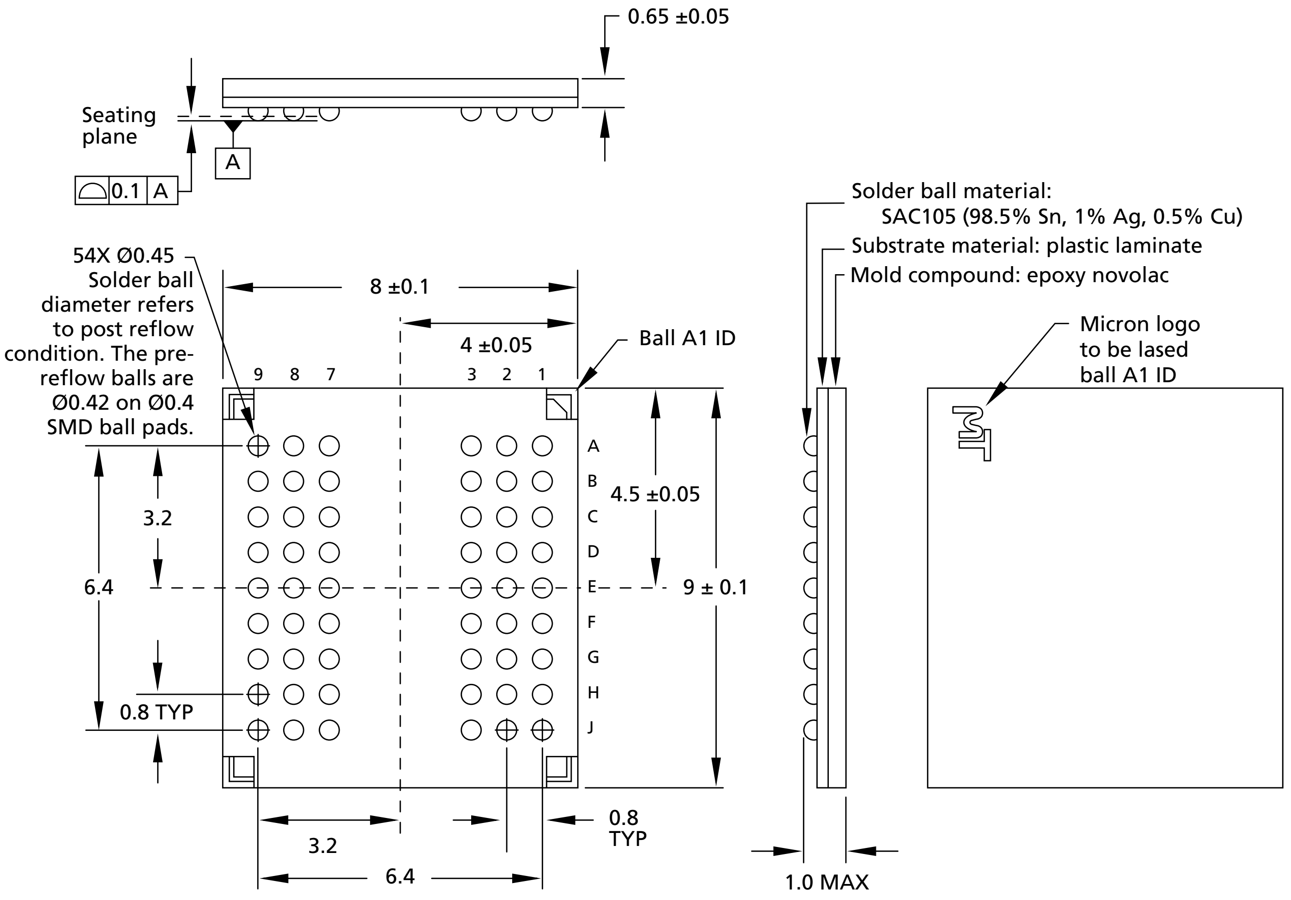
Ball Descriptions

Table 3: VFBGA Ball Descriptions

Symbol	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), deep power-down (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power.
CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
DQM[3:0] LDQM, UDQM	Input	Input/Output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. For the x16, LDQM corresponds to DQ[7:0] and UDQM corresponds to DQ[16:8]. For the x32, DQM0 corresponds to DQ[7:0], DQM1 corresponds to DQ[15:8], DQM2 corresponds to DQ[23:16], and DQM3 corresponds to DQ[31:24]. DQM[3:0] (or LDQM and UDQM if x16) are considered same state when referenced as DQM.
BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 become when registering an ALL BANK PRECHARGE (A10 HIGH).
A[12:0]	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row-address A[12:0]) and READ/WRITE command [column-address A[8:0] (x32); column-address A[9:0] (x16); with A10 defining auto precharge] to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LOAD MODE REGISTER command.
A13/NC	Input	H7 is used for the LG, reduced page-size, option (see Table 1 on page 1); otherwise, leave as NC.
DQ[31:0]	I/O	Data input/output: Data bus.
Vddq	Supply	DQ power: Provide isolated power to DQ for improved noise immunity.
Vssq	Supply	DQ ground: Provide isolated ground to DQ for improved noise immunity.
Vdd	Supply	Core power supply.
Vss	Supply	Ground.
NC	–	Ball E2 on the 54 ball and K2 on the 90 ball must be connected to Vss, Vssq, or left floating.
NC	–	Internally not connected. These balls can be left unconnected but it is recommended that they be connected to Vss.

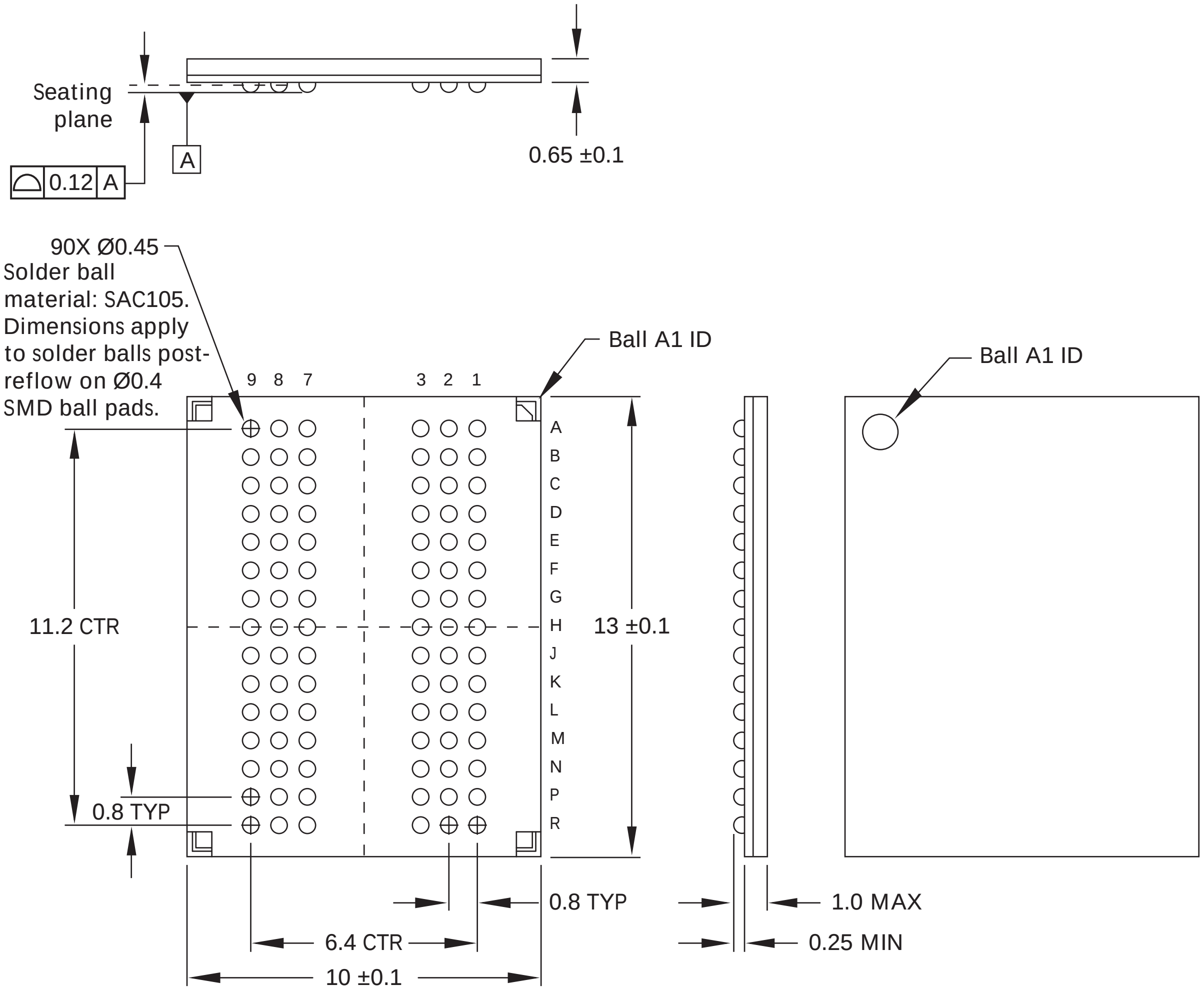
Package Dimensions

Figure 6: 54-Ball VFBGA (8mm x 9mm)


0.65 ±0.05
Seating plane
A
0.1 A
54X Ø0.45 Solder ball diameter refers to post reflow condition. The pre-reflow balls are Ø0.42 on Ø0.4 SMD ball pads.
8 ±0.1
4 ±0.05
Ball A1 ID
9 8 7 3 2 1
A B C D E F G H J
4.5 ±0.05
9 ± 0.1
3.2
6.4
0.8 TYP
3.2
6.4
0.8 TYP
Solder ball material: SAC105 (98.5% Sn, 1% Ag, 0.5% Cu)
Substrate material: plastic laminate
Mold compound: epoxy novolac
Micron logo to be lased ball A1 ID
1.0 MAX

Notes: 1. All dimensions are in millimeters.

Figure 7: 90-Ball VFBGA (10mm x 13mm)


Seating plane
0.12 A
A
0.65 ±0.1
90X Ø0.45 Solder ball material: SAC105. Dimensions apply to solder balls post-reflow on Ø0.4 SMD ball pads.
Ball A1 ID
Ball A1 ID
9 8 7
3 2 1
A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
11.2 CTR
13 ±0.1
0.8 TYP
0.8 TYP
6.4 CTR
10 ±0.1
1.0 MAX
0.25 MIN

Notes: 1. All dimensions are in millimeters.

Electrical Specifications

Absolute Maximum Ratings

Stresses greater than those listed in Table 4 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 4: Absolute Maximum Ratings

Voltage/Temperature	Symbol	Min	Max	Units
Voltage on Vdd/Vddq supply relative to Vss[1]	VDD/Vddq	–0.5	+2.4	V
Voltage on inputs, NC or I/O balls relative to Vss	Vin	–0.5	+2.4	
Storage temperature plastic	T_{STG}	–55	+150	°C

Notes: 1. Vdd and Vddq must be within 300mV of each other at all times. Vddq must not exceed Vdd.

Table 5: DC Electrical Characteristics and Operating Conditions

Notes: 1 and 2 apply to all parameters and conditions; Vdd/Vddq = 1.7–1.95V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply voltage	Vdd	1.7	1.95	V	
I/O supply voltage	Vddq	1.7	1.95	V	
Input high voltage: Logic 1; All inputs	VIH	0.8 × Vddq	Vddq + 0.3	V	3
Input low voltage: Logic 0; All inputs	Vil	–0.3	+0.3	V	3
Output high voltage	Voh	0.9 × VDDQ	–	V	4
Output low voltage	Vol	–	0.2	V	4
Input leakage current: Any input 0V ≤ Vin ≤ VDD (All other balls not under test = 0V)	II	–1.0	1.0	µA	
Output leakage current: DQ are disabled; 0V ≤ Vout ≤ VDDQ	Ioz	–1.5	1.5	µA	
Operating temperature: Commercial Industrial	T_A T_A	0 –40	+70 +85	°C	

Notes:
1. All voltages referenced to Vss.
2. A full initialization sequence is required before proper device operation is ensured
3. Vih overshoot: Vih (MAX) = Vddq + 2V for a pulse width ≤3ns, and the pulse width cannot be greater than one third of the cycle rate. Vil undershoot: Vil (MIN) = –2V for a pulse width ≤3ns.
4. Iout = 4mA for full drive strength. Other drive strengths require appropriate scale.

Table 6: Capacitance

Note 1 applies to all parameters and conditions

Parameter	Symbol	Min	Max	Units
Input capacitance: CLK	CI1	2.0	5.0	pF
Input capacitance: All other input-only balls	CI2	2.0	5.0	pF
Input/output capacitance: DQ	CIO	2.5	6.0	pF

Notes: 1. This parameter is sampled. Vdd, Vddq = +1.8V; T_A = 25°C; ball under test biased at 0.9V, f = 1 MHz.

Table 7: **Idd Specifications and Conditions (x16)**
Note 1 applies to all parameters and conditions; notes appear on page 15; Vdd/Vddq = 1.70–1.95V

Parameter/Condition		Symbol	Max		Units	Notes
			-6	-75		
Operating current: Active mode; Burst = 1; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		Idd1	90	80	mA	2, 3, 4
Standby current: Power-down mode; All banks idle; CKE = LOW		Idd2P	300	300	µA	5
Standby current: Non-power-down mode; All banks idle; CKE = HIGH		Idd2N	10	8	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		Idd3P	5	5	mA	3, 4, 6
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		Idd3N	20	18	mA	3, 4, 6
Operating current: Burst mode; READ or WRITE; All banks active, half DQ toggling every cycle		Idd4	100	90	mA	2, 3, 4
Auto refresh current CKE = HIGH; CS# = HIGH	^{t}RFC = 110ns	Idd5	100	100	mA	2, 3, 4, 6
	^{t}RFC = 7.8125µs	Idd6	3	3	mA	2, 3, 4, 7
Deep power-down		Izz	10	10	µA	5, 8

Table 8: **Idd Specifications and Conditions (x32)**
Note 1 applies to all parameters and conditions; notes appear on page 15; Vdd/Vddq = 1.70–1.95V

Parameter/Condition		Symbol	Max		Units	Notes
			-6	-75		
Operating current: Active mode; Burst = 1; READ or WRITE; ^{t}RC = ^{t}RC (MIN)		Idd1	90	80	mA	2, 3, 4
Standby current: Power-down mode; All banks idle; CKE = LOW		Idd2P	300	300	µA	5
Standby current: Non-power-down mode; All banks idle; CKE = HIGH		Idd2N	10	8	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress		Idd3P	5	5	mA	3, 4, 6
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after ^{t}RCD met; No accesses in progress		Idd3N	20	18	mA	3, 4, 6
Operating current: Burst mode; READ or WRITE; All banks active, half DQ toggling every cycle		Idd4	105	95	mA	2, 3, 4
Auto refresh current CKE = HIGH; CS# = HIGH	^{t}RFC = 110ns	Idd5	100	100	mA	2, 3, 4, 6
	^{t}RFC = 7.8125µs	Idd6	3	3	mA	2, 3, 4, 7
Deep power-down		Izz	10	10	µA	5, 8

Table 9: **Idd7 Specifications and Conditions (x16 and x32)**
Notes: 1, 5, 9, and 10 apply to all conditions and parameters; Vdd/Vddq = 1.70–1.95V

Parameter/Condition		Symbol	Low Power	Standard	Units
Self refresh CKE = LOW; ^tCK = ^tCK (MIN); Address and control inputs are stable; Data bus inputs are stable.	Full array, 85°C	IDD7	500	700	µA
	Full array, 45°C		250	390	µA
	Half array, 85°C		400	520	µA
	Half array, 45°C		220	310	µA
	1/4 array, 85°C		350	430	µA
	1/4 array, 45°C		205	275	µA
	1/8 array, 85°C		350	430	µA
	1/8 array, 45°C		205	275	µA
	1/16 array, 85°C		325	375	µA
	1/16 array, 45°C		200	250	µA

Notes:
1. A full initialization sequence is required before proper device operation is ensured.
2. Idd is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
3. The Idd current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every two clocks.
5. Measurement is taken 500ms after entering into this operating mode to allow tester measuring unit settling time.
6. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid Vih or Vil levels.
7. CKE is HIGH during REFRESH command period ^tRFC else CKE is LOW.
8. Typical values at 25°C (not a maximum value).
9. Enables on-die refresh and address counters.
10. Values for Idd7 85°C full array and partial array are guaranteed for the entire temperature range. All other Idd7 values are estimated.

Figure 8: **Typical IDD7 Curves**

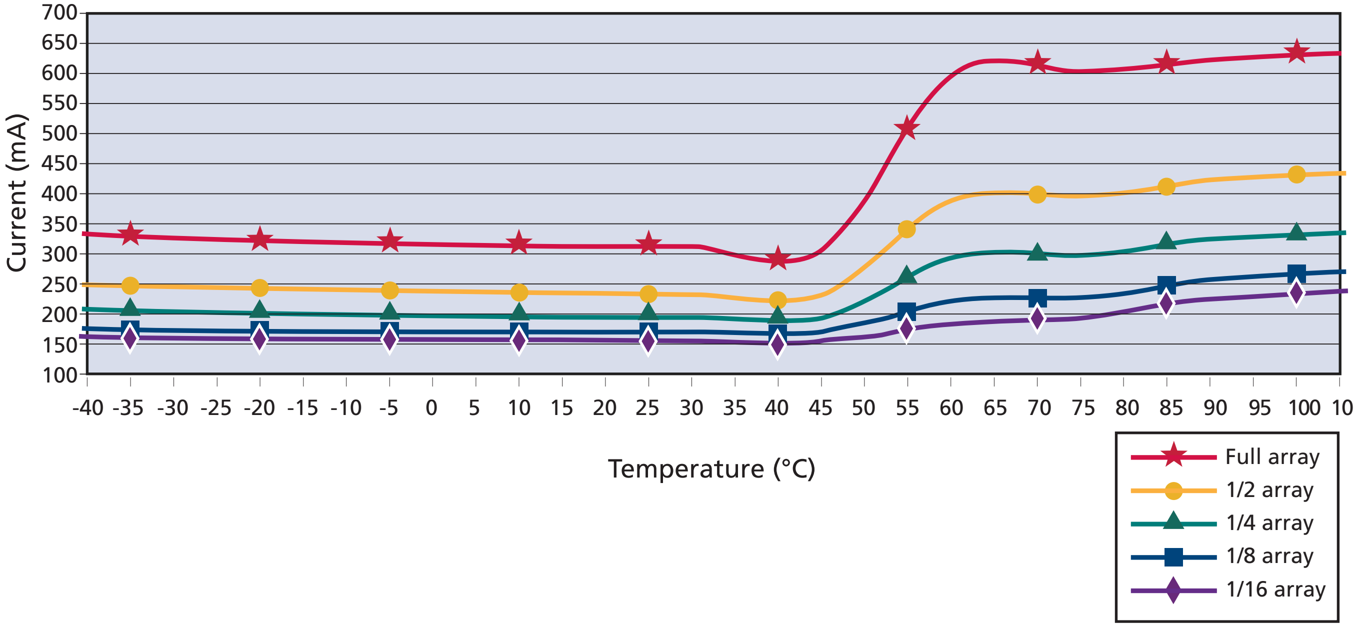


Table 10: Electrical Characteristics and Recommended AC Operating Conditions

Notes 1–5 apply to all parameters; notes begin below Table 11 on page 17

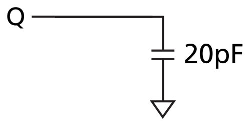
AC Characteristics		Symbol	-6		-75		Unit	Notes
Parameter			**Min**	**Max**	**Min**	**Max**		
Access time from CLK (positive edge)	CL = 3	^{t}AC	–	5	–	5.4	ns	
	CL = 2		–	8	–	8		
Address hold time		^{t}AH	1	–	1	–	ns	
Address setup time		^{t}AS	1.5	–	1.5	–	ns	
CLK high-level width		^{t}CH	2.5	–	2.5	–	ns	
CLK low-level width		^{t}CL	2.5	–	2.5	–	ns	
Clock cycle time	CL = 3	^{t}CK	6	–	7.5	–	ns	6
	CL = 2		9.6	–	9.6	–		
CKE hold time		^{t}CKH	1	–	1	–	ns	
CKE setup time		^{t}CKS	1.5	–	1.5	–	ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^{t}CMH	1	–	1	–	ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^{t}CMS	1.5	–	1.5	–	ns	
Data-in hold time		^{t}DH	1	–	1	–	ns	
Data-in setup time		^{t}DS	1.5	–	1.5	–	ns	
Data-out High-Z time	CL = 3	^{t}HZ	–	5	–	5.4	ns	7
	CL = 2		–	8	–	8	ns	
Data-out Low-Z time		^{t}LZ	1	–	1	–	ns	
Data-out hold time (load)		^{t}OH	2.5	–	2.5	–	ns	
Data-out hold time (no load)		^{t}OHn	1.8	–	1.8	–	ns	
ACTIVE-to-PRECHARGE command		^{t}RAS	42	120,000	45	120,000	ns	
ACTIVE-to-ACTIVE command period		^{t}RC	60	–	67.5	–	ns	
ACTIVE-to-READ or WRITE delay		^{t}RCD	18	–	19.2	–	ns	
Refresh period (8192 rows)		^{t}REF	–	64	–	64	ms	8
AUTO REFRESH period		^{t}RFC	97.5	–	97.5	–	ns	
PRECHARGE command period		^{t}RP	18	–	19.2	–	ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	2	–	2	–	^{t}CK	
Transition time		^{t}T	0.3	1.2	0.3	1.2	ns	9
WRITE recovery time		^{t}WR	15	–	15	–	ns	10
Exit SELF REFRESH-to-ACTIVE command		^{t}XSR	120	–	120	–	ns	11

Table 11: AC Functional Characteristics

Notes 1–5 apply to all parameters

Parameter		Symbol	-6	-75	Units	Notes
Last data-in to burst STOP command		^{t}BDL	1	1	^{t}CK	12
READ/WRITE command to READ/WRITE command		^{t}CCD	1	1	^{t}CK	12
Last data-in to new READ/WRITE command		^{t}CDL	1	1	^{t}CK	13
CKE to clock disable or power-down entry mode		^{t}CKED	1	1	^{t}CK	13
Data-in to ACTIVE command		^{t}DAL	5	5	^{t}CK	14, 16
Data-in to PRECHARGE command		^{t}DPL	2	2	^{t}CK	15, 16
DQM to input data delay		^{t}DQD	0	0	^{t}CK	12
DQM to data mask during WRITEs		^{t}DQM	0	0	^{t}CK	12
DQM to data High-Z during READs		^{t}DQZ	2	2	^{t}CK	12
WRITE command to input data delay		^{t}DWD	0	0	^{t}CK	12
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^{t}MRD	2	2	^{t}CK	
CKE to clock enable or power-down exit mode		^{t}PED	1	1	^{t}CK	13
Last data-in to PRECHARGE command		^{t}RDL	2	2	^{t}CK	15, 16
Data-out High-Z from PRECHARGE command	CL = 3	^{t}ROH	3	3	^{t}CK	12
	CL = 2		2	2	^{t}CK	

Notes:
1. A full initialization sequence is required before proper device operation is ensured.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ +70°C standard temperature and –40°C ≤ T_A ≤ +85°C industrial temperature) is ensured.
3. In addition to meeting the transition rate specification, the clock and CKE must transit between Vih and Vil (or between Vil and Vih) in a monotonic manner.
4. Outputs measured for 1.8V at 0.9V with equivalent load:



Test loads with full DQ driver strength. Performance will vary with actual system DQ bus capacitive loading, termination, and programmed drive strength.

5. AC timing tests have Vil and Vih with timing referenced to Vih/2 = crossover point. If the input transition time is longer than ^{t}T (MAX), then the timing is referenced at Vil (MAX) and Vih (MIN) and no longer at the Vih/2 crossover point.
6. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) during access or precharge states (READ, WRITE, including ^{t}WR, and PRECHARGE commands). CKE may be used to reduce the data rate.
7. ^{t}HZ defines the time at which the output achieves the open circuit condition, it is not a reference to Voh or Vol. The last valid data element will meet ^{t}OH before going High-Z.
8. The 512Mb Mobile LPSDR requires 8192 AUTO REFRESH cycles every 64ms (^{t}REF). Providing a distributed AUTO REFRESH command every 7.8125µs meets the refresh requirement and ensures that each row is refreshed. Alternatively, 8192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RFC), once every 64ms.
9. AC characteristics assume ^{t}T = 1ns.
10. Auto precharge mode only. The precharge timing budget (^{t}RP) begins at *x* ns for -75 after the first clock delay and after the last WRITE is executed. May not exceed the limit set for precharge mode.
11. CLK must be toggled a minimum of two times during this period.

12. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
13. Timing is specified by ^{t}CKS. Clock(s) specified as a reference only at minimum cycle rate.
14. Timing is specified by ^{t}WR plus ^{t}RP. Clock(s) specified as a reference only at minimum cycle rate.
15. Timing is specified by ^{t}WR.
16. Based on ^{t}CK (MIN), CL = 3.

Table 12: Target Output Drive Characteristics (Full Strength)

Notes 1–2 apply to all values. Characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.80	18.53	–2.80	–18.53
0.20	5.60	26.80	–5.60	–26.80
0.30	8.40	32.80	–8.40	–32.80
0.40	11.20	37.05	–11.20	–37.05
0.50	14.00	40.00	–14.00	–40.00
0.60	16.80	42.50	–16.80	–42.50
0.70	19.60	44.57	–19.60	–44.57
0.80	22.40	46.50	–22.40	–46.50
0.85	23.80	47.48	–23.80	–47.48
0.90	23.80	48.50	–23.80	–48.50
0.95	23.80	49.40	–23.80	–49.40
1.00	23.80	50.05	–23.80	–50.05
1.10	23.80	51.35	–23.80	–51.35
1.20	23.80	52.65	–23.80	–52.65
1.30	23.80	53.95	–23.80	–53.95
1.40	23.80	55.25	–23.80	–55.25
1.50	23.80	56.55	–23.80	–56.55
1.60	23.80	57.85	–23.80	–57.85
1.70	23.80	59.15	–23.80	–59.15
1.80	–	60.45	–	–60.45
1.90	–	61.75	–	–61.75

Notes:
1. Table values based on nominal impedance of 25Ω (full drive strength) at Vddq/2.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.

Table 13: Target Output Drive Characteristics (Three-Quarter Strength)

Notes 1–3 apply to all values. Characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.96	12.97	–1.96	–12.97
0.20	3.92	18.76	–3.92	–18.76
0.30	5.88	22.96	–5.88	–22.96
0.40	7.84	25.94	–7.84	–25.94
0.50	9.80	28.00	–9.80	–28.00
0.60	11.76	29.75	–11.76	–29.75
0.70	13.72	31.20	–13.72	–31.20
0.80	15.68	32.55	–15.68	–32.55
0.85	16.66	33.24	–16.66	–33.24
0.90	16.66	33.95	–16.66	–33.95
0.95	16.66	34.58	–16.66	–34.58
1.00	16.66	35.04	–16.66	–35.04
1.10	16.66	35.95	–16.66	–35.95
1.20	16.66	36.86	–16.66	–36.86
1.30	16.66	37.77	–16.66	–37.77
1.40	16.66	38.68	–16.66	–38.68
1.50	16.66	39.59	–16.66	–39.59
1.60	16.66	40.50	–16.66	–40.50
1.70	16.66	41.41	–16.66	–41.41
1.80	–	42.32	–	–42.32
1.90	–	43.23	–	–43.23

Notes:
1. Table values based on nominal impedance of 37Ω (three-quarter drive strength) at Vddq/2.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.

Table 14: Target Output Drive Characteristics (One-Half Strength)

Notes 1–2 apply to all values. Characteristics are specified under best and worst process variations/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	–1.27	–8.42
0.20	2.55	12.30	–2.55	–12.30
0.30	3.82	14.95	–3.82	–14.95
0.40	5.09	16.84	–5.09	–16.84
0.50	6.36	18.20	–6.36	–18.20
0.60	7.64	19.30	–7.64	–19.30
0.70	8.91	20.30	–8.91	–20.30
0.80	10.16	21.20	–10.16	–21.20
0.85	10.80	21.60	–10.80	–21.60
0.90	10.80	22.00	–10.80	–22.00
0.95	10.80	22.45	–10.80	–22.45
1.00	10.80	22.73	–10.80	–22.73
1.10	10.80	23.21	–10.80	–23.21
1.20	10.80	23.67	–10.80	–23.67
1.30	10.80	24.14	–10.80	–24.14
1.40	10.80	24.61	–10.80	–24.61
1.50	10.80	25.08	–10.80	–25.08
1.60	10.80	25.54	–10.80	–25.54
1.70	10.80	26.01	–10.80	–26.01
1.80	–	26.48	–	–26.48
1.90	–	26.95	–	–26.95

Notes:
1. Table values based on nominal impedance of 55Ω (half drive strength) at Vddq/2.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.
3. The I-V curve for one-quarter drive strength is approximately 50% of one-half drive strength.

Functional Description

Mobile LPSDR devices are quad-bank DRAM that operate at 1.8V and include a synchronous interface. All signals are registered on the positive edge of the clock signal, CLK.

Read and write accesses to SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, that is followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Mobile LPSDR provides for programmable READ or WRITE burst lengths. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

Mobile LPSDR uses an internal pipelined architecture to achieve high-speed operation. This architecture enables changing the column address on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

Mobile LPSDR is designed to operate in 1.8V memory systems. An auto refresh mode is provided, along with power-saving, power-down, and deep power-down modes. All inputs and outputs are LVTTL-compatible.

Mobile LPSDR offers substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

Commands

Table 15 provides a quick reference of available commands. A written description of each command follows the table. Three additional Truth Tables appear on pages 28–32; these tables provide current state/next state information.

Table 15: Truth Table – Commands and DQM Operation
Note 1 applies to all commands; notes appear below table

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQ	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (select bank and activate row)	L	L	H	H	X	Bank/row	X	2
READ (select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/col	X	3
WRITE (select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/col	Valid	3
BURST TERMINATE or deep power-down (enter deep power-down mode)	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	6
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	7, 8
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	9
Write enable/output enable	X	X	X	X	L	X	Active	10
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	10

Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.
2. A[0:*n*] provide row address (where A*n* is the most significant address bit), BA0 and BA1 determine which bank is made active.
3. A[0:*i*] provide column address (where *i* = the most significant column address for a given device configuration). A10 HIGH enables the auto precharge feature (non-persistent), while A10 LOW disables the auto precharge feature. BA0 and BA1 determine which bank is being read from or written to.
4. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.
5. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQ column reads a “Don’t Care” state to illustrate that the BURST TERMINATE command can occur when there is no data present.
6. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: all banks precharged and BA0, BA1 are “Don’t Care.”
7. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
8. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
9. A[11:0] define the op-code written to the mode register.
10. Activates or deactivates the DQ during WRITEs (zero-clock delay) and READs (two-clock delay).

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to a selected SDRAM (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

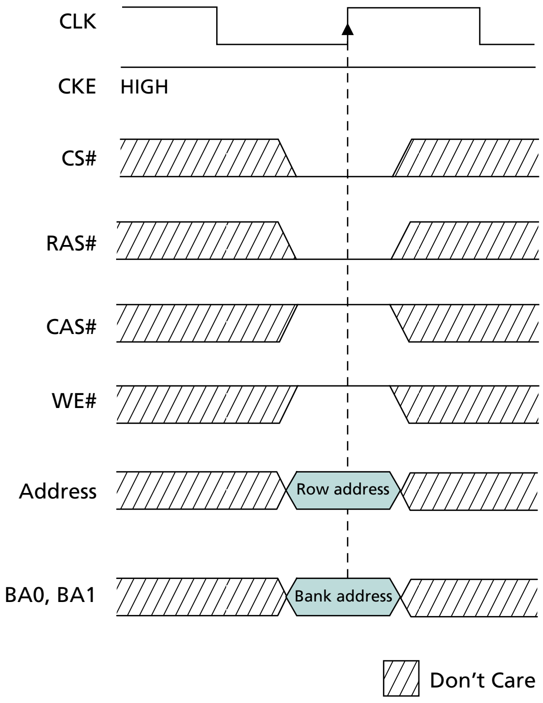
LOAD MODE REGISTER (LMR)

The mode registers are loaded via inputs A[*n:0*] (where A*n* is the most significant address term), BA0, and BA1(see "Mode Register" on page 34). The LOAD MODE REGISTER command can only be issued when all banks are idle and a subsequent executable command cannot be issued until ^tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank. Figure 9 shows the ACTIVE command.

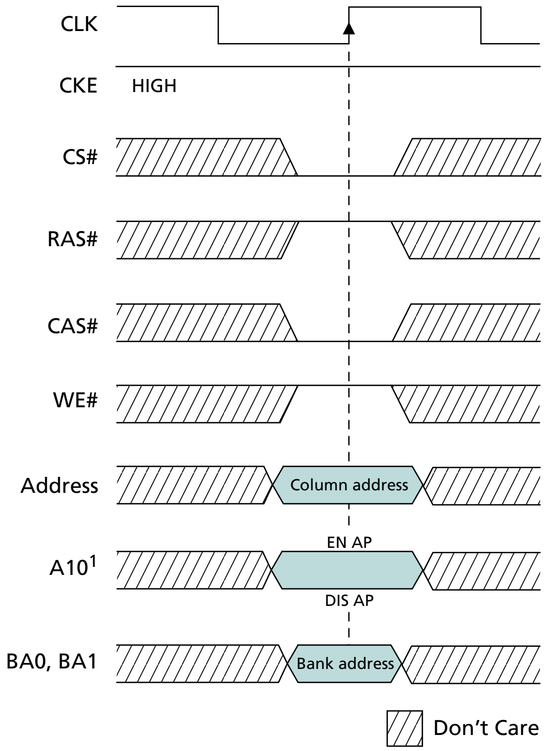
Figure 9: ACTIVE Command



READ

The READ command is used to initiate a burst read access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the READ burst; if auto precharge is not selected, the row remains open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data. Figure 10 shows the READ command.

Figure 10: READ Command

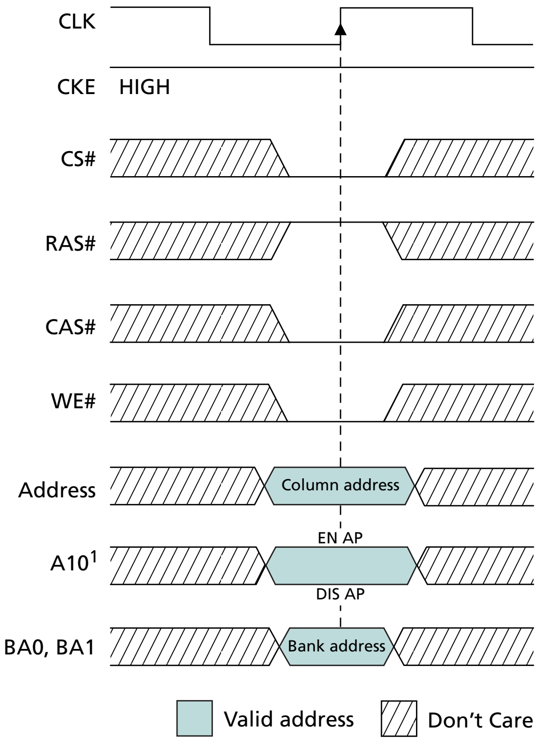


Notes: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge

WRITE

The WRITE command is used to initiate a burst write access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the write burst; if auto precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data is written to memory; if the DQM signal is registered HIGH, the corresponding data inputs are ignored and a WRITE is not executed to that byte/column location. Figure 11 shows the WRITE command.

Figure 11: WRITE Command

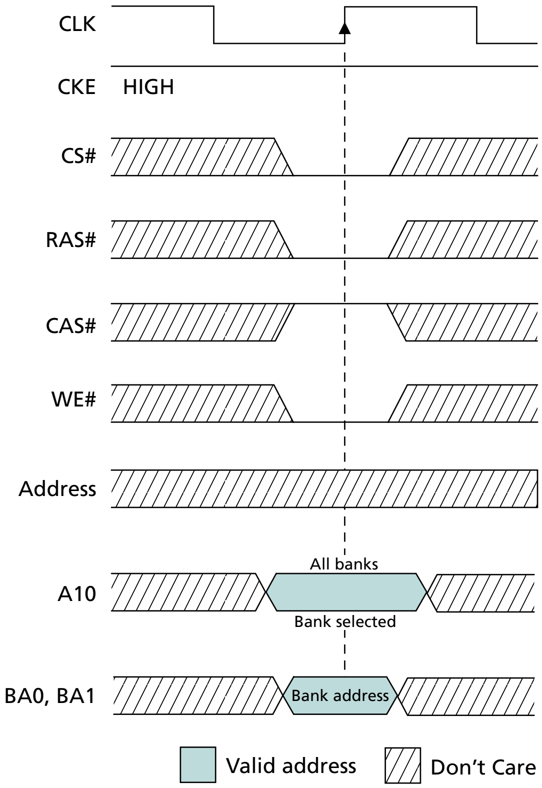

CLK
CKE HIGH
CS#
RAS#
CAS#
WE#
Address
Column address
A10¹
EN AP
DIS AP
BA0, BA1
Bank address
Valid address
Don't Care

Notes: 1. EN AP = enable auto precharge, DIS AP = disable auto precharge

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0 and BA1 select the bank. Otherwise BA0 and BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. Figure 12 on page 27 shows the PRECHARGE command.

Figure 12: PRECHARGE Command



BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or continuous page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command is truncated.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) REFRESH in FPM/EDO DRAM. Addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command.

SELF REFRESH

The SELF REFRESH command is used to place the device in self refresh mode. The self refresh mode is used to retain data in the SDRAM while the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except that CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW.

DEEP POWER-DOWN (DPD)

The DEEP POWER-DOWN (DPD) command is used to enter deep power-down mode, achieving maximum power reduction by eliminating the power to the memory array. To enter DPD, all banks must be idle. While CKE is LOW, hold CS# and WE# LOW, and hold RAS# and CAS# HIGH at the rising edge of the clock. To exit DPD, assert CKE HIGH.

Operations

Truth Tables

Table 16: Truth Table – Current State Bank *n*, Command to Bank *n*

Notes 1–6 apply to all parameters in this table; notes appear below table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	11
Row active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9, 10
Write (auto precharge disabled)	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9, 10

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Table 18 on page 32) and after ^tXSR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted; i.e., the current state is for a specific bank and the commands shown can be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:

Idle:	The bank has been precharged, and ^tRP has been met.
Row active:	A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Read:	A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
Write:	A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

4. The states listed below must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or supported commands to the other bank, should be issued on any clock edge occurring during these states. Supported commands to any

other bank are determined by the bank's current state and the conditions described in this table and in Table 17 on page 30.

Precharging:	Starts with registration of a PRECHARGE command and ends when ${}^tRP$ is met. After ${}^tRP$ is met, the bank will be in the idle state.
Row activating:	Starts with registration of an ACTIVE command and ends when ${}^tRCD$ is met. After ${}^tRCD$ is met, the bank will be in the row active state.
Read with auto precharge enabled:	Starts with registration of a READ command with auto precharge enabled and ends when ${}^tRP$ has been met. After ${}^tRP$ is met, the bank will be in the idle state.
Write with auto precharge enabled:	Starts with registration of a WRITE command with auto precharge enabled and ends when${}^tRP$ has been met. After ${}^tRP$ is met, the bank will be in the idle state.

5. The states listed below must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

Refreshing:	Starts with registration of an AUTO REFRESH command and ends when ${}^tRFC$ is met. After ${}^tRFC$ is met, the SDRAM will be in the all-banks-idle state.
Accessing mode register:	Starts with registration of a LOAD MODE REGISTER command and ends when ${}^tMRD$ has been met. After ${}^tMRD$ is met, the Mobile LPSDR will be in the all-banks-idle state.
Precharging all:	Starts with registration of a PRECHARGE ALL command and ends when ${}^tRP$ is met. After ${}^tRP$ is met, all banks will be in the idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank specific; requires that all banks are idle.
8. May or may not be bank specific; if all banks are to be precharged, each must be in a valid state for precharging.
9. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

Table 17: Truth Table – Current State Bank *n*, Command to Bank *m*

Notes 1–6 apply to all parameters in this table; notes appear below table

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any command otherwise supported for bank *m*	
Row activating, active, or precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 10
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 11
	L	L	H	L	PRECHARGE	9
Write (auto precharge disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 12
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 13
	L	L	H	L	PRECHARGE	9
Read (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 8, 14
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 8, 15
	L	L	H	L	PRECHARGE	9
Write (with auto precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8, 16
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 8, 17
	L	L	H	L	PRECHARGE	9

Notes:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (Table 18 on page 32), and after ^tXSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown can be issued to bank *m* (assuming that bank *m* is in such a state that the given command is supported). Exceptions are covered in the notes below.
3. Current state definitions:

Idle:	The bank has been precharged, and ^tRP has been met.
Row active:	A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Read:	A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
Write:	A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
Read with auto precharge enabled:	Starts with registration of a READ command with auto precharge enabled and ends when ^tRP has been met. After ^tRP is met, the bank will be in the idle state.
Write with auto precharge enabled:	Starts with registration of a WRITE command with auto precharge enabled and ends when ^tRP has been met. After ^tRP is met, the bank will be in the idle state.

4. AUTO REFRESH, SELF REFRESH, and LOAD MODE REGISTER commands can only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.

6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Concurrent auto precharge: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m* burst.
9. The burst in bank *n* continues as initiated.
10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency (CL) later.
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered.
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered.
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE bank *n* will be data-in registered one clock prior to the READ to bank *m*.
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock to the WRITE to bank *m*.

Table 18: Truth Table – CKE
Notes 1–4 apply to all parameters in this table; notes appear below table

CKE_{n-1}	CKE_n	Current State	$Command_n$	$Action_n$	Notes
L	L	Power-down	X	Maintain power-down	
		Self refresh	X	Maintain self refresh	
		Clock suspend	X	Maintain clock suspend	
		Deep power-down	X	Maintain deep power-down	
L	H	Power-down	COMMAND INHIBIT or NOP	Exit power-down	5
		Deep power-down	X	Exit deep power-down	
		Self refresh	COMMAND INHIBIT or NOP	Exit self refresh	6
		Clock suspend	X	Exit clock suspend	7
H	L	All banks idle	COMMAND INHIBIT or NOP	Power-down entry	
		All banks idle	BURST TERMINATE	Deep power-down entry	8
		All banks idle	AUTO REFRESH	Self refresh entry	
		Reading or writing	VALID	Clock suspend entry	
H	H		Table 17 on page 30		

Notes:
1. CKE_n is the logic state of CKE at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge *n* will put the device in the all-banks-idle state in time for clock edge *n* + 1 (provided that ^tCKS is met).
6. Exiting self refresh at clock edge *n* will put the device in the all-banks-idle state after ^tXSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the ^tXSR period. A minimum of two NOP commands must be provided during the ^tXSR period.
7. After exiting clock suspend at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n* + 1.
8. Deep power-down is a power-saving feature of this Mobile LPSDR device. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.

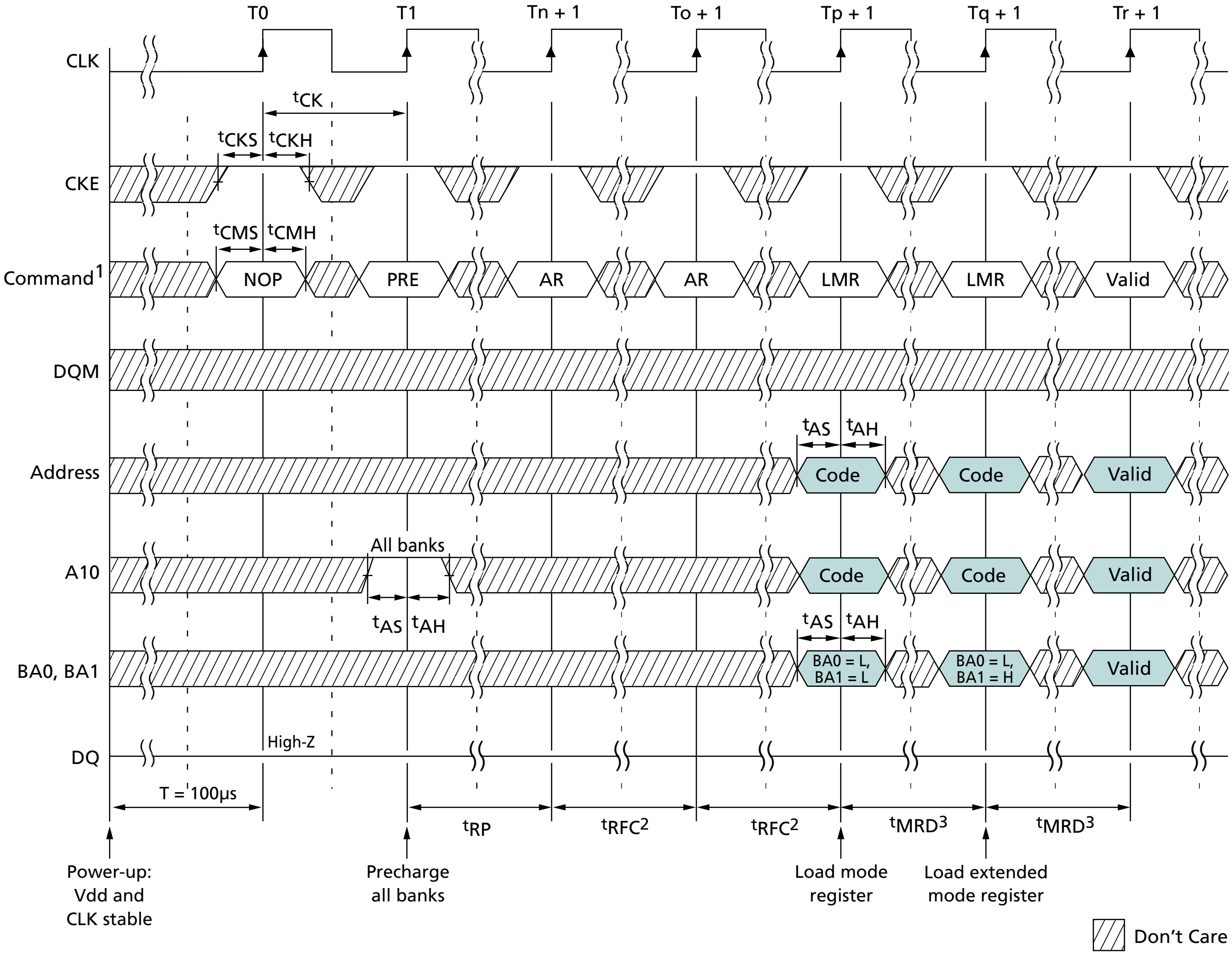
Initialization

Low-power SDRAM devices must be powered up and initialized in a predefined manner. Using initialization procedures other than those specified may result in undefined operation. After power is simultaneously applied to Vdd and Vddq and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

After the 100µs delay is satisfied by issuing at least one COMMAND INHIBIT or NOP command, a PRECHARGE command must be issued. All banks must then be precharged, which places the device in the all-banks-idle state.

When in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register powers up in an unknown state, it should be loaded prior to issuing any operational command. The low-power SDRAM initialization sequence is shown in Figure 13.

Figure 13: Initialize and Load Mode Register


T0
T1
Tn + 1
To + 1
Tp + 1
Tq + 1
Tr + 1
CLK
tCK
tCKS
tCKH
CKE
tCMS
tCMH
Command1
NOP
PRE
AR
AR
LMR
LMR
Valid
DQM
tAS
tAH
Address
Code
Code
Valid
All banks
A10
Code
Code
Valid
tAS
tAH
tAS
tAH
BA0, BA1
BA0 = L, BA1 = L
BA0 = L, BA1 = H
Valid
DQ
High-Z
T = 100µs
tRP
tRFC2
tRFC2
tMRD3
tMRD3
Power-up: Vdd and CLK stable
Precharge all banks
Load mode register
Load extended mode register
Don't Care

Notes:
1. PRE = PRECHARGE command, AR = AUTO REFRESH command, LMR = LOAD MODE REGISTER command.
2. NOPs or DESELECTs must only be provided during ^{t}RFC time.
3. NOPs or DESELECTs must only be provided during ^{t}MRD time.

Register Definition

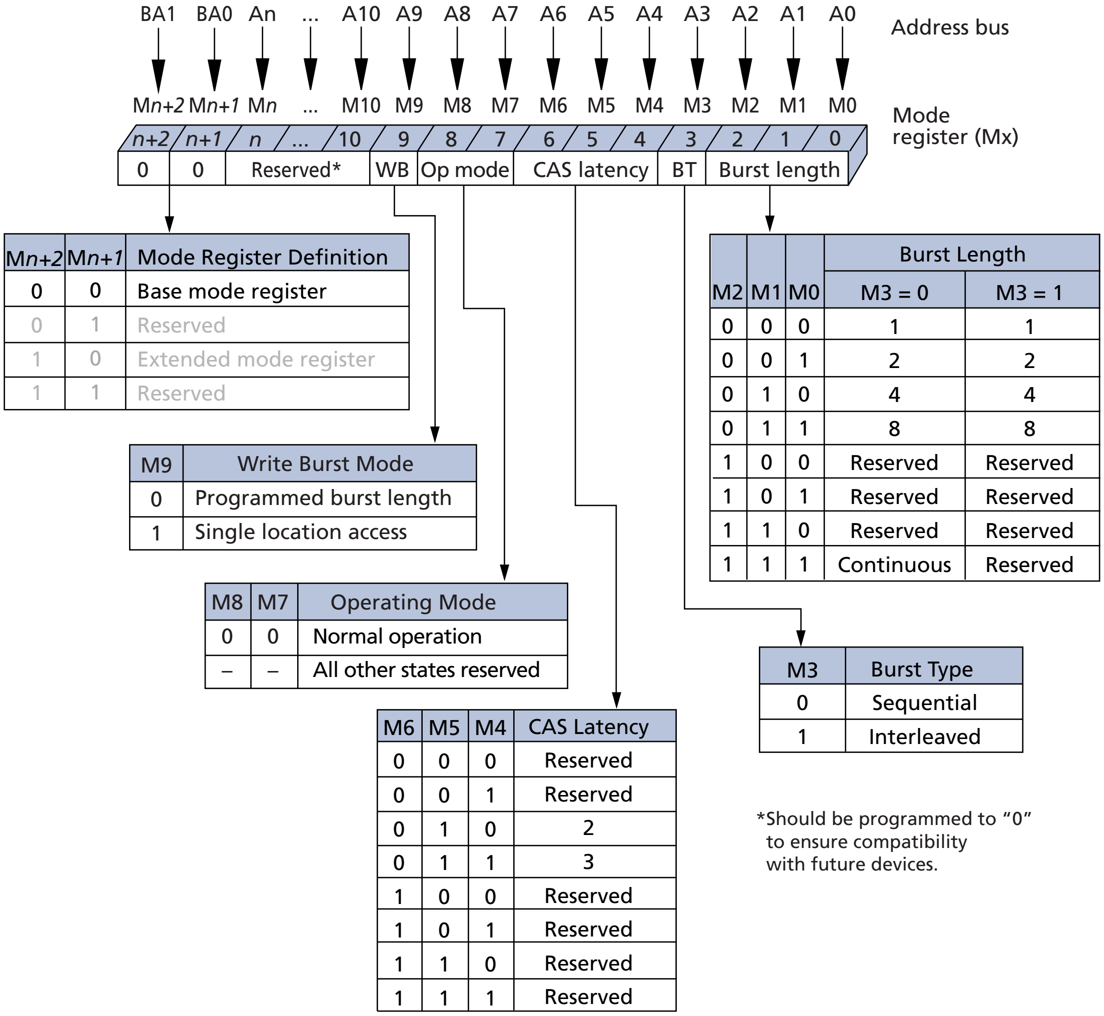
Mode Register

There are two mode registers in the Mobile LPSDR component, the mode register and the extended mode register (EMR). The mode register is illustrated in Figure 14 on page 35. The mode register defines the specific mode of operation of the Mobile LPSDR, including burst length (BL), burst type, CAS latency (CL), operating mode, and write burst mode. The mode register is programmed via the LOAD MODE REGISTER command and retains the stored information until it is programmed again or the device loses power.

Mode register bits M[2:0] specify the BL, M3 specifies the type of burst, M[6:4] specify the CL, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 through M*n* should be set to zero to ensure compatibility with future revisions. M*n* + 1 and M*n* + 2 should be set to zero to prevent the extended mode register from being programmed.

The mode registers must be loaded when all banks are idle, and the controller must wait ^{t}MRD before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Figure 14: Mode Register Definition


BA1 BA0 An ... A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Address bus
Mn+2 Mn+1 Mn ... M10 M9 M8 M7 M6 M5 M4 M3 M2 M1 M0
Mode register (Mx)
n+2 / n+1 / n / ... / 10 / 9 / 8 / 7 / 6 / 5 / 4 / 3 / 2 / 1 / 0
0 | 0 | Reserved* | WB | Op mode | CAS latency | BT | Burst length

Mn+2	Mn+1	Mode Register Definition
0	0	Base mode register
0	1	Reserved
1	0	Extended mode register
1	1	Reserved

M9	Write Burst Mode
0	Programmed burst length
1	Single location access

M8	M7	Operating Mode
0	0	Normal operation
–	–	All other states reserved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

			Burst Length	
M2	M1	M0	M3 = 0	M3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Continuous	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

*Should be programmed to "0" to ensure compatibility with future devices.

Burst Length (BL)

Read and write accesses to the SDRAM are burst oriented and the BL is programmable, (see Figure 14). The BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, 8, or continuous locations are available for both the sequential and the interleaved burst types, and a continuous page burst is available for the sequential type. The continuous page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary BLs.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst wraps within the block when a boundary is reached. The block is uniquely selected by A[8:1] when BL = 2, A[8:2] when BL = 4, and A[8:3] when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Continuous page bursts wrap within the page when the boundary is reached.

Burst Type

Accesses within a given burst can be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the BL, the burst type, and the starting column address, as shown in Table 19.

Table 19: Burst Definition Table

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			**A0**		
			0	0-1	0-1
			1	1-0	1-0
4		**A1**	**A0**		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	**A2**	**A1**	**A0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Continuous					
	n = A0–An/9/8 (location 0–y)			Cn, Cn + 1, Cn + 2, Cn + 3...Cn - 1, Cn...	Not supported

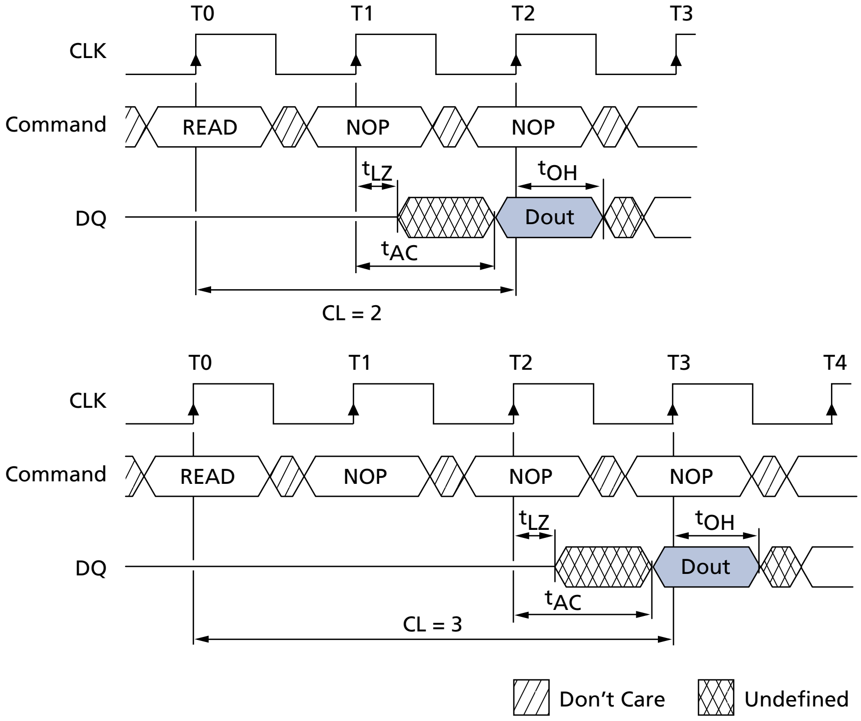
CAS Latency (CL)

The CL is the delay, in clock cycles, between the registration of a READ command and the availability of the output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQ start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data is valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQ start driving after T1 and the data is valid by T2, as shown in Figure 15 on page 37.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Figure 15: CAS Latency


T0
T1
T2
T3
CLK
Command
READ
NOP
NOP
tLZ
tOH
DQ
Dout
tAC
CL = 2
T0
T1
T2
T3
T4
CLK
Command
READ
NOP
NOP
NOP
tLZ
tOH
DQ
Dout
tAC
CL = 3
Don't Care
Undefined

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use. Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

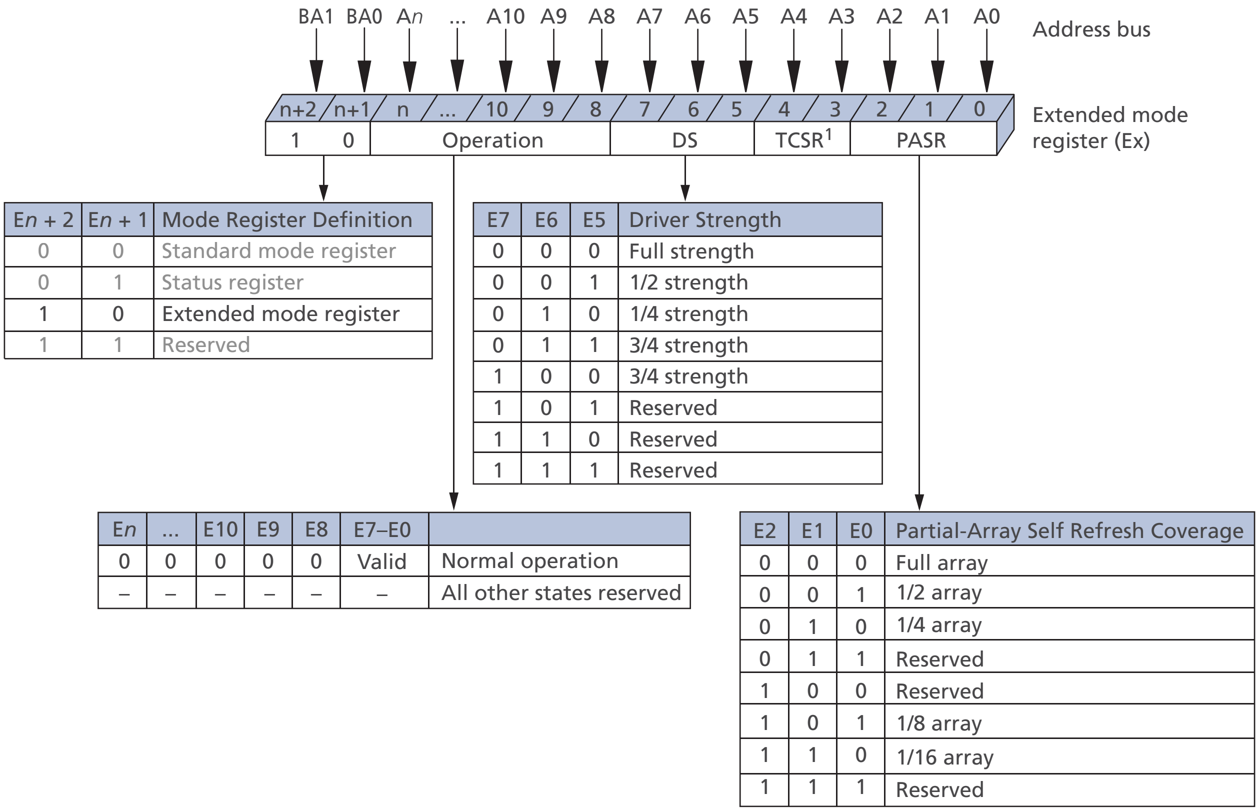
When M9 = 0, the BL programmed via M[2:0] applies to both READ and WRITE bursts; when M9 = 1, the programmed BL applies to READ bursts, but write accesses are single-location (nonburst) accesses.

Extended Mode Register (EMR)

The EMR controls additional functions beyond those controlled by the mode register. These additional functions are special features of the Mobile LPSDR device that help reduce overall system power consumption and include TCSR, PASR, and output drive strength.

The EMR is programmed via the LMR command (BA1 = 1, BA0 = 0) and retains the stored information until it is programmed again or the device loses power.

Figure 16: Extended Mode Register


BA1 BA0 An ... A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Address bus
n+2 n+1 n ... 10 9 8 7 6 5 4 3 2 1 0
1 0 Operation DS TCSR1 PASR
Extended mode register (Ex)

En + 2	En + 1	Mode Register Definition
0	0	Standard mode register
0	1	Status register
1	0	Extended mode register
1	1	Reserved

E7	E6	E5	Driver Strength
0	0	0	Full strength
0	0	1	1/2 strength
0	1	0	1/4 strength
0	1	1	3/4 strength
1	0	0	3/4 strength
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

En	...	E10	E9	E8	E7–E0	
0	0	0	0	0	Valid	Normal operation
–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial-Array Self Refresh Coverage
0	0	0	Full array
0	0	1	1/2 array
0	1	0	1/4 array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 array
1	1	0	1/16 array
1	1	1	Reserved

Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

The EMR must be programmed with E[*n:7*] set to "0." It must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. After the values are entered, the EMR settings are retained even after exiting deep power-down mode.

Temperature-Compensated Self Refresh (TCSR)

Mobile LPSDR includes a temperature sensor that is implemented for automatic control of the self refresh oscillator on the device. Programming the TCSR bits has no effect on the device. The self refresh oscillator will continue refresh at the optimal factory-programmed rate for the device temperature.

Partial-Array Self Refresh (PASR)

For further power savings during self refresh, the PASR feature enables the controller to select the amount of memory to be refreshed during self refresh. The refresh options are:

- Full array: banks 0, 1, 2, and 3
- One-half array: banks 0 and 1
- One-quarter array: bank 0
- One-eighth array: bank 0 with row address most significant bit (MSB) = 0
- One-sixteenth array: bank 0 with row address MSB = 0 and row address MSB - 1 = 0

WRITE and READ commands can still be issued to any bank selected during standard operation, but only the selected banks or segments of a bank in PASR are refreshed during self refresh. It is important to note that data in unused banks or portions of banks is lost when PASR is used.

Output Drive Strength

Because the Mobile LPSDR is designed for use in smaller systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. There are four supported settings for the output drivers: 25Ω, 37Ω, 55Ω, and 80Ω internal impedance. These are full, three-quarter, one-half, and one-quarter drive strengths, respectively.

Bank/Row Activation

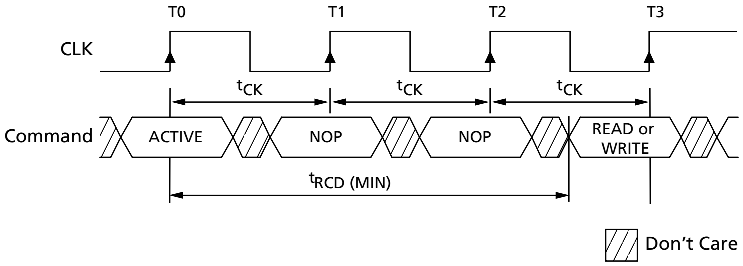
Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, that selects both the bank and the row to be activated (see Figure 17).

After opening a row is opened with the ACTIVE command, a READ or WRITE command can be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 17, which covers any case where $2 < {}^{t}\text{RCD (MIN)}/{}^{t}\text{CK} \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 17: Example: Meeting ^{t}RCD (MIN) When $2 < {}^{t}\text{RCD (MIN)}/{}^{t}\text{CK} \leq 3$



Timing Diagrams

READs

READ bursts are initiated with a READ command, as shown in Figure 10 on page 25. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

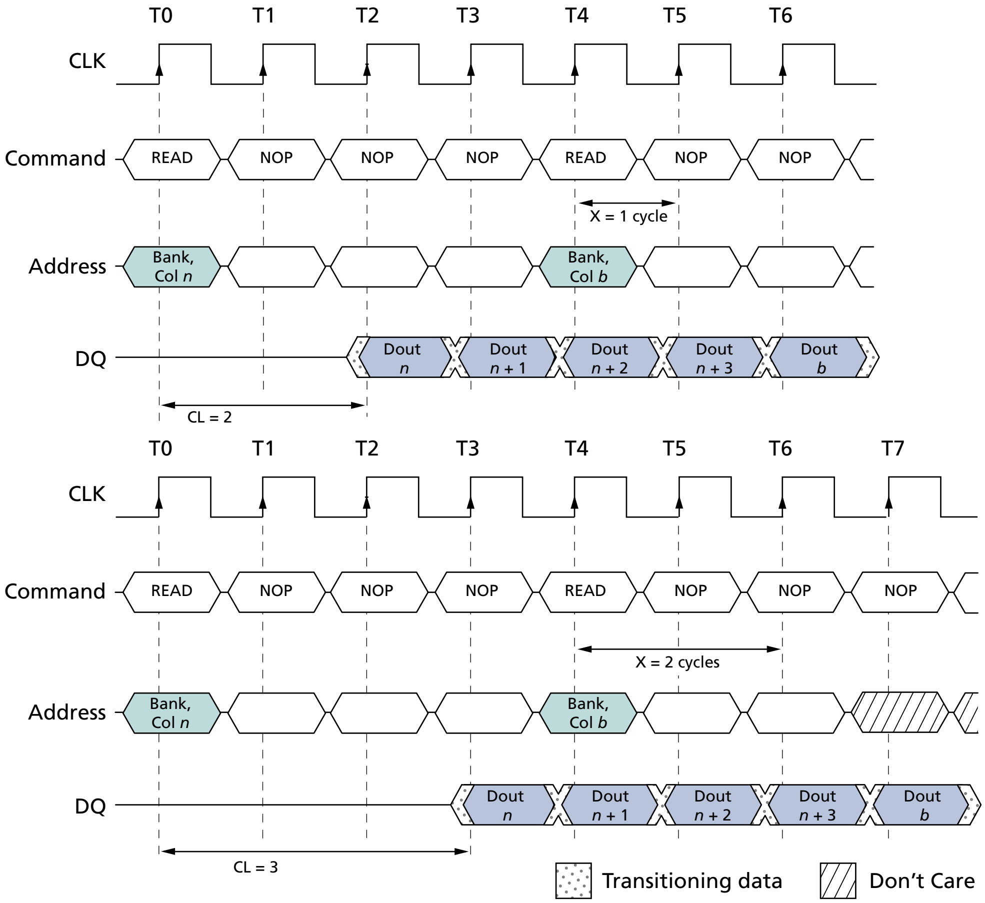
During READ bursts, the valid data-out element from the starting column address is available following the CL after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 18 on page 41 shows general timing for each possible CL setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQ signals will go to High-Z. A continuous page burst continues until terminated. At the end of the page, it wraps to column 0 and continues.

Data from any READ burst can be truncated with a subsequent READ command, and data from a fixed-length READ burst can be followed immediately by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued x cycles before the clock edge at which the last desired data element is valid, where x = CL - 1. This is shown in Figure 19 on page 42 for CL2 and CL3.

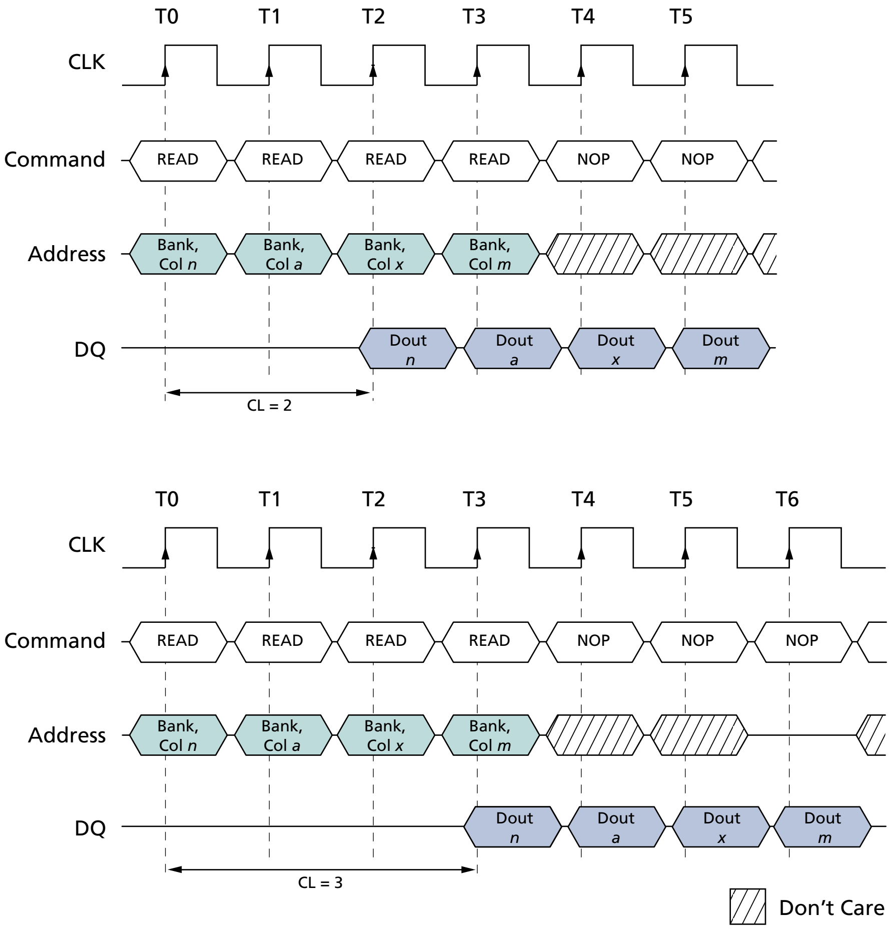
Mobile LPSDR devices use a pipelined architecture and therefore do not require the 2n rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 18 on page 41, or each subsequent READ can be performed to a different bank.

Figure 18: Consecutive READ Bursts


T0
T1
T2
T3
T4
T5
T6
CLK
Command
READ
NOP
NOP
NOP
READ
NOP
NOP
X = 1 cycle
Address
Bank, Col n
Bank, Col b
DQ
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout b
CL = 2
T0
T1
T2
T3
T4
T5
T6
T7
CLK
Command
READ
NOP
NOP
NOP
READ
NOP
NOP
NOP
X = 2 cycles
Address
Bank, Col n
Bank, Col b
DQ
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout b
CL = 3
Transitioning data
Don't Care

Notes: 1. Each READ command can be to any bank. DQM is LOW.

Figure 19: Random READ Accesses


T0
T1
T2
T3
T4
T5
CLK
Command
READ
READ
READ
READ
NOP
NOP
Address
Bank, Col n
Bank, Col a
Bank, Col x
Bank, Col m
DQ
Dout n
Dout a
Dout x
Dout m
CL = 2
T0
T1
T2
T3
T4
T5
T6
CLK
Command
READ
READ
READ
READ
NOP
NOP
NOP
Address
Bank, Col n
Bank, Col a
Bank, Col x
Bank, Col m
DQ
Dout n
Dout a
Dout x
Dout m
CL = 3
Don't Care

Notes: 1. Each READ command can be to any bank. DQM is LOW.

Data from any READ burst can be truncated with a subsequent WRITE command, and data from a fixed-length READ burst can be followed immediately by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst can be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there is a possibility that the device driving the input data will go Low-Z before the SDRAM DQ go to High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

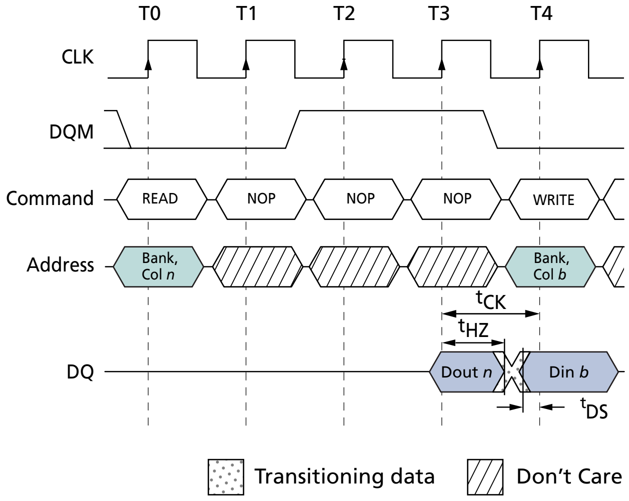
The DQM input is used to avoid I/O contention, as shown in Figure 20 on page 43 and Figure 21 on page 44. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. After the WRITE command is registered, the DQ will go to High-Z (or remain at High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 19 on page 42 shows the case where the clock frequency provides for bus contention avoidance without adding a NOP cycle, and Figure 21 on page 44 shows the case where the additional NOP cycle is required.

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated). The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 22 on page 44 for each possible CL; data element *n* + 3 is either the last of a burst of four or the last desired data element of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

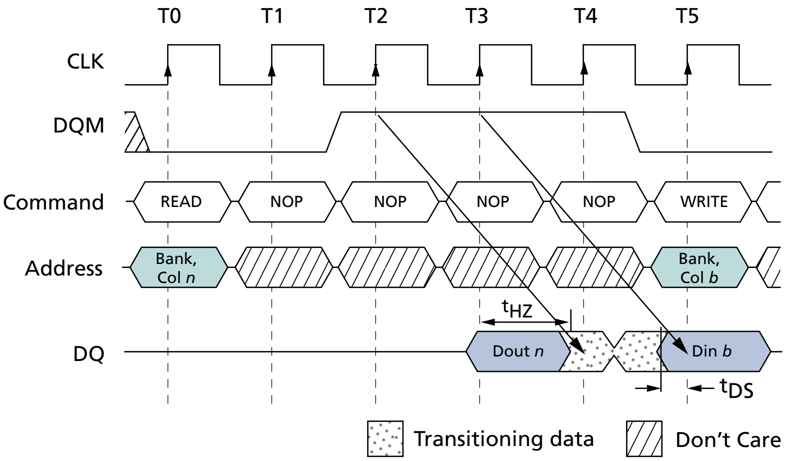
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. However, the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or continuous page bursts.

Figure 20: READ-to-WRITE



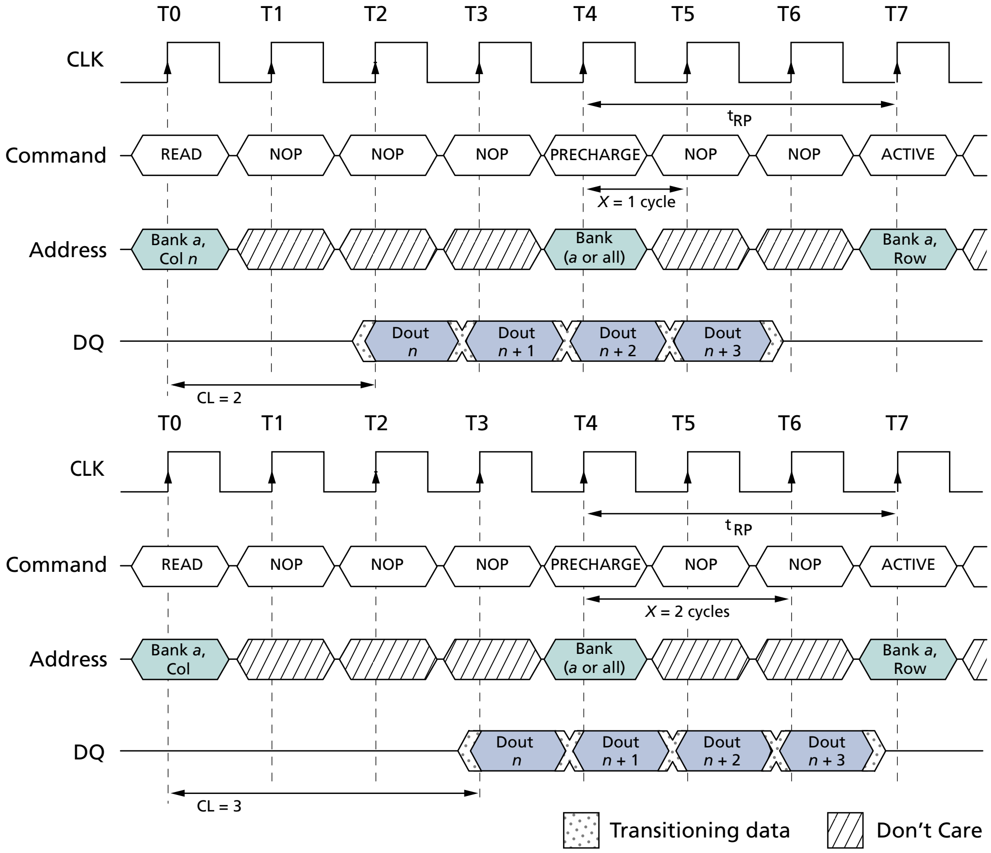
Notes: 1. CL = 3. The READ command can be to any bank, and the WRITE command can be to any bank. If a burst of one is used, DQM is not required.

Figure 21: READ-to-WRITE With Extra Clock Cycle


T0
T1
T2
T3
T4
T5
CLK
DQM
Command
READ
NOP
NOP
NOP
NOP
WRITE
Address
Bank, Col n
Bank, Col b
tHZ
DQ
Dout n
Din b
tDS
Transitioning data
Don't Care

Notes: 1. CL = 3. The READ command can be to any bank, and the WRITE command can be to any bank.

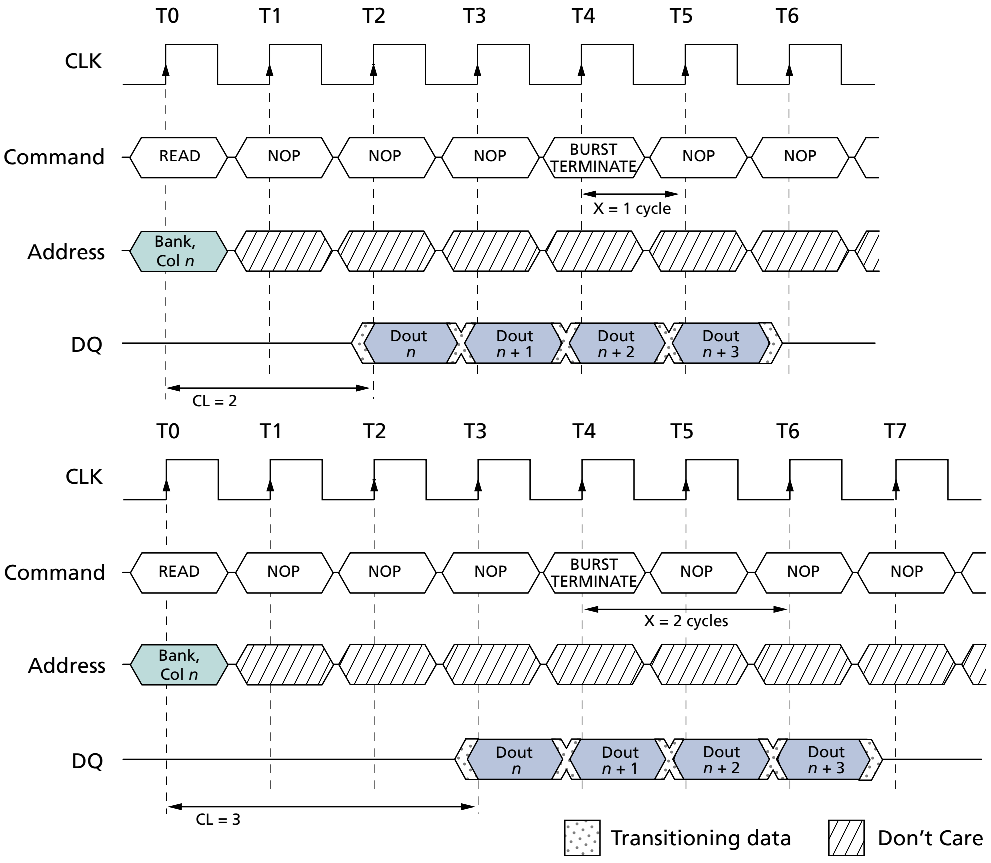
Figure 22: READ-to-PRECHARGE


T0
T1
T2
T3
T4
T5
T6
T7
CLK
tRP
Command
READ
NOP
NOP
NOP
PRECHARGE
NOP
NOP
ACTIVE
X = 1 cycle
Address
Bank a, Col n
Bank (a or all)
Bank a, Row
DQ
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
CL = 2
T0
T1
T2
T3
T4
T5
T6
T7
CLK
tRP
Command
READ
NOP
NOP
NOP
PRECHARGE
NOP
NOP
ACTIVE
X = 2 cycles
Address
Bank a, Col
Bank (a or all)
Bank a, Row
DQ
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
CL = 3
Transitioning data
Don't Care

Notes: 1. DQM is LOW.

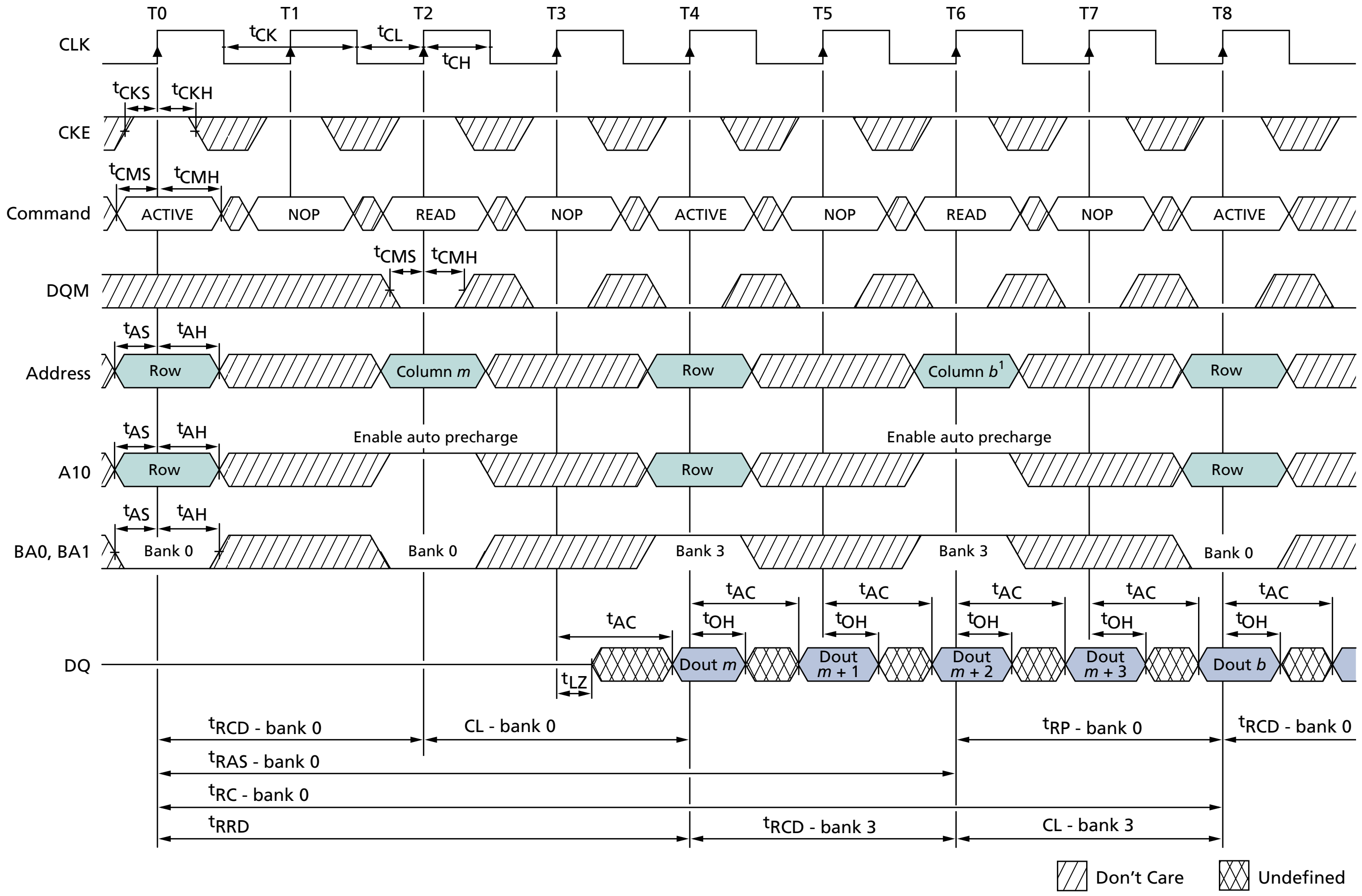
Continuous-page READ bursts can be truncated with a BURST TERMINATE command and fixed-length READ bursts can be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* = CL - 1. This is shown in Figure 23 for each possible CL; data element *n* + 3 is the last desired data element of a longer burst.

Figure 23: Terminating a READ Burst


T0
T1
T2
T3
T4
T5
T6
CLK
Command
READ
NOP
NOP
NOP
BURST TERMINATE
NOP
NOP
X = 1 cycle
Address
Bank, Col n
DQ
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
CL = 2
T0
T1
T2
T3
T4
T5
T6
T7
CLK
Command
READ
NOP
NOP
NOP
BURST TERMINATE
NOP
NOP
NOP
X = 2 cycles
Address
Bank, Col n
DQ
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
CL = 3
Transitioning data
Don't Care

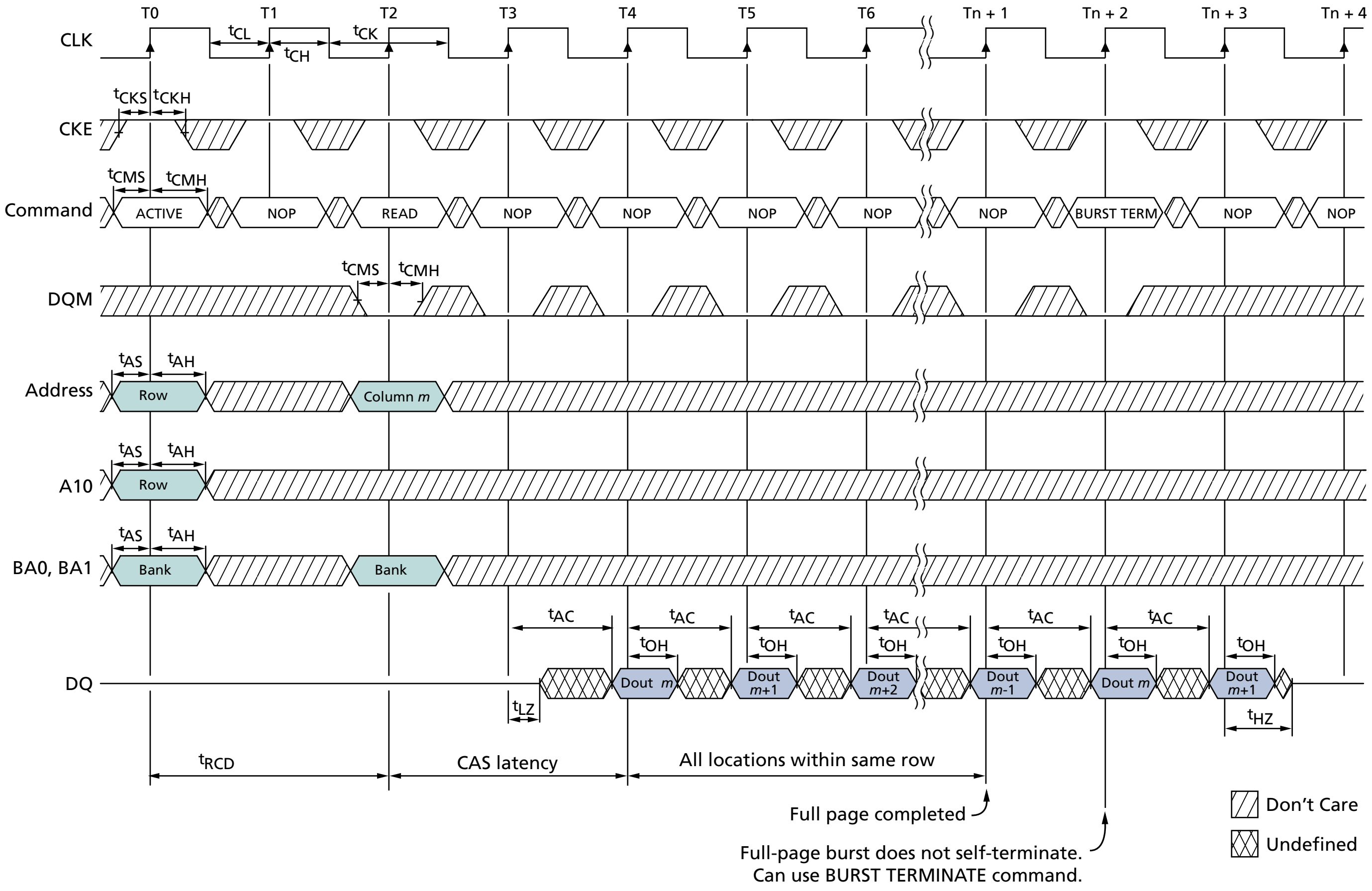
Notes: 1. DQM is LOW.

Figure 24: Alternating Bank Read Accesses


T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
READ
NOP
ACTIVE
NOP
READ
NOP
ACTIVE
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
Row
Column b1
Row
tAS
tAH
Enable auto precharge
Enable auto precharge
A10
Row
Row
Row
tAS
tAH
BA0, BA1
Bank 0
Bank 0
Bank 3
Bank 3
Bank 0
tAC
tAC
tAC
tAC
tAC
tAC
tOH
tOH
tOH
tOH
tOH
DQ
tLZ
Dout m
Dout m + 1
Dout m + 2
Dout m + 3
Dout b
tRCD - bank 0
CL - bank 0
tRP - bank 0
tRCD - bank 0
tRAS - bank 0
tRC - bank 0
tRRD
tRCD - bank 3
CL - bank 3
Don't Care
Undefined

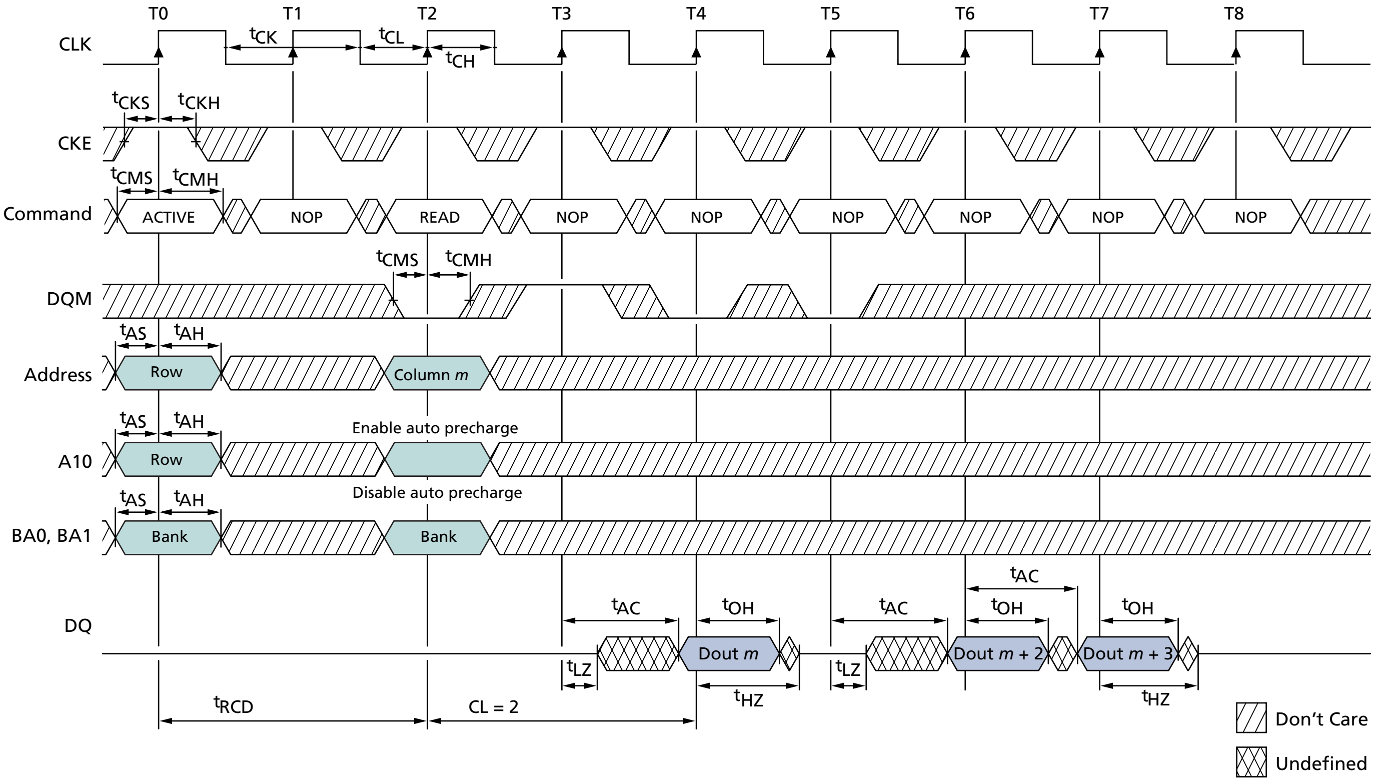
Notes: 1. For this example, BL = 4 and CL = 2.

Figure 25: READ Continuous Page Burst


T0
T1
T2
T3
T4
T5
T6
Tn + 1
Tn + 2
Tn + 3
Tn + 4
CLK
tCL
tCK
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
READ
NOP
NOP
NOP
NOP
NOP
BURST TERM
NOP
NOP
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
tAS
tAH
A10
Row
tAS
tAH
BA0, BA1
Bank
Bank
tAC
tAC
tAC
tAC
tAC
tAC
tOH
tOH
tOH
tOH
tOH
tOH
DQ
Dout m
Dout m+1
Dout m+2
Dout m-1
Dout m
Dout m+1
tLZ
tHZ
tRCD
CAS latency
All locations within same row
Full page completed
Full-page burst does not self-terminate.
Can use BURST TERMINATE command.
Don't Care
Undefined

Notes: 1. For this example, CL = 2.

Figure 26: READ – DQM Operation


T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
tCK
tCL
tCH
CKE
tCKS
tCKH
Command
tCMS
tCMH
ACTIVE
NOP
READ
NOP
NOP
NOP
NOP
NOP
NOP
DQM
tCMS
tCMH
Address
tAS
tAH
Row
Column m
A10
tAS
tAH
Row
Enable auto precharge
Disable auto precharge
BA0, BA1
tAS
tAH
Bank
Bank
DQ
tAC
tOH
tAC
tAC
tOH
tOH
Dout m
Dout m + 2
Dout m + 3
tLZ
tLZ
tHZ
tHZ
tRCD
CL = 2
Don't Care
Undefined

Notes: 1. For this example, BL = 4 and CL = 2.

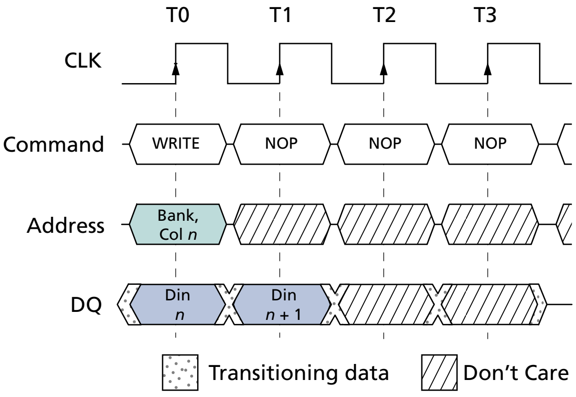
WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 11 on page 26. The starting column and bank addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element is registered coincident with the WRITE command. Subsequent data elements are registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQ will remain at High-Z and any additional input data will be ignored (see Figure 27). A continuous page burst continues until terminated; at the end of the page, it wraps to column 0 and continues.

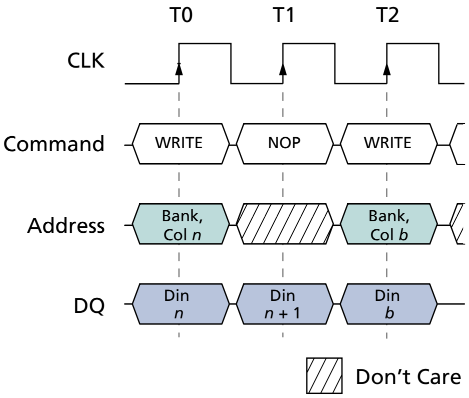
Data for any WRITE burst can be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst can be followed immediately by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command (seeFigure 28 on page 50). Data *n* + 1 is either the last of a burst of two or the last desired data element of a longer burst. Mobile LPSDR uses a pipelined architecture and therefore does not require the 2*n* rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 29 on page 51, or each subsequent WRITE can be performed to a different bank.

Figure 27: WRITE Burst



Notes: 1. BL = 2. DQM is LOW.

Figure 28: WRITE-to-WRITE



Notes: 1. DQM is LOW. Each WRITE command may be to any bank.

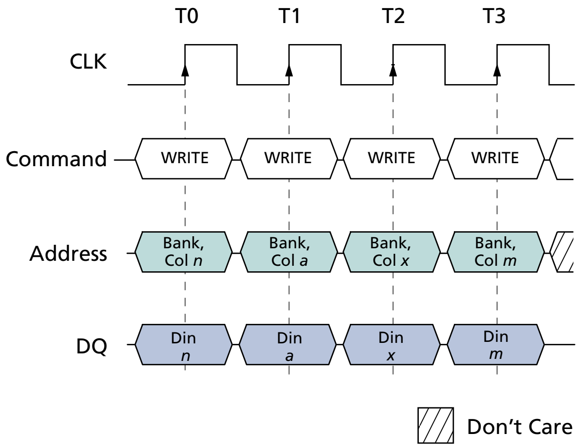
Data for any WRITE burst can be truncated with a subsequent READ command, and data for a fixed-length WRITE burst can be followed immediately by a READ command. After the READ command is registered, data input is ignored and WRITEs will not be executed (see Figure 30 on page 51). Data *n* + 1 is either the last of a burst of two or the last desired data element of a longer burst.

Data for a fixed-length WRITE burst can be followed by or truncated with a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a continuous-page WRITE burst can be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued ^{t}WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a ^{t}WR of at least one clock with time to complete, regardless of frequency.

In addition, when truncating a WRITE burst at high clock frequencies (^{t}CK < 15ns), the DQM signal must be used to mask input data for the clock edge prior to and the clock edge coincident with the PRECHARGE command (see Figure 31 on page 52). Data *n* + 1 is either the last of a burst of two or the last desired data element of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

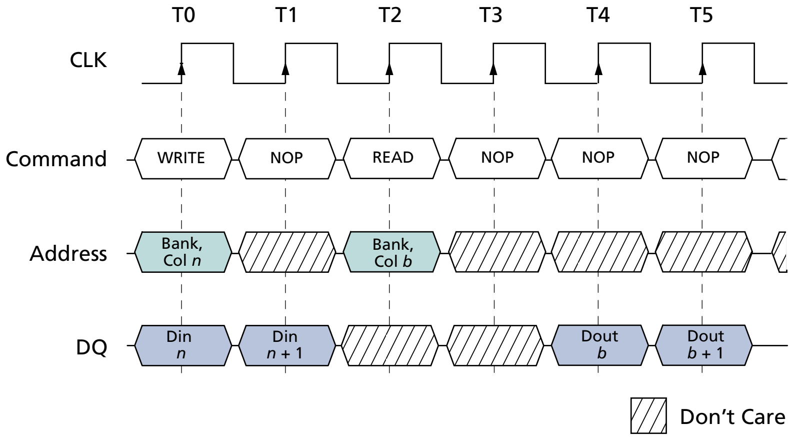
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts or continuous page bursts.

Figure 29: Random WRITE Cycles


T0
T1
T2
T3
CLK
Command
WRITE
WRITE
WRITE
WRITE
Address
Bank, Col n
Bank, Col a
Bank, Col x
Bank, Col m
DQ
Din n
Din a
Din x
Din m
Don't Care

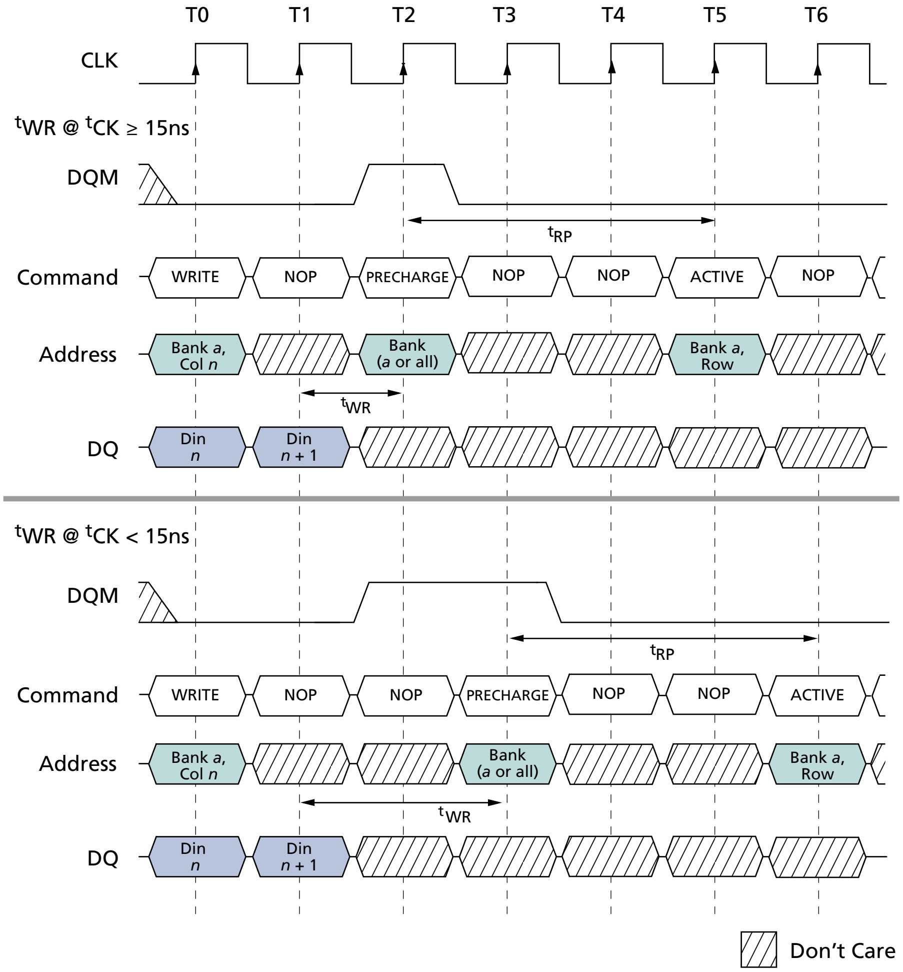
Notes: 1. Each WRITE command can be to any bank. DQM is LOW.

Figure 30: WRITE-to-READ


T0
T1
T2
T3
T4
T5
CLK
Command
WRITE
NOP
READ
NOP
NOP
NOP
Address
Bank, Col n
Bank, Col b
DQ
Din n
Din n + 1
Dout b
Dout b + 1
Don't Care

Notes: 1. The WRITE command can be to any bank, and the READ command can be to any bank. DQM is LOW. CL = 2 for illustration.

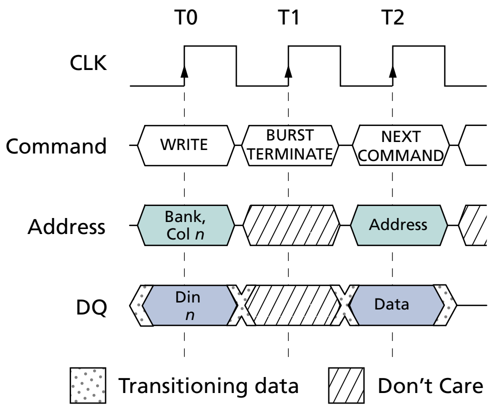
Figure 31: WRITE-to-PRECHARGE


T0
T1
T2
T3
T4
T5
T6
CLK
tWR @ tCK ≥ 15ns
DQM
tRP
Command
WRITE
NOP
PRECHARGE
NOP
NOP
ACTIVE
NOP
Address
Bank a, Col n
Bank (a or all)
Bank a, Row
tWR
DQ
Din n
Din n + 1
tWR @ tCK < 15ns
DQM
tRP
Command
WRITE
NOP
NOP
PRECHARGE
NOP
NOP
ACTIVE
Address
Bank a, Col n
Bank (a or all)
Bank a, Row
tWR
DQ
Din n
Din n + 1
Don't Care

Notes: 1. In this example DQM could remain LOW if the WRITE burst is a fixed length of two.

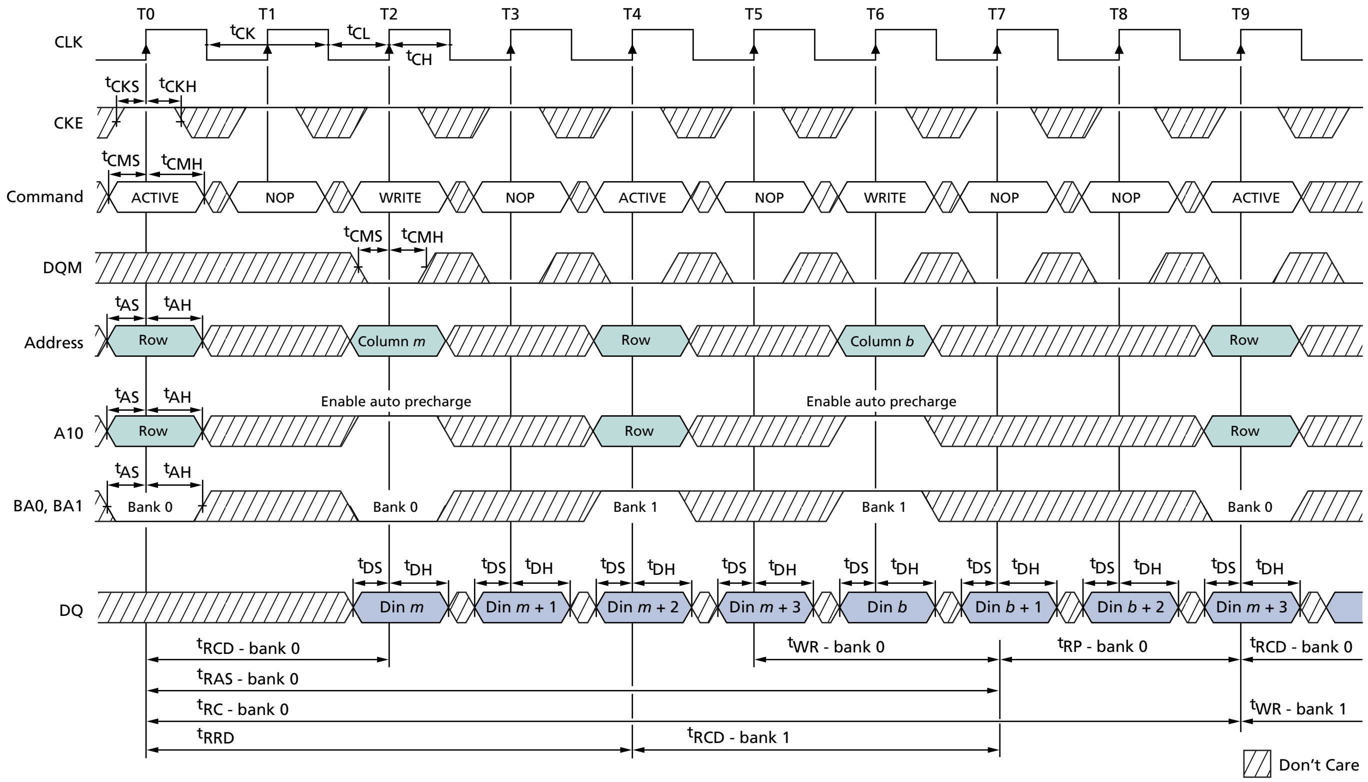
Fixed-length WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command is ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 32 on page 53, where data *n* is the last desired data element of a longer burst.

Figure 32: Terminating a WRITE Burst


T0
T1
T2
CLK
Command
WRITE
BURST TERMINATE
NEXT COMMAND
Address
Bank, Col n
Address
DQ
Din n
Data
Transitioning data
Don't Care

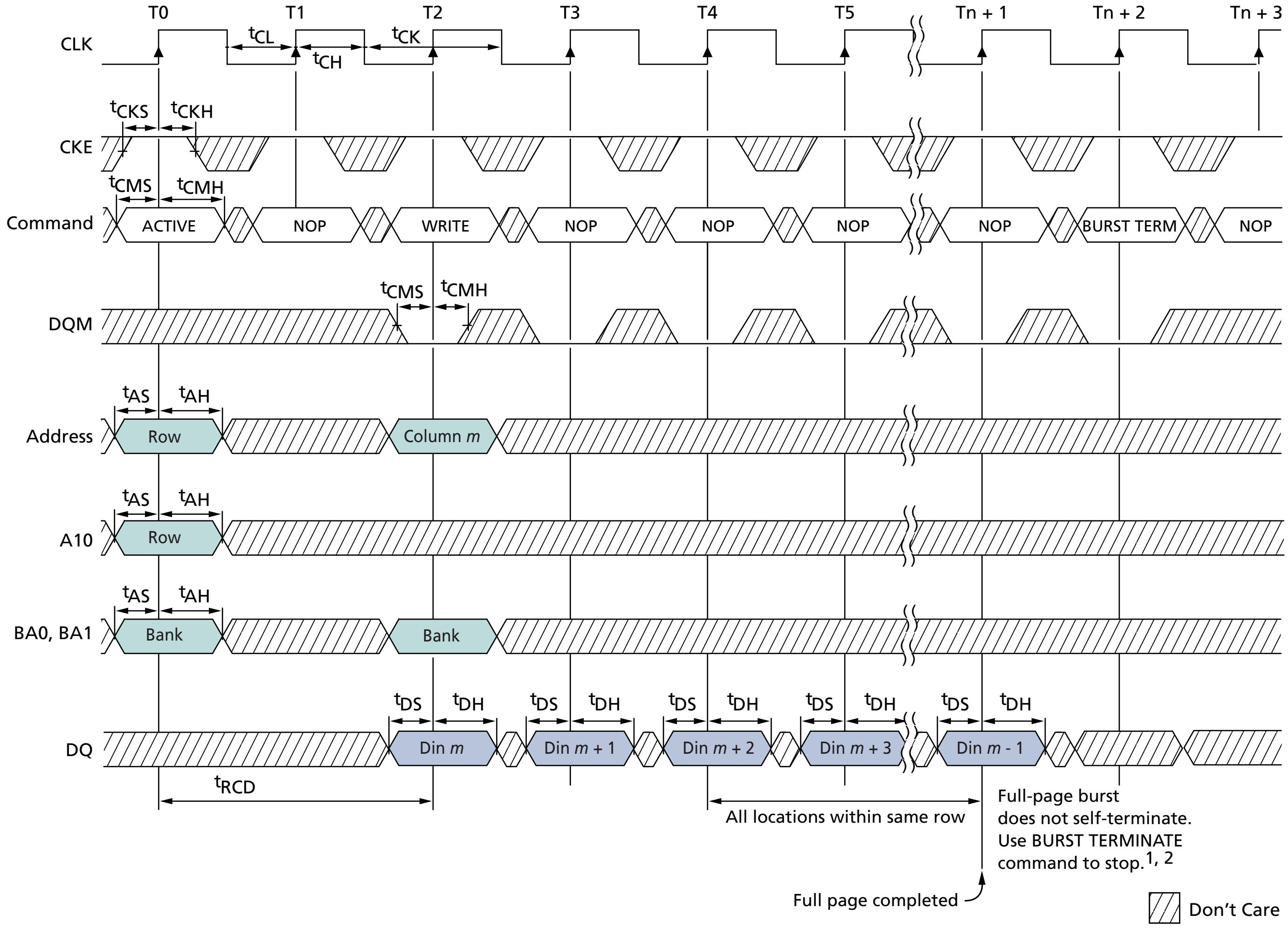
Notes: 1. DQM is LOW.

Figure 33: Alternating Bank Write Accesses


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
WRITE
NOP
ACTIVE
NOP
WRITE
NOP
NOP
ACTIVE
DQM
Address
tAS
tAH
Row
Column m
Row
Column b
Row
A10
Enable auto precharge
Enable auto precharge
BA0, BA1
Bank 0
Bank 0
Bank 1
Bank 1
Bank 0
tDS
tDH
DQ
Din m
Din m + 1
Din m + 2
Din m + 3
Din b
Din b + 1
Din b + 2
Din m + 3
tRCD - bank 0
tWR - bank 0
tRP - bank 0
tRCD - bank 0
tRAS - bank 0
tRC - bank 0
tWR - bank 1
tRRD
tRCD - bank 1
Don't Care

Notes: 1. For this example, BL = 4.

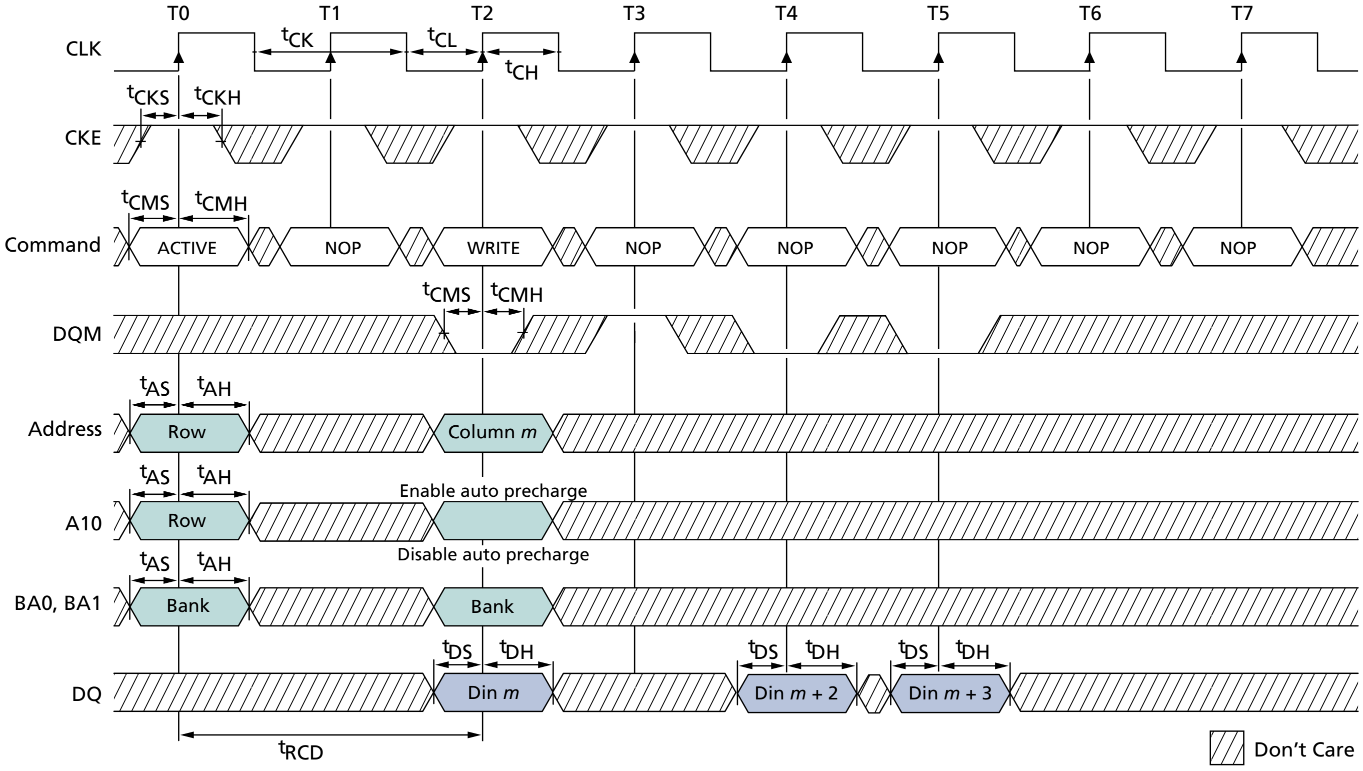
Figure 34: WRITE – Continuous Page Burst


T0
T1
T2
T3
T4
T5
Tn + 1
Tn + 2
Tn + 3
CLK
tCL
tCH
tCK
CKE
tCKS
tCKH
Command
tCMS
tCMH
ACTIVE
NOP
WRITE
NOP
NOP
NOP
NOP
BURST TERM
NOP
DQM
tCMS
tCMH
Address
tAS
tAH
Row
Column m
A10
tAS
tAH
Row
BA0, BA1
tAS
tAH
Bank
Bank
DQ
tDS
tDH
Din m
Din m + 1
Din m + 2
Din m + 3
Din m - 1
tRCD
All locations within same row
Full-page burst
does not self-terminate.
Use BURST TERMINATE
command to stop.1, 2
Full page completed
Don't Care

Notes: 1. ^{t}WR must be satisfied prior to issuing a PRECHARGE command.

2. Page left open; no ^{t}RP.

Figure 35: WRITE – DQM Operation


T0
T1
T2
T3
T4
T5
T6
T7
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
tAS
tAH
Enable auto precharge
A10
Row
tAS
tAH
Disable auto precharge
BA0, BA1
Bank
Bank
tDS
tDH
tDS
tDH
tDS
tDH
DQ
Din m
Din m + 2
Din m + 3
tRCD
Don't Care

Notes: 1. For this example, BL = 4.

Burst Read/Single Write

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a "1." In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed BL. READ commands access columns according to the programmed BL and sequence, just as in the normal mode of operation (M9 = 0).

PRECHARGE

The PRECHARGE command (see Figure 12 on page 27) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged (A10 = LOW), inputs BA0 and BA1 select the bank. When all banks are to be precharged (A10 = HIGH), inputs BA0 and BA1 are treated as "Don't Care." After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Auto Precharge

Auto precharge is a feature that performs the same individual-bank PRECHARGE function described previously, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the continuous page burst mode, where auto precharge does not apply. In the specific case of write burst mode set to single location access with burst length set to continuous, the burst length setting is the overriding setting and auto precharge does not apply. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Burst Type section on page 36.

This device supports ^{t}RAS lock-out. In the case of a single READ with auto precharge, or a single WRITE with auto precharge, issued at ^{t}RCD (MIN), the internal precharge will be delayed until ^{t}RAS (MIN) has been satisfied.

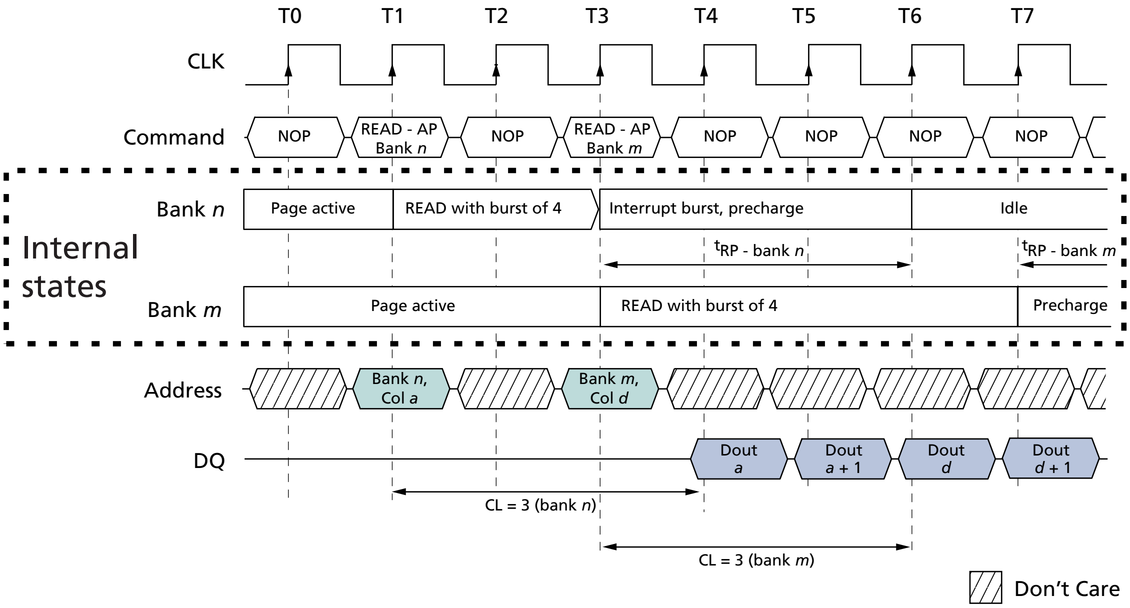
Concurrent Auto Precharge

Initiating an access command (READ or WRITE) to a second bank while an access command with auto precharge enabled on a first bank is executing is not supported by SDRAM, unless the SDRAM supports concurrent auto precharge. Micron SDRAM supports concurrent auto precharge. Four cases where concurrent auto precharge occurs are defined in the following sections; two are for READ with auto precharge, two are for WRITE with auto precharge.

READ With Auto Precharge

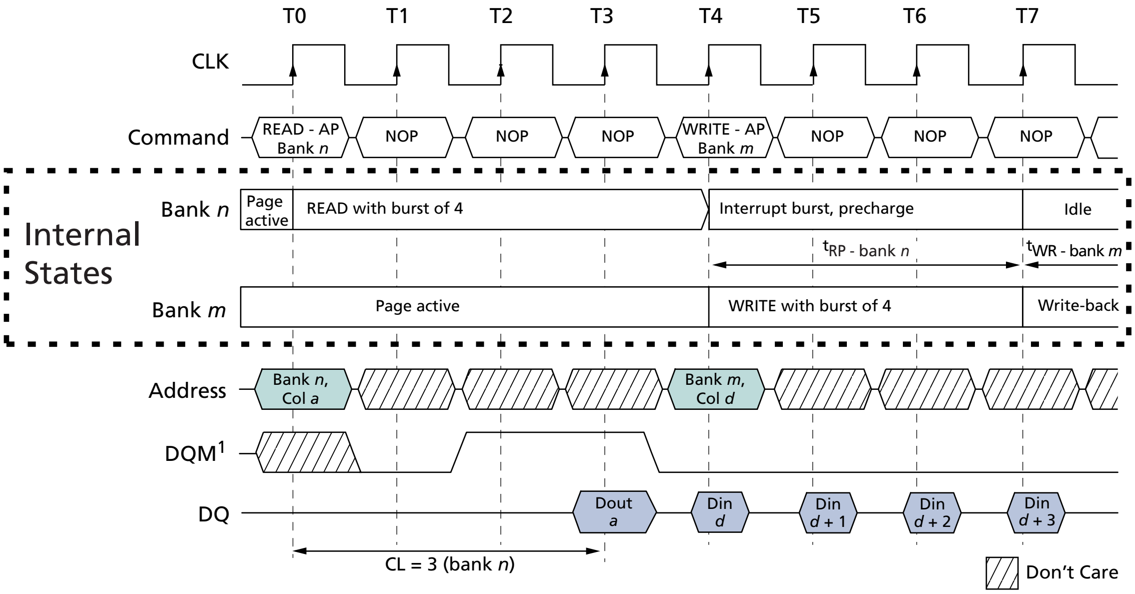
- Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a READ on bank *n* following the programmed CL. The precharge to bank *n* begins when the READ to bank *m* is registered (see Figure 36 on page 57).
- Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank *n* begins when the WRITE to bank *m* is registered (see Figure 37 on page 57).

Figure 36: READ With Auto Precharge Interrupted by a READ


T0
T1
T2
T3
T4
T5
T6
T7
CLK
Command
NOP
READ - AP Bank n
NOP
READ - AP Bank m
NOP
NOP
NOP
NOP
Internal states
Bank n
Page active
READ with burst of 4
Interrupt burst, precharge
Idle
tRP - bank n
tRP - bank m
Bank m
Page active
READ with burst of 4
Precharge
Address
Bank n, Col a
Bank m, Col d
DQ
Dout a
Dout a + 1
Dout d
Dout d + 1
CL = 3 (bank n)
CL = 3 (bank m)
Don't Care

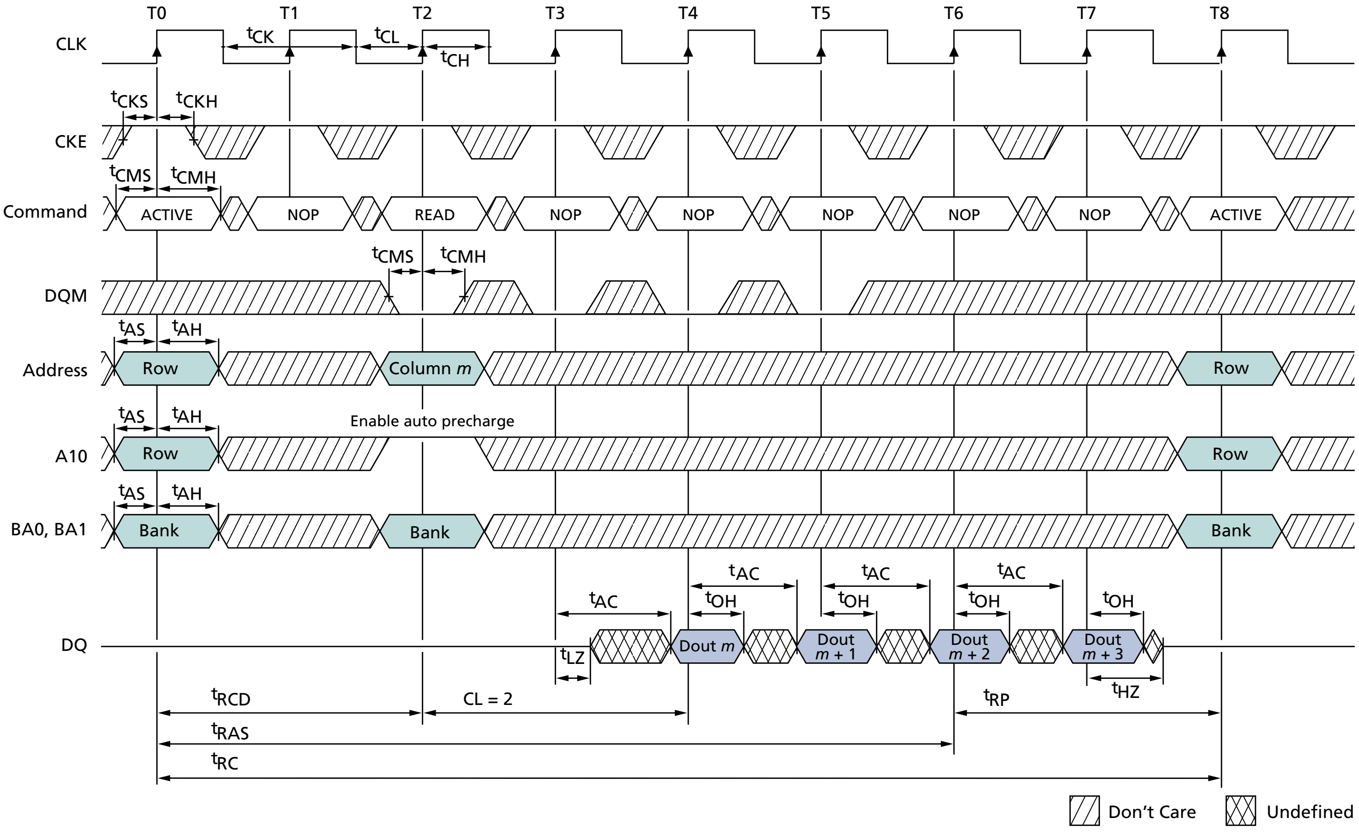
Notes: 1. DQM is LOW.

Figure 37: READ With Auto Precharge Interrupted by a WRITE


T0
T1
T2
T3
T4
T5
T6
T7
CLK
Command
READ - AP Bank n
NOP
NOP
NOP
WRITE - AP Bank m
NOP
NOP
NOP
Internal States
Bank n
Page active
READ with burst of 4
Interrupt burst, precharge
Idle
tRP - bank n
tWR - bank m
Bank m
Page active
WRITE with burst of 4
Write-back
Address
Bank n, Col a
Bank m, Col d
DQM1
DQ
Dout a
Din d
Din d + 1
Din d + 2
Din d + 3
CL = 3 (bank n)
Don't Care

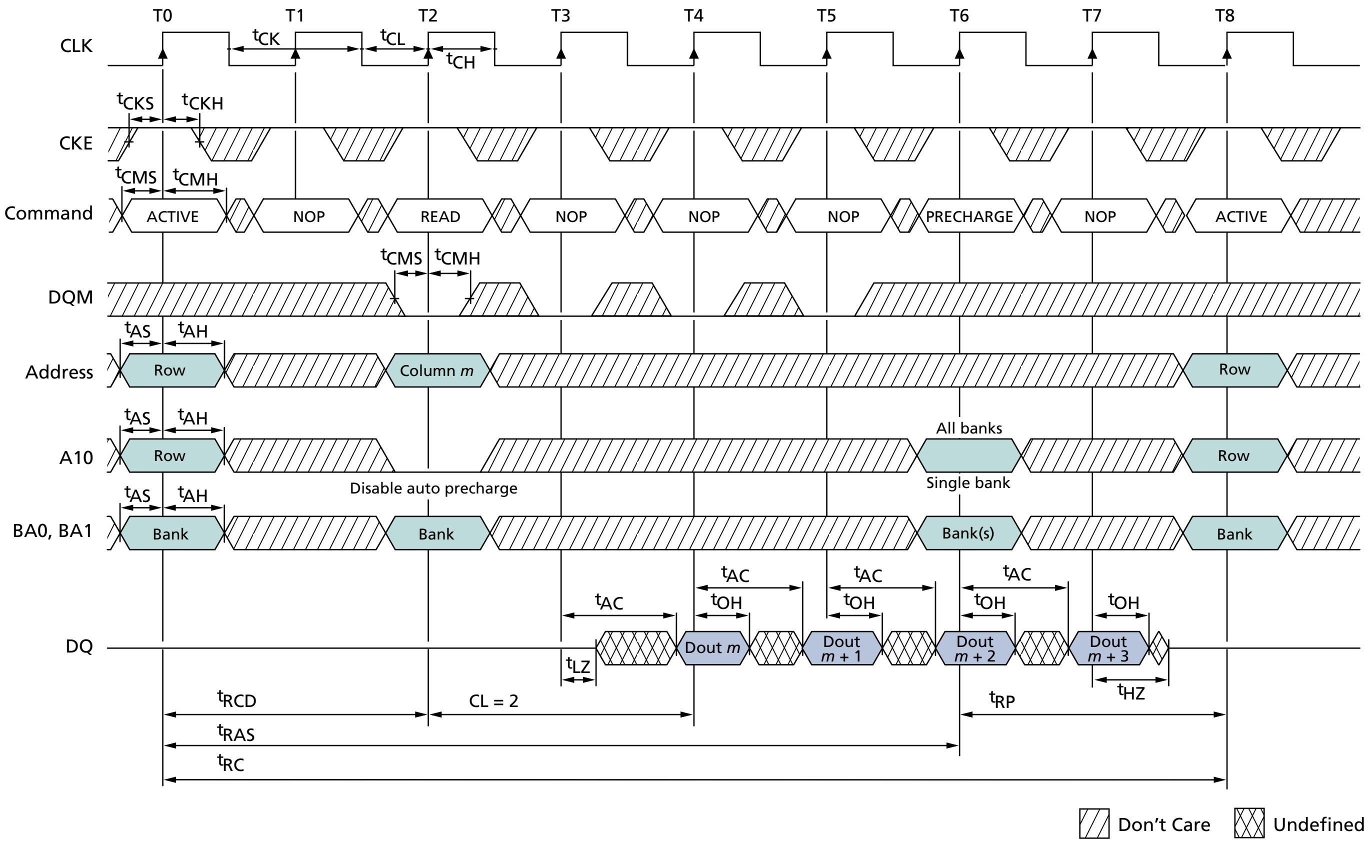
Notes: 1. DQM is HIGH at T2 to prevent Dout *a* + 1 from contending with Din *d* at T4.

Figure 38: READ With Auto Precharge


T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
READ
NOP
NOP
NOP
NOP
NOP
ACTIVE
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
Row
tAS
tAH
Enable auto precharge
A10
Row
Row
tAS
tAH
BA0, BA1
Bank
Bank
Bank
tAC
tOH
tAC
tOH
tAC
tOH
tAC
tOH
DQ
tLZ
Dout m
Dout m + 1
Dout m + 2
Dout m + 3
tHZ
tRCD
CL = 2
tRP
tRAS
tRC
Don't Care
Undefined

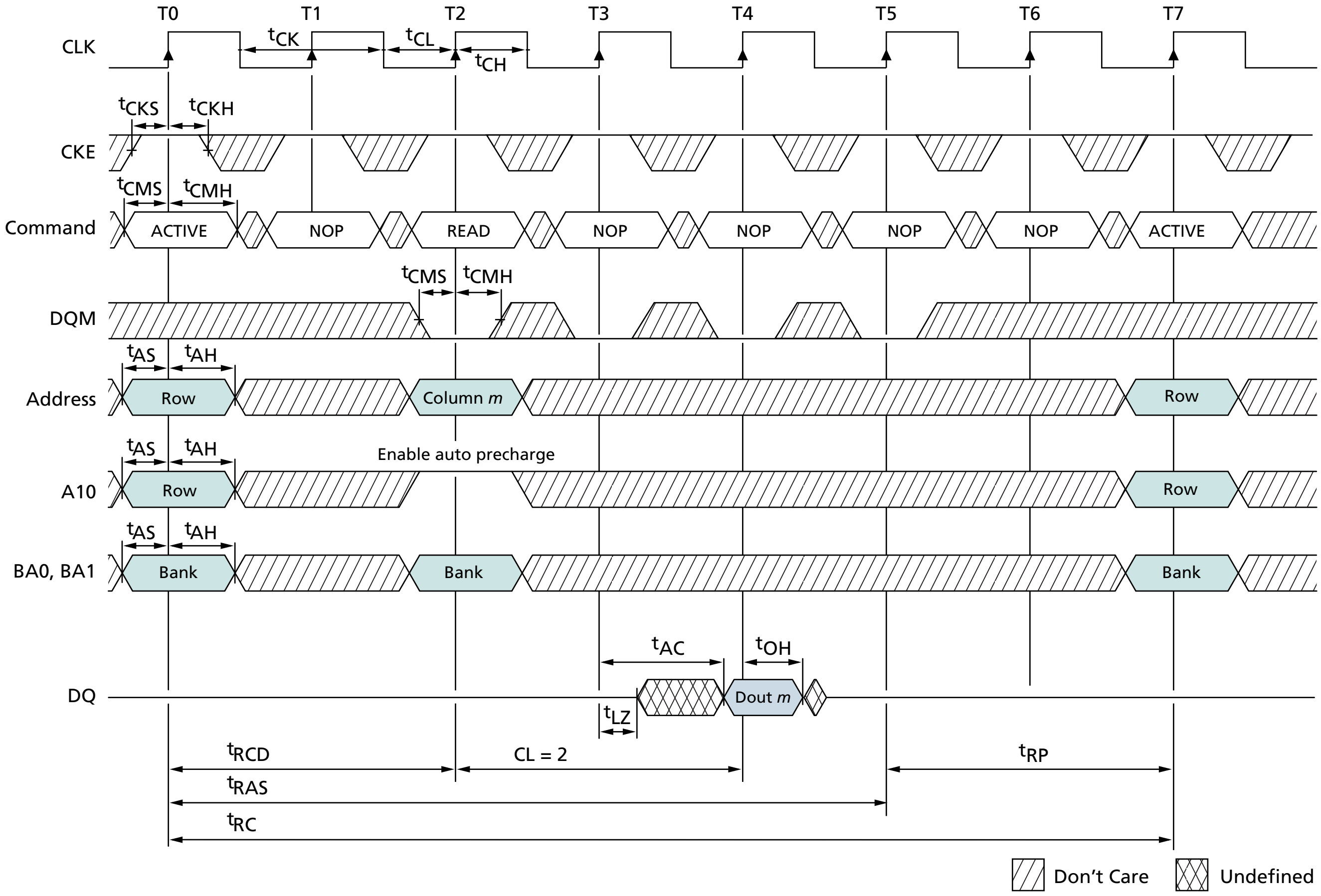
Notes: 1. For this example, BL = 4 and CL = 2.

Figure 39: READ Without Auto Precharge


T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
READ
NOP
NOP
NOP
PRECHARGE
NOP
ACTIVE
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
Row
tAS
tAH
A10
Row
All banks
Row
Disable auto precharge
Single bank
tAS
tAH
BA0, BA1
Bank
Bank
Bank(s)
Bank
tAC
tAC
tAC
tAC
tOH
tOH
tOH
tOH
DQ
Dout m
Dout m + 1
Dout m + 2
Dout m + 3
tLZ
tHZ
tRCD
CL = 2
tRP
tRAS
tRC
Don't Care
Undefined

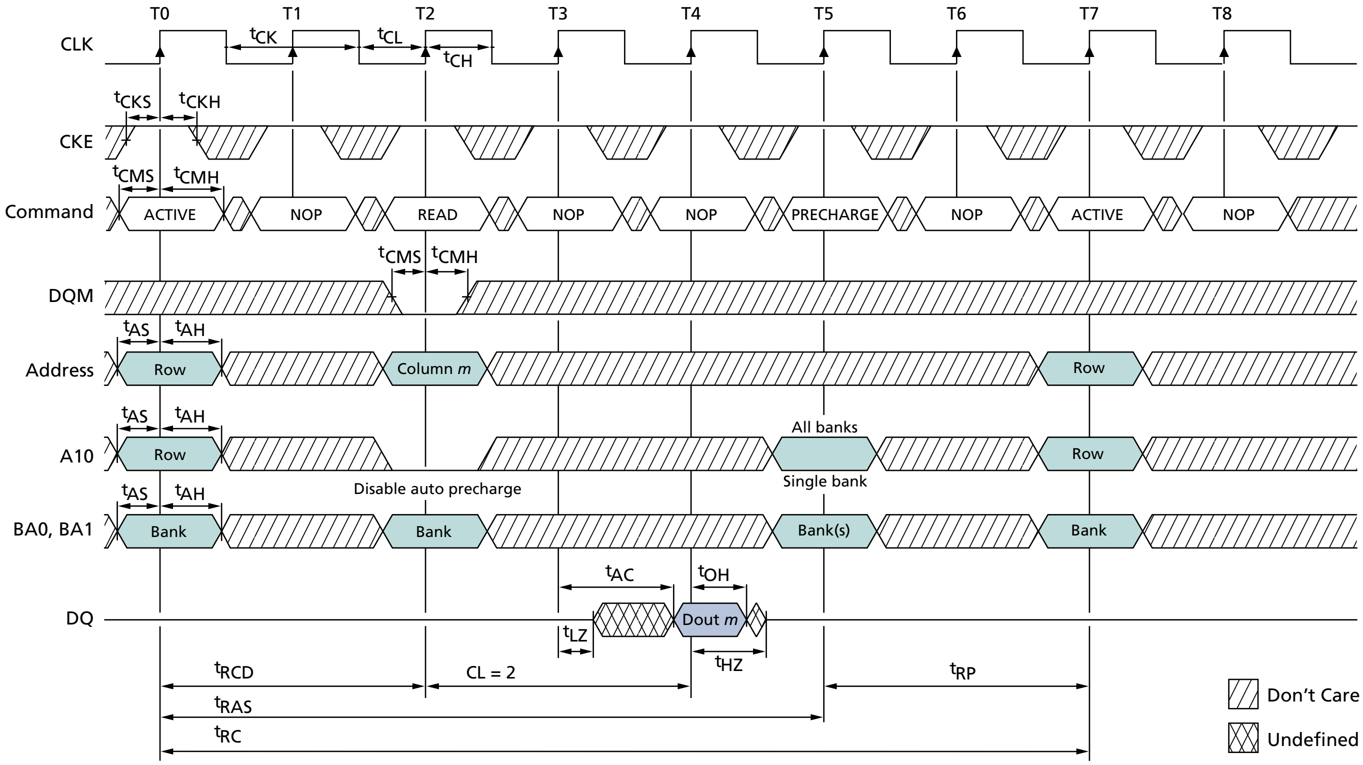
Notes: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.

Figure 40: Single READ With Auto Precharge


T0
T1
T2
T3
T4
T5
T6
T7
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
READ
NOP
NOP
NOP
NOP
ACTIVE
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
Row
tAS
tAH
Enable auto precharge
A10
Row
Row
tAS
tAH
BA0, BA1
Bank
Bank
Bank
tAC
tOH
DQ
Dout m
tLZ
tRCD
CL = 2
tRP
tRAS
tRC
Don't Care
Undefined

Notes: 1. For this example, BL = 1 and CL = 2.

Figure 41: Single READ Without Auto Precharge

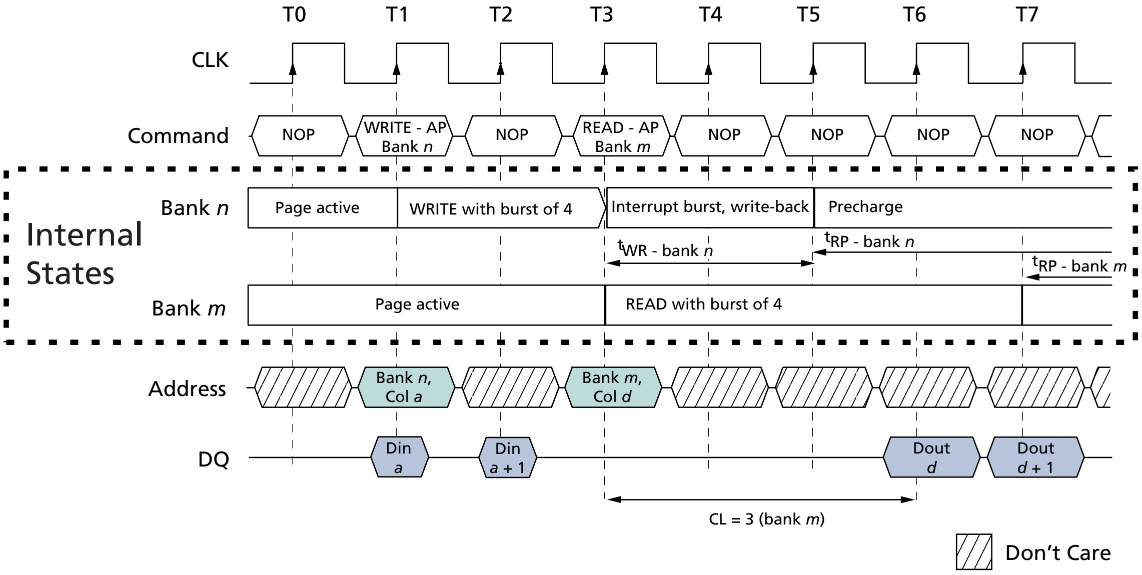

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
READ
NOP
NOP
PRECHARGE
NOP
ACTIVE
NOP
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
Row
tAS
tAH
A10
Row
All banks
Row
Single bank
tAS
tAH
Disable auto precharge
BA0, BA1
Bank
Bank
Bank(s)
Bank
tAC
tOH
DQ
Dout m
tLZ
tHZ
tRCD
CL = 2
tRP
tRAS
tRC
Don't Care
Undefined

Notes: 1. For this example, BL = 1, CL = 2, and the READ burst is followed by a manual PRECHARGE.

WRITE With Auto Precharge

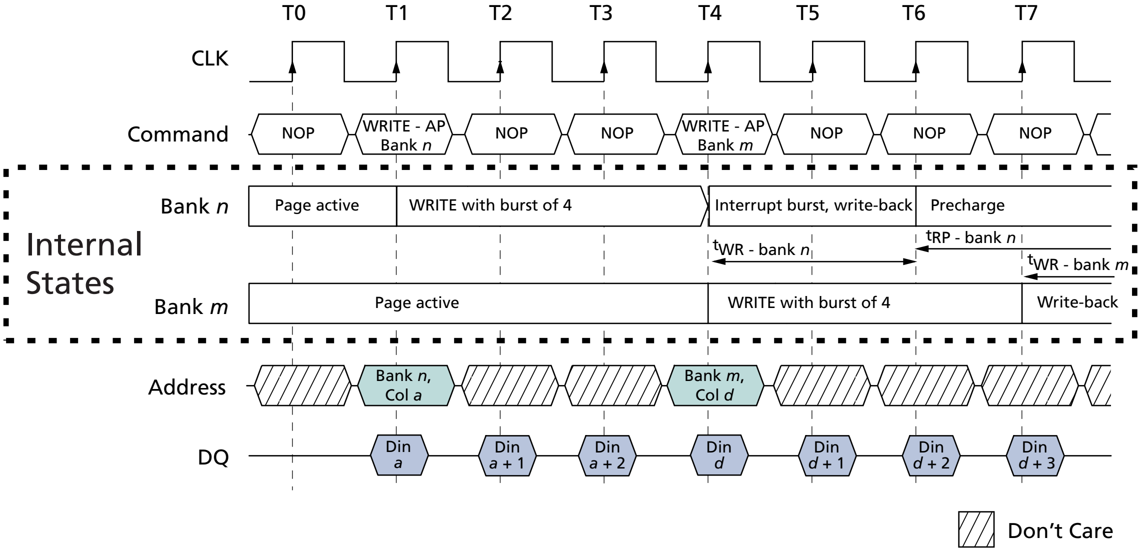
- Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a WRITE on bank *n* when registered, with the data-out appearing CL later. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (see Figure 42 on page 62).
- Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a WRITE on bank *n* when registered. The precharge to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (see Figure 43 on page 62).

Figure 42: WRITE With Auto Precharge Interrupted by a READ


T0
T1
T2
T3
T4
T5
T6
T7
CLK
Command
NOP
WRITE - AP Bank n
NOP
READ - AP Bank m
NOP
NOP
NOP
NOP
Internal States
Bank n
Page active
WRITE with burst of 4
Interrupt burst, write-back
Precharge
tWR - bank n
tRP - bank n
tRP - bank m
Bank m
Page active
READ with burst of 4
Address
Bank n, Col a
Bank m, Col d
DQ
Din a
Din a + 1
Dout d
Dout d + 1
CL = 3 (bank m)
Don't Care

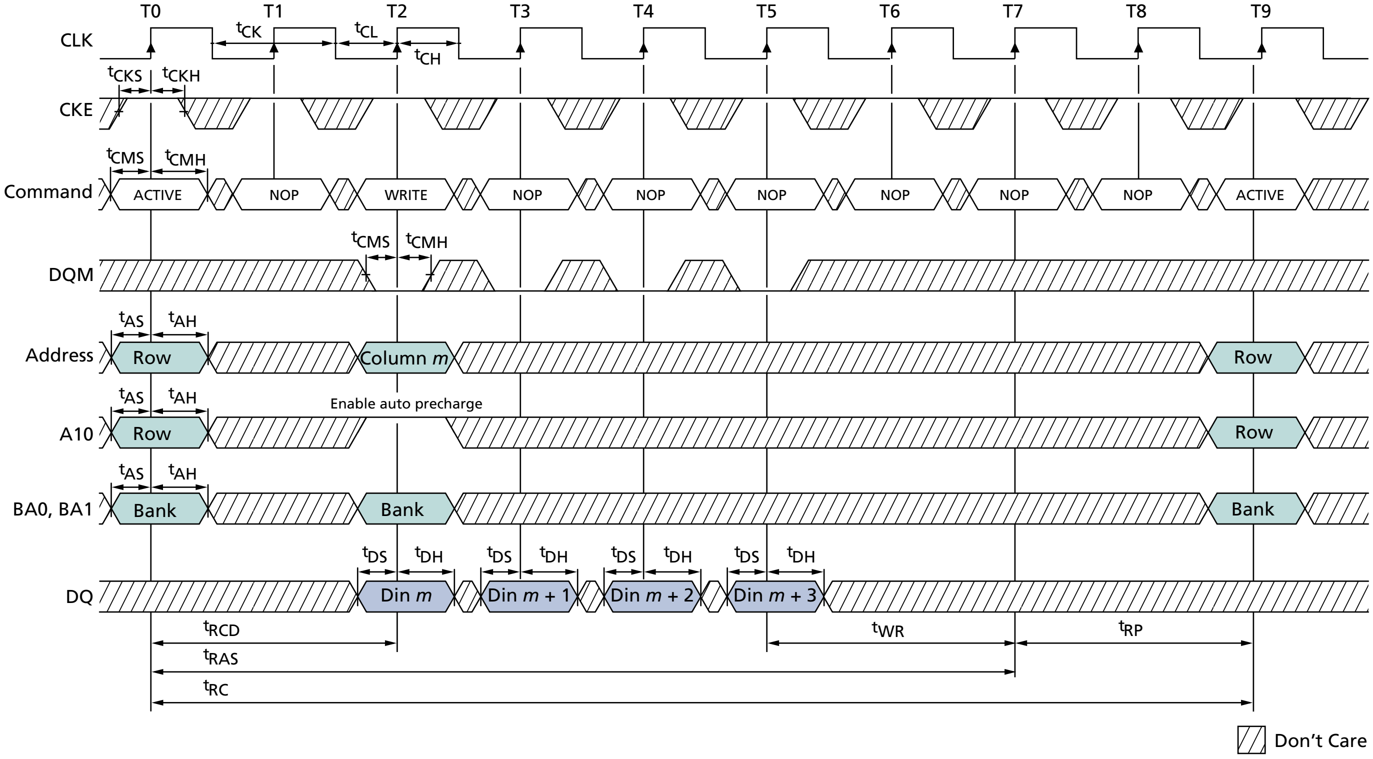
Notes: 1. DQM is LOW.

Figure 43: WRITE With Auto Precharge Interrupted by a WRITE


T0
T1
T2
T3
T4
T5
T6
T7
CLK
Command
NOP
WRITE - AP Bank n
NOP
NOP
WRITE - AP Bank m
NOP
NOP
NOP
Internal States
Bank n
Page active
WRITE with burst of 4
Interrupt burst, write-back
Precharge
tWR - bank n
tRP - bank n
tWR - bank m
Bank m
Page active
WRITE with burst of 4
Write-back
Address
Bank n, Col a
Bank m, Col d
DQ
Din a
Din a + 1
Din a + 2
Din d
Din d + 1
Din d + 2
Din d + 3
Don't Care

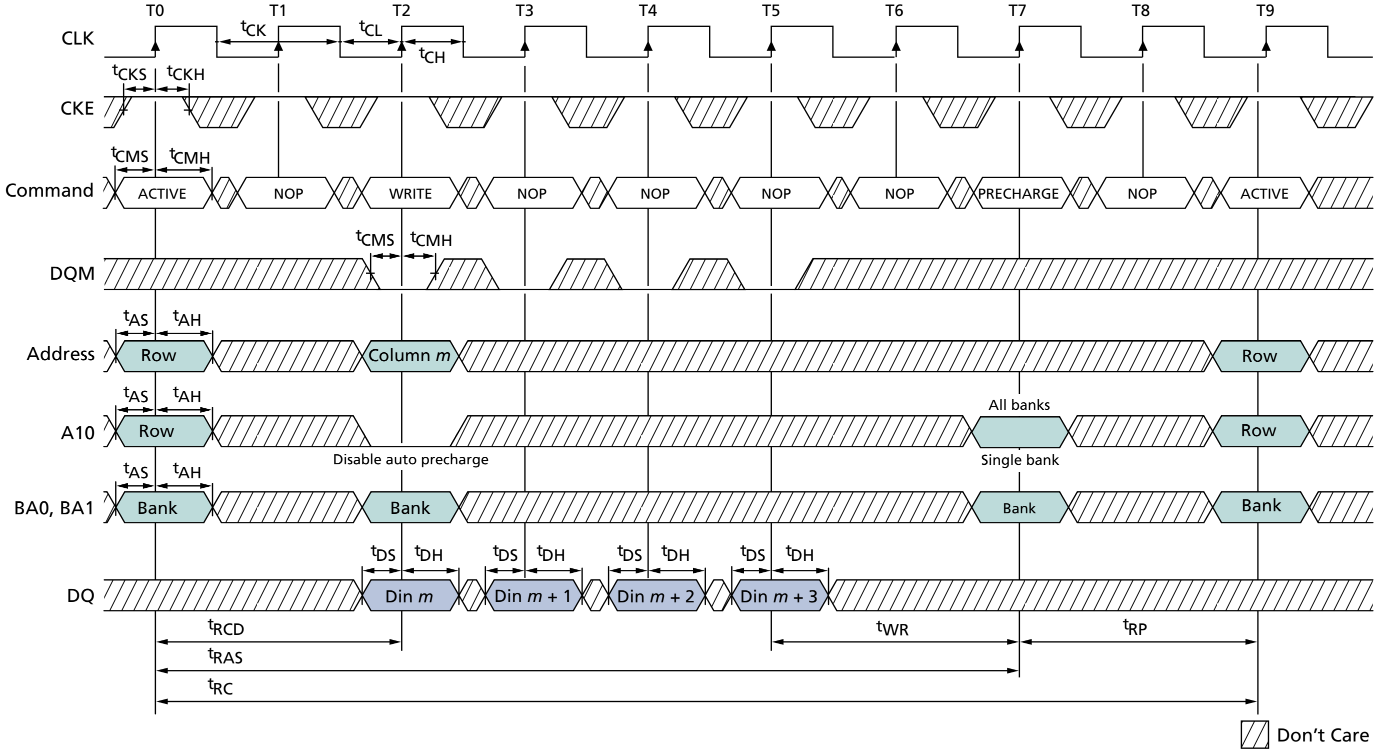
Notes: 1. DQM is LOW.

Figure 44: **WRITE With Auto Precharge**


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
NOP
ACTIVE
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
Row
tAS
tAH
Enable auto precharge
A10
Row
Row
tAS
tAH
BA0, BA1
Bank
Bank
Bank
tDS
tDH
tDS
tDH
tDS
tDH
tDS
tDH
DQ
Din m
Din m + 1
Din m + 2
Din m + 3
tRCD
tWR
tRP
tRAS
tRC
Don't Care

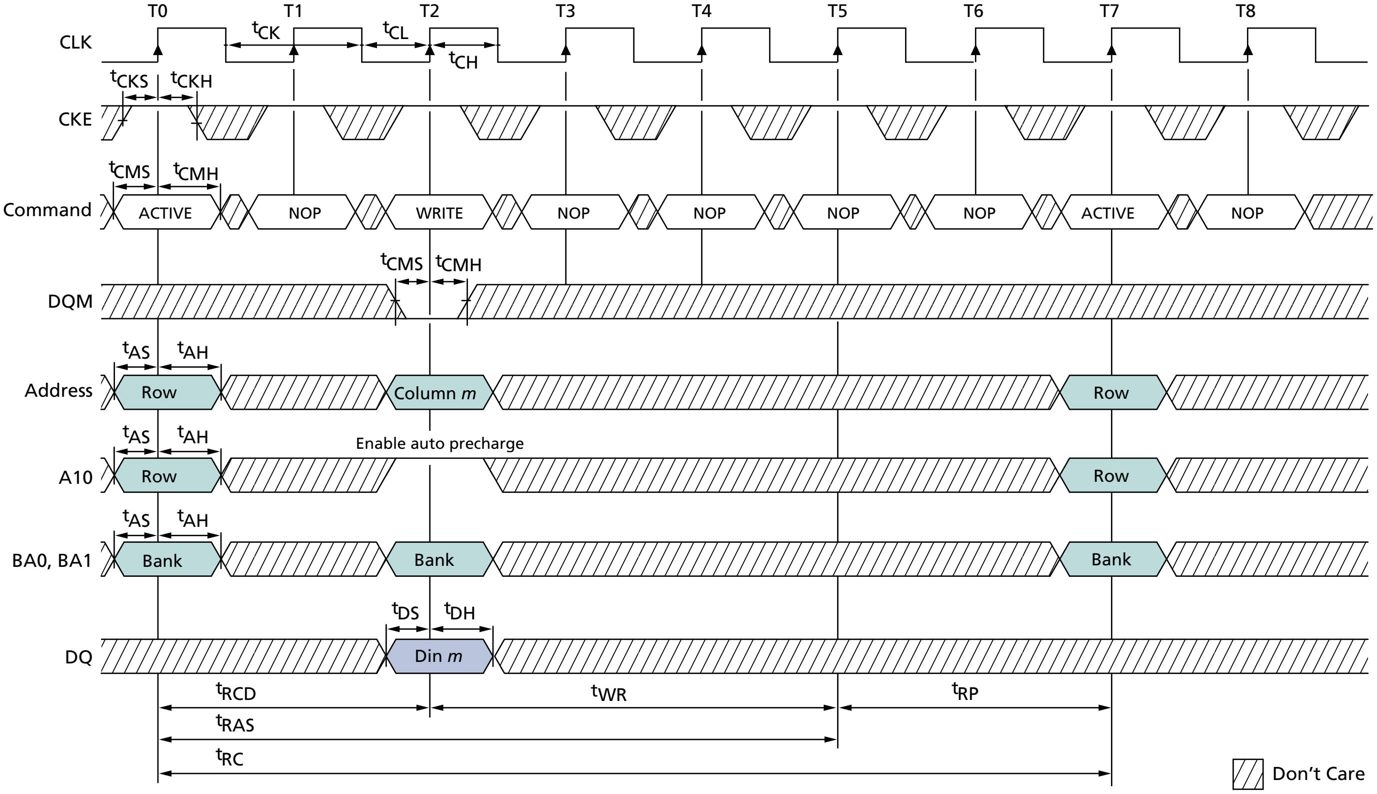
Notes: 1. For this example, BL = 4.

Figure 45: WRITE Without Auto Precharge


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
WRITE
NOP
NOP
NOP
NOP
PRECHARGE
NOP
ACTIVE
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
Row
tAS
tAH
A10
Row
All banks
Row
Disable auto precharge
Single bank
tAS
tAH
BA0, BA1
Bank
Bank
Bank
Bank
tDS
tDH
DQ
Din m
Din m + 1
Din m + 2
Din m + 3
tRCD
tWR
tRP
tRAS
tRC
Don’t Care

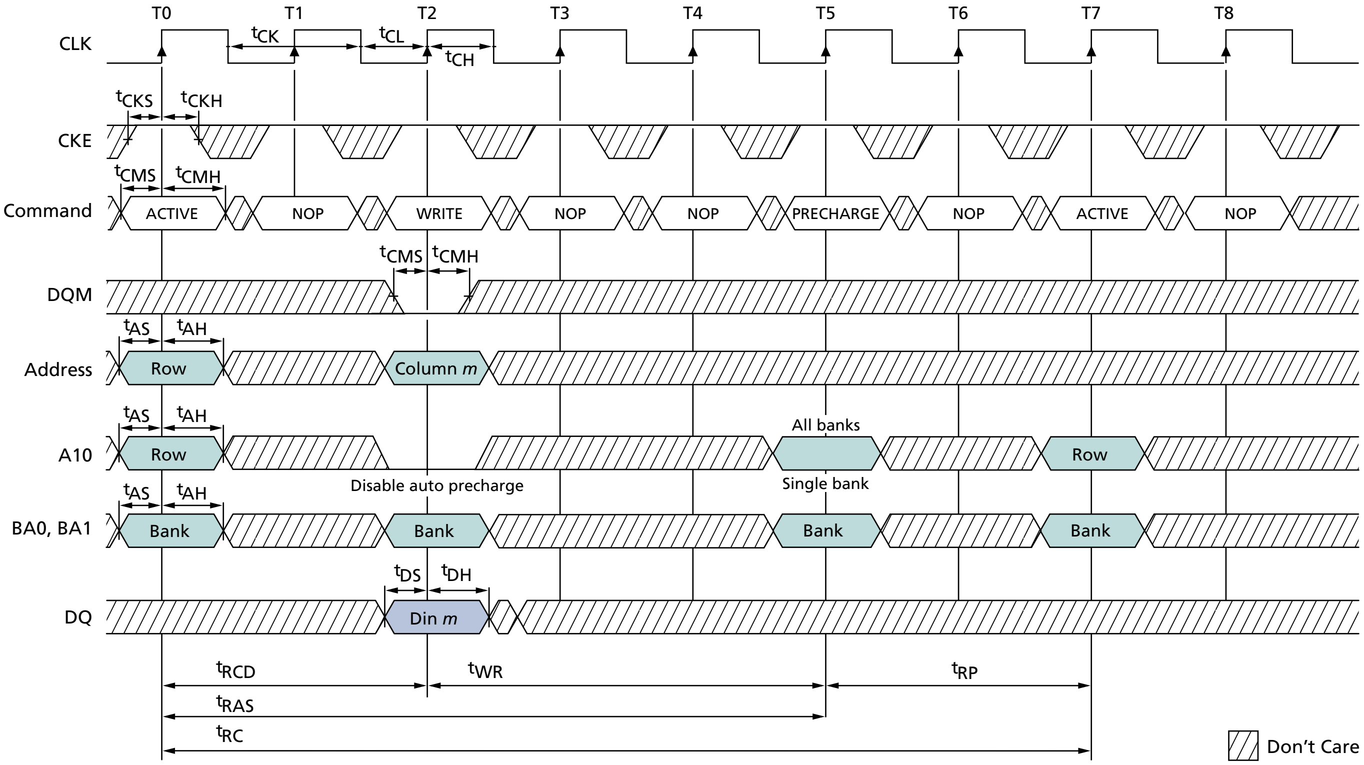
Notes: 1. For this example, BL = 4 and the WRITE burst is followed by a manual PRECHARGE.

Figure 46: Single WRITE With Auto Precharge


T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
WRITE
NOP
NOP
NOP
NOP
ACTIVE
NOP
tCMS
tCMH
DQM
tAS
tAH
Address
Row
Column m
Row
tAS
tAH
Enable auto precharge
A10
Row
Row
tAS
tAH
BA0, BA1
Bank
Bank
Bank
tDS
tDH
DQ
Din m
tRCD
tWR
tRP
tRAS
tRC
Don't Care

Notes: 1. For this example, BL = 1.

Figure 47: Single WRITE Without Auto Precharge


T0
T1
T2
T3
T4
T5
T6
T7
T8
CLK
tCK
tCL
tCH
tCKS
tCKH
CKE
tCMS
tCMH
Command
ACTIVE
NOP
WRITE
NOP
NOP
PRECHARGE
NOP
ACTIVE
NOP
DQM
Address
tAS
tAH
Row
Column m
A10
Row
All banks
Row
Disable auto precharge
Single bank
BA0, BA1
Bank
Bank
Bank
Bank
DQ
tDS
tDH
Din m
tRCD
tWR
tRP
tRAS
tRC
Don't Care

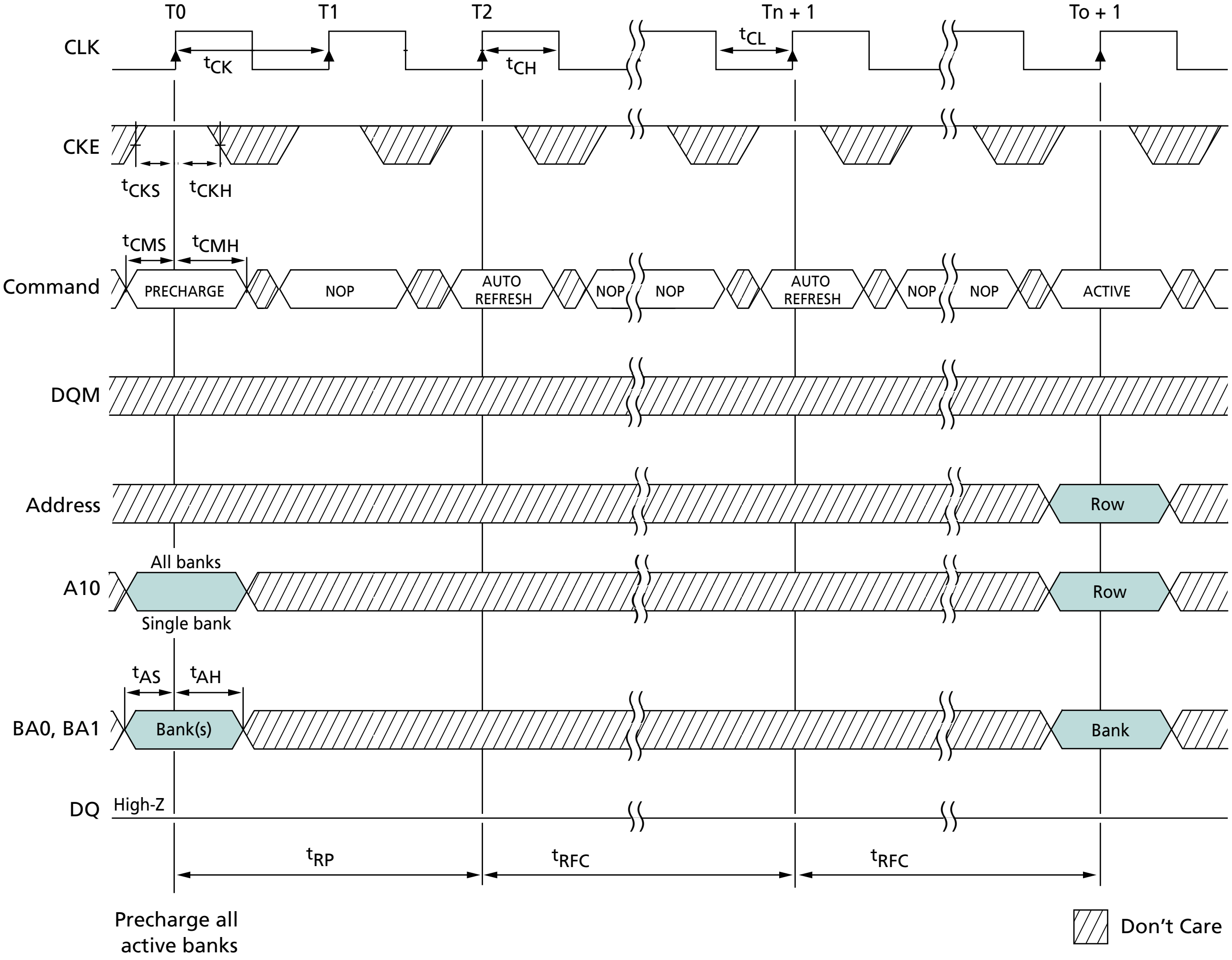
Notes: 1. For this example, BL = 1 and the WRITE burst is followed by a manual PRECHARGE.

AUTO REFRESH

The AUTO REFRESH command is used during normal operation of the SDRAM to refresh the contents of the SDRAM array. This command is non persistent, so it must be issued each time a refresh is required. All active banks must be precharged prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP is met following the PRECHARGE command. Addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command.

After the AUTO REFRESH command is initiated, it must not be interrupted by any executable command until ^{t}RFC has been met. During ^{t}RFC time, COMMAND INHIBIT or NOP commands must be issued on each positive edge of the clock. The SDRAM requires that every row be refreshed each ^{t}REF period. Providing a distributed AUTO REFRESH command—calculated by dividing the refresh period (^{t}REF) by the number of rows to be refreshed—meets the timing requirement and ensures that each row is refreshed. Alternatively, a burst refresh can be employed after every ^{t}REF period—by issuing consecutive AUTO REFRESH commands for the number of rows to be refreshed at the minimum cycle rate (^{t}RFC)—to satisfy the refresh requirement.

Figure 48: Auto Refresh Mode


T0
T1
T2
Tn + 1
To + 1
CLK
^tCK
^tCH
^tCL
CKE
^tCKS
^tCKH
^tCMS
^tCMH
Command
PRECHARGE
NOP
AUTO REFRESH
NOP
NOP
AUTO REFRESH
NOP
NOP
ACTIVE
DQM
Address
Row
A10
All banks
Single bank
Row
^tAS
^tAH
BA0, BA1
Bank(s)
Bank
DQ
High-Z
^tRP
^tRFC
^tRFC
Precharge all active banks
Don't Care

Notes: 1. Back-to-back AUTO REFRESH commands are not required.

Self Refresh

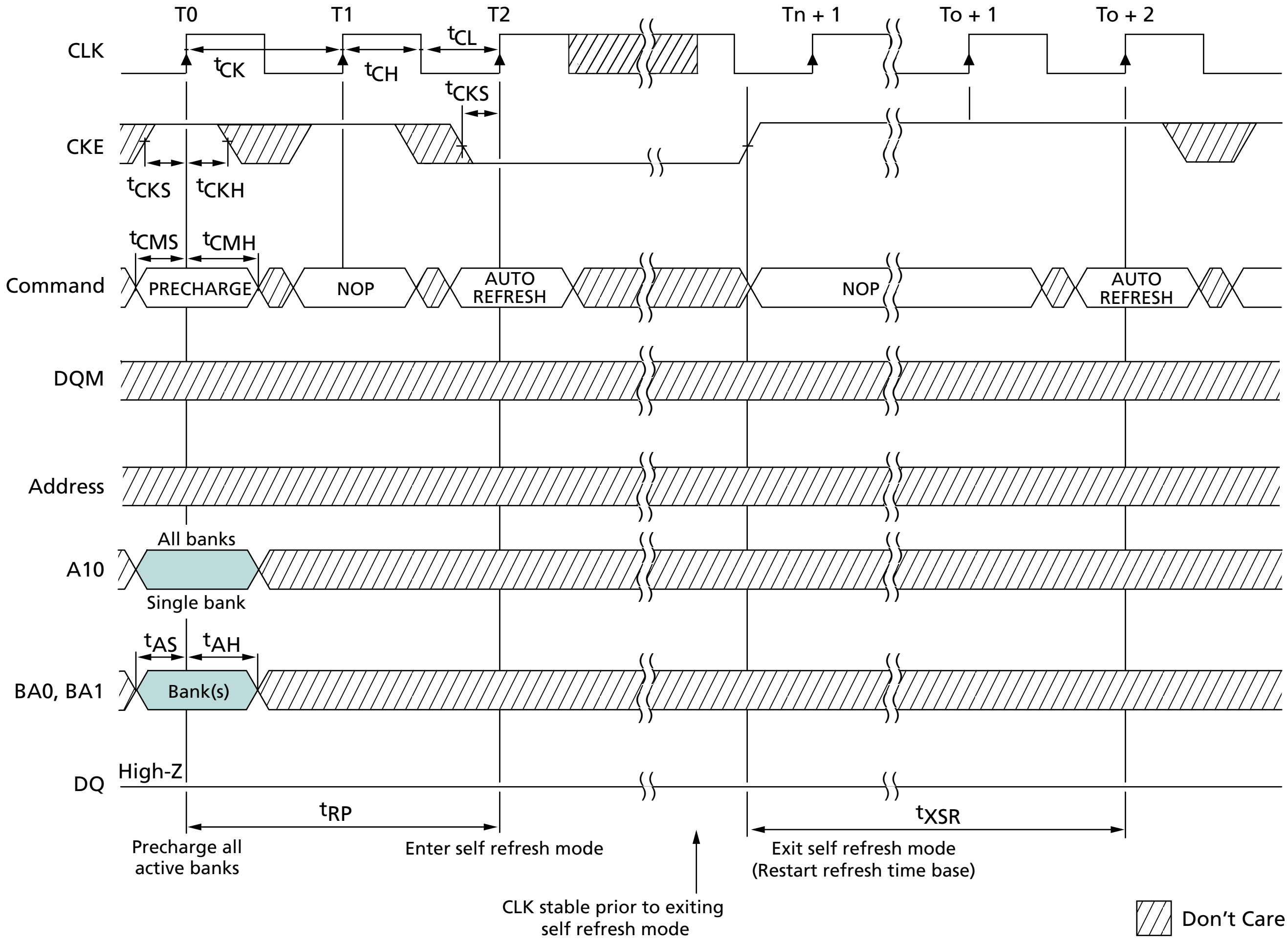
The self refresh mode can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don't Care” with the exception of CKE, which must remain LOW.

After self refresh mode is engaged, the SDRAM provides its own internal clocking, enabling it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and remains in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) prior to CKE going back HIGH. After CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued according to the distributed refresh rate (^{t}REF/refresh row count) as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

Figure 49: Self Refresh Mode


T0
T1
T2
Tn + 1
To + 1
To + 2
CLK
tCK
tCH
tCL
tCKS
CKE
tCKS
tCKH
tCMS
tCMH
Command
PRECHARGE
NOP
AUTO REFRESH
NOP
AUTO REFRESH
DQM
Address
A10
All banks
Single bank
tAS
tAH
BA0, BA1
Bank(s)
DQ
High-Z
tRP
tXSR
Precharge all active banks
Enter self refresh mode
CLK stable prior to exiting self refresh mode
Exit self refresh mode (Restart refresh time base)
Don't Care

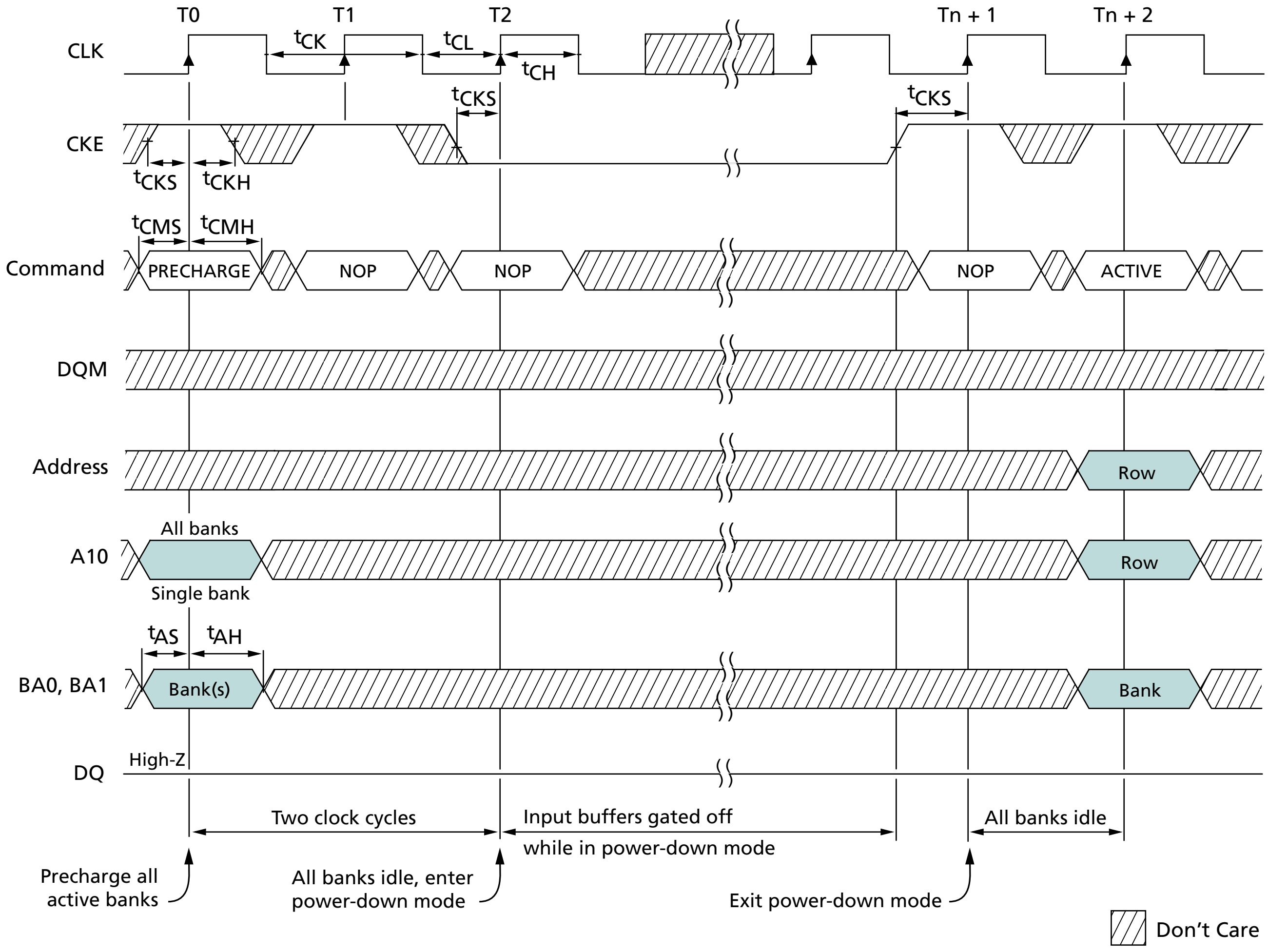
Notes: 1. Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required.

Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device cannot remain in the power-down state longer than the refresh period (64ms) as no REFRESH operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT with CKE HIGH at the desired clock edge (meeting ^{t}CKS), (see Figure 50).

Figure 50: Power-Down Mode


T0
T1
T2
Tn + 1
Tn + 2
CLK
tCK
tCL
tCH
tCKS
CKE
tCKS
tCKH
tCMS
tCMH
Command
PRECHARGE
NOP
NOP
NOP
ACTIVE
DQM
Address
Row
A10
All banks
Single bank
Row
tAS
tAH
BA0, BA1
Bank(s)
Bank
High-Z
DQ
Two clock cycles
Input buffers gated off
while in power-down mode
All banks idle
Precharge all
active banks
All banks idle, enter
power-down mode
Exit power-down mode
Don't Care

Notes: 1. Violating refresh requirements during power-down may result in a loss of data.

Deep Power-Down

Deep power-down mode is a maximum power-saving feature achieved by shutting off the power to the entire device memory array. Data on the memory array will not be retained after deep power-down mode is executed. Deep power-down mode is entered by having all banks idle, with CS# and WE# held LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during deep power-down.

To exit deep power-down mode, CKE must be asserted HIGH. Upon exiting deep power-down mode, a full initialization sequence is required.

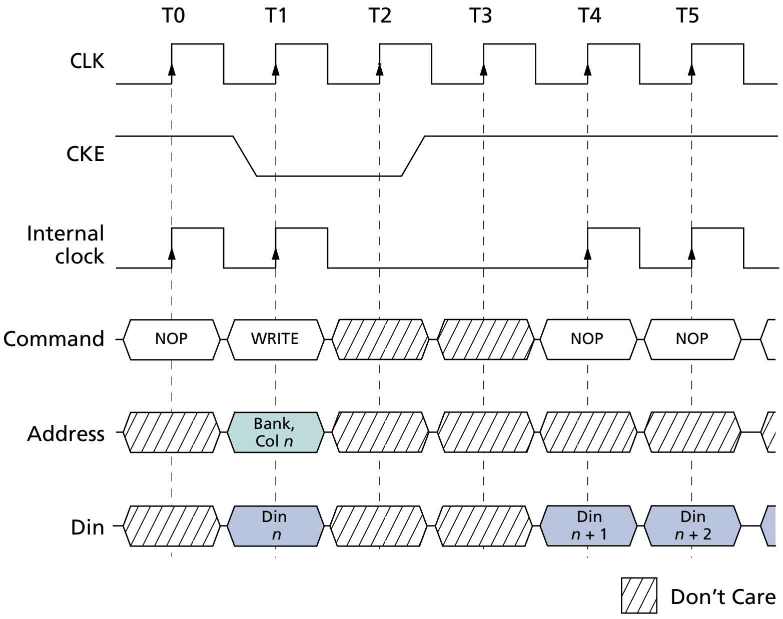
Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input balls when an internal clock edge is suspended will be ignored; any data present on the DQ balls remains driven; and burst counters are not incremented, as long as the clock is suspended (see examples in Figure 51, and Figure 52 on page 71).

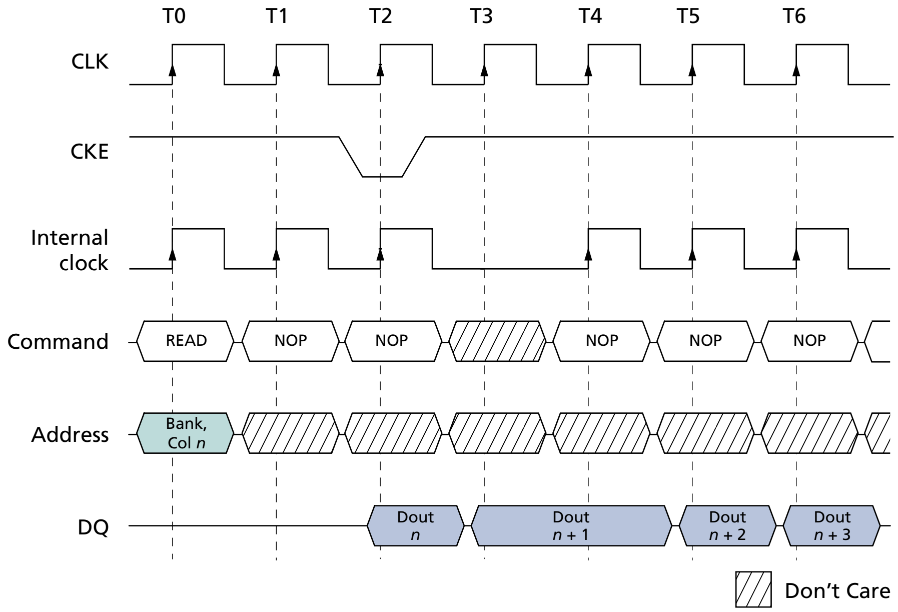
Exit clock suspend mode by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

Figure 51: Clock Suspend During WRITE Burst



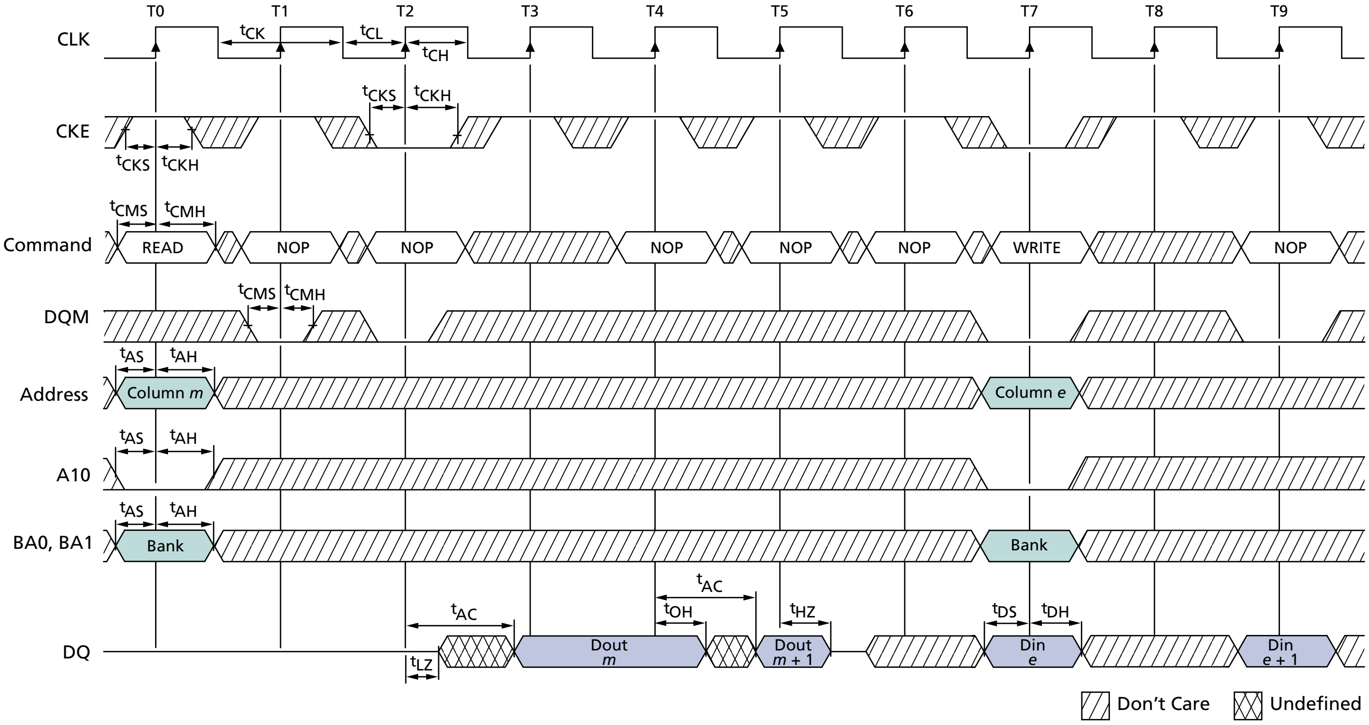
Notes: 1. For this example, BL = 4 or greater, and DQM is LOW.

Figure 52: Clock Suspend During READ Burst


T0
T1
T2
T3
T4
T5
T6
CLK
CKE
Internal clock
Command
READ
NOP
NOP
NOP
NOP
NOP
Address
Bank, Col n
DQ
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Don't Care

Notes: 1. For this example, CL = 2, BL = 4 or greater, and DQM is LOW.

Figure 53: Clock Suspend Mode


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
CLK
tCK
tCL
tCH
CKE
tCKS
tCKH
Command
tCMS
tCMH
READ
NOP
NOP
NOP
NOP
NOP
WRITE
NOP
DQM
Address
tAS
tAH
Column m
Column e
A10
BA0, BA1
Bank
Bank
DQ
tAC
tLZ
tOH
tHZ
tDS
tDH
Dout m
Dout m + 1
Din e
Din e + 1
Don't Care
Undefined

Notes: 1. For this example, BL = 2, CL = 3, and auto precharge is disabled.

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Revision History: Commands, Operations, and Timing Diagrams

Update **10/08**

- "Deep Power-Down" on page 69: Added description for exiting DPD.

Update **7/08**

- Updated address/data range presentation to industry-standard presentation.
- Replaced "MODE REGISTER SET" with "LMR" as appropriate.
- Table 17, "Truth Table – Current State Bank n, Command to Bank m," on page 30, Note 13: added missing "*m*."
- "Mode Register" on page 34: Corrected presentation of mode register bits.
- "Partial-Array Self Refresh (PASR)" on page 38: Updated refresh options presentation.

Update **5/08**

- "Auto Precharge" on page 55: Added fourth paragraph regarding ^{t}RAS lock-out.
- Figure 40: "Single READ With Auto Precharge," on page 60: Updated figure.
- Figure 45: "WRITE Without Auto Precharge," on page 64: Updated note to BL = 4.
- Figure 46: "Single WRITE With Auto Precharge," on page 65: Updated figure.
- Figure 47: "Single WRITE Without Auto Precharge," on page 66: Updated figure.

Update **4/08**

- Added three-quarter drive strength content.

Revision History: Device

Rev. D, Production **2/09**

- Deleted ball out columns from Table 3, page 10.
- Updated values in Tables 7 and 8, page 15.
- Corrected typographical error in heading of Table 11, page 17.

Rev. C, Production **12/08**

- “Options” on page 1: Added Low-power option.
- Figure 1 on page 5: Added low-power option.
- Table 9, “IDD7 Specifications and Conditions (x16 and x32),” on page 15: Added column with values for Low-power option.

Rev. B, Preliminary **4/08**

- Table 7, “IDD Specifications and Conditions (x16),” on page 14: Updated Idd values and changed Idd5 auto refresh current to ^{t}RFC = 110ns.
- Table 8, “Idd Specifications and Conditions (x32),” on page 14: Updated Idd values and changed Idd5 auto refresh current to ^{t}RFC = 110ns
- Figure 8, Typical Idd7 Curves, on page 15: Added figure.
- Table 10, “Electrical Characteristics and Recommended AC Operating Conditions,” on page 16: Updated values for ^{t}CH, ^{t}CL.
- Table 12, “Target Output Drive Characteristics (Full Strength),” on page 19, Table 13, “Target Output Drive Characteristics (Three-Quarter Strength),” on page 20, and Table 14, “Target Output Drive Characteristics (One-Half Strength),” on page 21: Added drive-strength tables.

Rev. A, Advance **10/07**

- Initial release.