

DDR2 SDRAM SODIMM

MT16HTF12864H – 1GB
MT16HTF25664H – 2GB

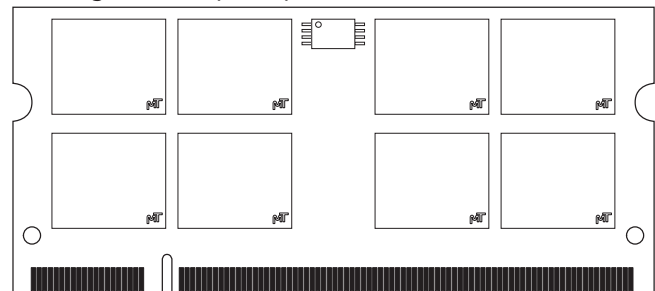
For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 200-pin, small outline dual in-line memory module (SODIMM)
- Fast data transfer rates: PC2-3200, PC2-4200, PC2-5300, or PC2-6400.
- 1GB (128 Meg x 64), 2GB (256 Meg x 64)
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 t_{CK}
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Dual rank

Figure 1: 200-Pin SODIMM (MO-224 R/C E)

PCB height: 30mm (1.18in)



Options

- Operating temperature¹
- Commercial ($0^{\circ}C \leq T_C \leq +70^{\circ}C$)
- Industrial ($-40^{\circ}C \leq T_C \leq +85^{\circ}C$)
- Package
 - 200-pin DIMM (Pb-free)
- Frequency/CAS latency
 - 2.5ns @ CL = 5 (DDR2-800)
 - 2.5ns @ CL = 6 (DDR2-800)
 - 3ns @ CL = 5 (DDR2-667)
 - 3.75ns @ CL = 4 (DDR2-533)
 - 5.0ns @ CL = 3 (DDR2-400)²
- PCB height
 - 30mm (1.18in)

Marking

None
I
Y
-80E
-800
-667
-53E
-40E

Notes: 1. Contact Micron for industrial temperature module offerings.

2. Not recommended for new designs.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)				t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 6	CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	–	800	533	–	12.5	12.5	55
-800	PC2-6400	800	667	533	–	15	15	55
-667	PC2-5300	–	667	533	400	15	15	55
-53E	PC2-4200	–		533	400	15	15	55
-40E	PC2-3200	–		400	400	15	15	55



1GB, 2GB (x64, DR) 200-Pin DDR2 SDRAM SODIMM Features

Table 2: Addressing

Parameter	1GB	2GB
Refresh count	8K	8K
Row address	16K (A0–A13)	16K (A0–A13)
Device bank address	4 (BA0, BA1)	8 (BA0–BA2)
Device page size per bank	1KB	1KB
Device configuration	512Mb (64 Meg x 8)	1Gb (128 Meg x 8)
Column address	1K (A0–A9)	1K (A0–A9)
Module rank address	2 (S0#, S1#)	2 (S0#, S1#)

Table 3: Part Numbers and Timing Parameters – 1GB Modules

Base device: MT47H64M8,¹ 512Mb DDR2 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT16HTF12864HY-80E__	1GB	128 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT16HTF12864HY-800__	1GB	128 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT16HTF12864HY-667__	1GB	128 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTF12864HY-53E__	1GB	128 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT16HTF12864HY-40E__	1GB	128 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

Table 4: Part Numbers and Timing Parameters – 2GB Modules

Base device: MT47H128M8,¹ 1Gb DDR2 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL- ^t RCD- ^t RP)
MT16HTF25664HY-80E__	2GB	256 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	5-5-5
MT16HTF25664HY-800__	2GB	256 Meg x 64	6.4 GB/s	2.5ns/800 MT/s	6-6-6
MT16HTF25664HY-667__	2GB	256 Meg x 64	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT16HTF25664HY-53E__	2GB	256 Meg x 64	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT16HTF25664HY-40E__	2GB	256 Meg x 64	3.2 GB/s	5.0ns/400 MT/s	3-3-3

- Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown) designating component and PCB revisions. Consult factory for current revision codes. Example: MT16HTF12864HY-40ED3.



1GB, 2GB (x64, DR) 200-Pin DDR2 SDRAM SODIMM Module Pin Assignments and Descriptions

Module Pin Assignments and Descriptions

Table 5: Pin Assignments

200-Pin SODIMM Front								200-Pin SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	DQS2	101	A1	151	DQ42	2	Vss	52	DM2	102	A0	152	DQ46
3	Vss	53	Vss	103	VDD	153	DQ43	4	DQ4	54	Vss	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10	155	Vss	6	DQ5	56	DQ22	106	BA1	156	Vss
7	DQ1	57	DQ19	107	BA0	157	DQ48	8	Vss	58	DQ23	108	RAS#	158	DQ52
9	Vss	59	Vss	109	WE#	159	DQ49	10	DM0	60	Vss	110	SO#	160	DQ53
11	DQS0#	61	DQ24	111	VDD	161	Vss	12	Vss	62	DQ28	112	VDD	162	Vss
13	DQS0	63	DQ25	113	CAS#	163	NC	14	DQ6	64	DQ29	114	ODT0	164	CK1
15	Vss	65	Vss	115	S1#	165	Vss	16	DQ7	66	Vss	116	A13	166	CK1#
17	DQ2	67	DM3	117	VDD	167	DQS6#	18	Vss	68	DQS3#	118	VDD	168	Vss
19	DQ3	69	NC	119	ODT1	169	DQS6	20	DQ12	70	DQS3	120	NC	170	DM6
21	Vss	71	Vss	121	Vss	171	Vss	22	DQ13	72	Vss	122	Vss	172	Vss
23	DQ8	73	DQ26	123	DQ32	173	DQ50	24	Vss	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51	26	DM1	76	DQ31	126	DQ37	176	DQ55
27	Vss	77	Vss	127	Vss	177	Vss	28	Vss	78	Vss	128	Vss	178	Vss
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56	30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57	32	CK0#	82	VDD	132	Vss	182	DQ61
33	Vss	83	NC	133	Vss	183	Vss	34	Vss	84	NC	134	DQ38	184	Vss
35	DQ10	85 ¹	NC/BA2	135	DQ34	185	DM7	36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	VDD	137	DQ35	187	Vss	38	DQ15	88	VDD	138	Vss	188	DQS7
39	Vss	89	A12	139	Vss	189	DQ58	40	Vss	90	A11	140	DQ44	190	Vss
41	Vss	91	A9	141	DQ40	191	DQ59	42	Vss	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	Vss	44	DQ20	94	A6	144	Vss	194	DQ63
45	DQ17	95	VDD	145	Vss	195	SDA	46	DQ21	96	VDD	146	DQS5#	196	Vss
47	Vss	97	A5	147	DM5	197	SCL	48	Vss	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	Vss	199	VDDSPD	50	NC	100	A2	150	Vss	200	SA1

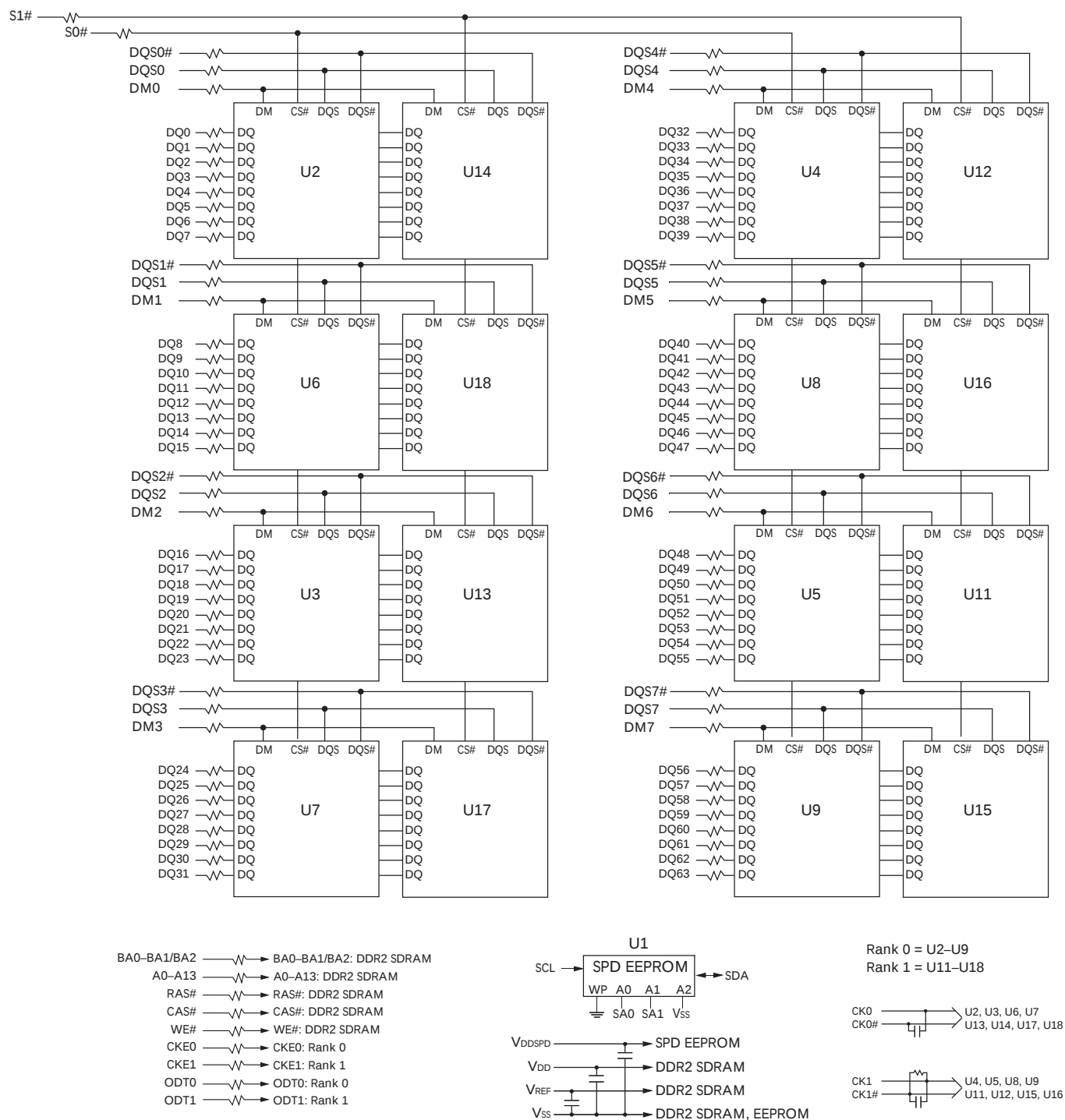
Notes: 1. Pin 85 is NC for 1GB and BA2 for 2GB.

Table 6: Pin Descriptions

Symbol	Type	Description
ODT0, ODT1	Input (SSTL_18)	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
CK0, CK0# CK1, CK1#	Input (SSTL_18)	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0, CKE1	Input (SSTL_18)	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
S0#, S1#	Input (SSTL_18)	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
RAS#, CAS#, WE#	Input (SSTL_18)	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
BA0–BA2	Input (SSTL_18)	Bank address inputs: BA0–BA1/BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1/BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command. BA0, BA0 (1GB), BA0–BA2 (2GB)
A0–A13	Input (SSTL_18)	Address inputs: Provide the row address for ACTIVE commands and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1/BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
DM0–DM7 (DQS9–DQS17)	Input (SSTL_18)	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. If RDQS is disabled, DQS9–DQS17 become DM0–DM8 and DQS9#–DQS17# are not used.
SCL	Input (SSTL_18)	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0–SA1	Input (SSTL_18)	Presence-detect address inputs: These pins are used to configure the presence-detect device.
DQ0–DQ63	I/O (SSTL_18)	Data input/output: Bidirectional data bus.
DQS0–DQS7, DQS0#–DQS7#	I/O (SSTL_18)	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O (SSTL_18)	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
VDD	Supply	Power supply: +1.8V ±0.1V.
VREF	Supply	SSTL_18 reference voltage. VDD/2.
VSS	Supply	Ground.
VDDSPD	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
NC	–	No connect: These pins should be left unconnected.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT16HTF12864H and MT16HTF25664H DDR2 SDRAM modules are high-speed, CMOS, dynamic random-access 1GB and 2GB memory modules organized in a x64 configuration. These DDR2 SDRAM modules use internally configured 4-bank (512Mb) or 8-bank (1Gb) DDR2 SDRAM devices.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a $4n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single $4n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during reads and by the memory controller during writes. DQS is edge-aligned with data for reads and center-aligned with data for writes.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes are programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (1:0), which provide four unique DIMM/EEPROM addresses. Write protect (WP) is tied to VSS on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 7 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in the device data sheet are not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 7: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Units
VDD	VDD supply voltage relative to Vss		−1.0	+2.3	V
VIN, VOUT	Voltage on any pin relative to Vss		−0.5	+2.3	V
II	Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; VREF input $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#	−80	+80	μA
		S#, CKE, ODT, CK, CK#	−40	+40	
		DM	−10	+10	
IOZ	Output leakage current; $0V \leq V_{OUT}$; DQs and ODT are disabled	DQ, DQS, DQS#	−10	+10	μA
IVREF	VREF leakage current; VREF = valid VREF level		−32	+32	μA
TA	Module ambient operating temperature	Commercial	0	+70	°C
		Industrial	−40	+85	°C
TC ¹	DDR2 SDRAM component case operating temperature ²	Commercial	0	+85	°C
		Industrial	−40	+95	°C

- Notes: 1. The refresh rate is required to double when 85°C < T_C ≤ 95°C.
2. For further information, refer to technical note TN-00-08: Thermal Applications, available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 8.

Table 8: Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-80E	-25E
-800	-25
-667	-3
-53E	-37E
-40E	-53E

IDD Specifications

Table 9: DDR2 IDD Specifications and Conditions – 1GB

Values shown for MT47H64M8 DDR2 SDRAM only and are computed from values specified in the 512Mb (64 Meg x 8) component data sheet

Parameter/Condition		Symbol	-80E/-800	-667	-53E	-40E	Units
Operating one bank active-precharge current: $t_{CK} = t_{CK} (I_{DD})$, $t_{RC} = t_{RC} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD0}^1	856	776	696	696	mA
Operating one bank active-read-precharge current: $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (I _{DD}), AL = 0; $t_{CK} = t_{CK} (I_{DD})$, $t_{RC} = t_{RC} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$, $t_{RCD} = t_{RCD} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I _{DD} 4W		I_{DD1}^1	976	896	816	776	mA
Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2P}^2	112	112	112	112	mA
Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating		I_{DD2Q}^2	800	720	640	560	mA
Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD2N}^2	880	800	720	640	mA
Active power-down current: All device banks open; $t_{CK} = t_{CK} (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	I_{DD3P}^2	640	560	480	400	mA
	Slow PDN exit MR[12] = 1		192	192	192	192	mA
Active standby current: All device banks open; $t_{CK} = t_{CK} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$, $t_{RP} = t_{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD3N}^2	1,120	1,040	880	720	mA
Operating burst write current: All device banks open; continuous burst writes; BL = 4, CL = CL (I _{DD}), AL = 0; $t_{CK} = t_{CK} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$, $t_{RP} = t_{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4W}^1	1,616	1,416	1,176	976	mA
Operating burst read current: All device banks open; continuous burst reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (I _{DD}), AL = 0; $t_{CK} = t_{CK} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$, $t_{RP} = t_{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching		I_{DD4R}^1	1,696	1,496	1,216	976	mA
Burst refresh current: $t_{CK} = t_{CK} (I_{DD})$; REFRESH command at every $t_{RFC} (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching		I_{DD5}^2	3,680	2,880	2,720	2,640	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating		I_{DD6}^2	112	112	112	112	mA
Operating bank interleave read current: All device banks interleaving reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (I _{DD}), AL = $t_{RCD} (I_{DD}) - 1 \times t_{CK} (I_{DD})$; $t_{CK} = t_{CK} (I_{DD})$, $t_{RC} = t_{RC} (I_{DD})$, $t_{RRD} = t_{RRD} (I_{DD})$, $t_{RCD} = t_{RCD} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching		I_{DD7}^1	2,456	1,976	1,856	1,816	mA

- Notes:
- Value calculated as one module rank in this operating condition; all other module ranks in $IDD2P$ (CKE LOW) mode.
 - Value calculated reflects all module ranks in this operating condition.

Table 10: DDR2 I_{DD} Specifications and Conditions – 2GB

Values shown for MT47H128M8 DDR2 SDRAM only and are computed from values specified in the 1Gb (128 Meg x 8) component data sheet

Parameter/Condition	Symbol	-80E/-800	-667	-53E	-40E	Units
Operating one bank active-precharge current: $t_{CK} = t_{CK} (I_{DD})$, $t_{RC} = t_{RC} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD0}^1	776	736	616	616	mA
Operating one bank active-read-precharge current: $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (I _{DD}), AL = 0; $t_{CK} = t_{CK} (I_{DD})$, $t_{RC} = t_{RC} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MIN} (I_{DD})$, $t_{RCD} = t_{RCD} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as I _{DD4W}	I_{DD1}^1	936	856	816	776	mA
Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2P}^2	112	112	112	112	mA
Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD2Q}^2	800	640	640	560	mA
Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (I_{DD})$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD2N}^2	800	640	640	560	mA
Active power-down current: All device banks open; $t_{CK} = t_{CK} (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{DD3P}^2	Fast PDN exit MR[12] = 0	640	480	480	mA
		Slow PDN exit MR[12] = 1	160	160	160	mA
Active standby current: All device banks open; $t_{CK} = t_{CK} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$, $t_{RP} = t_{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD3N}^2	960	880	720	640	mA
Operating burst write current: All device banks open; continuous burst writes; BL = 4, CL = CL (I _{DD}), AL = 0; $t_{CK} = t_{CK} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$, $t_{RP} = t_{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4W}^1	1,336	1,136	1,056	896	mA
Operating burst read current: All device banks open; continuous burst reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (I _{DD}), AL = 0; $t_{CK} = t_{CK} (I_{DD})$, $t_{RAS} = t_{RAS} \text{ MAX} (I_{DD})$, $t_{RP} = t_{RP} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	I_{DD4R}^1	1,336	1,136	1,056	896	mA
Burst refresh current: $t_{CK} = t_{CK} (I_{DD})$; REFRESH command at every $t_{RFC} (I_{DD})$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	I_{DD5}^2	3,760	3,440	3,360	3,280	mA
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I_{DD6}^2	112	112	112	112	mA
Operating bank interleave read current: All device banks interleaving reads; $I_{OUT} = 0\text{mA}$; BL = 4, CL = CL (I _{DD}), AL = $t_{RCD} (I_{DD}) - 1 \times t_{CK} (I_{DD})$; $t_{CK} = t_{CK} (I_{DD})$, $t_{RC} = t_{RC} (I_{DD})$, $t_{RRD} = t_{RRD} (I_{DD})$, $t_{RCD} = t_{RCD} (I_{DD})$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselections; Data bus inputs are switching	I_{DD7}^1	2,736	2,296	2,216	2,136	mA

- Notes:
- Value calculated as one module rank in this operating condition; all other module ranks in I_{DD2P} (CKE LOW) mode.
 - Value calculated reflects all module ranks in this operating condition.

Serial Presence-Detect

Table 11: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V _{DDSPD}	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V _{IH}	V _{DDSPD} × 0.7	V _{DDSPD} + 0.5	V
Input low voltage: Logic 0; All inputs	V _{IL}	−0.6	V _{DDSPD} × 0.3	V
Output low voltage: I _{OUT} = 3mA	V _{OL}	−	0.4	V
Input leakage current: V _{IN} = GND to V _{DD}	I _{LI}	0.10	3	μA
Output leakage current: V _{OUT} = GND to V _{DD}	I _{LO}	0.05	3	μA
Standby current	I _{SB}	1.6	4	μA
Power supply current, READ: SCL clock frequency = 100 kHz	I _{CC_R}	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I _{CC_W}	2	3	mA

Table 12: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	t _{AA}	0.2	0.9	μs	1
Time the bus must be free before a new transition can start	t _{BUF}	1.3	−	μs	
Data-out hold time	t _{DH}	200	−	ns	
SDA and SCL fall time	t _F	−	300	ns	2
Data-in hold time	t _{HD:DAT}	0	−	μs	
Start condition hold time	t _{HD:STA}	0.6	−	μs	
Clock HIGH period	t _{HIGH}	0.6	−	μs	
Noise suppression time constant at SCL, SDA inputs	t _I	−	50	ns	
Clock LOW period	t _{LOW}	1.3	−	μs	
SDA and SCL rise time	t _R	−	0.3	μs	2
SCL clock frequency	f _{SCL}	−	400	kHz	
Data-in setup time	t _{SU:DAT}	100	−	ns	
Start condition setup time	t _{SU:STA}	0.6	−	μs	3
Stop condition setup time	t _{SU:STO}	0.6	−	μs	
WRITE cycle time	t _{WRC}	−	10	ms	4

- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a restart condition, or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Table 13: Serial Presence-Detect Matrix

Byte	Description	Entry (Version)	1GB	2GB
0	Number of SPD bytes used by Micron	128	80	80
1	Total Number of bytes in SPD device	256	08	08
2	Fundamental memory type	DDR2 SDRAM	08	08
3	Number of row addresses on assembly	14	0E	0E
4	Number of column addresses on assembly	10	0A	0A
5	DIMM height and module ranks	30mm, dual rank	61	61
6	Module data width	64	40	40
7	Reserved	0	00	00
8	Module voltage interface levels	SSTL 1.8V	05	05
9	SDRAM cycle time, t_{CK} (CL = maximum value, see byte 18)	-80E/-800 -667 -53E -40E	25 30 3D 50	25 30 3D 50
10	SDRAM access from clock, t_{AC} (CL = maximum value, see byte 18)	-80E/-800 -667 -53E -40E	40 45 50 60	40 45 50 60
11	Module configuration type	Non-ECC	00	00
12	Refresh rate/type	7.81 μ s/SELF	82	82
13	SDRAM device width (primary SDRAM)	8	08	08
14	Error-checking SDRAM data width	n/a	00	00
15	Reserved	0	00	00
16	Burst lengths supported	4, 8	0C	0C
17	Number of banks on SDRAM device	4 or 8	04	08
18	CAS latencies supported	-80E (5, 4) -800 (6, 5, 4) -667 (5, 4, 3) -53E/-40E (4, 3)	30 70 38 18	30 70 38 18
19	Module thickness		01	01
20	DDR2 DIMM type	SODIMM	04	04
21	SDRAM module attributes	No PLL or Reg	00	00
22	SDRAM device attributes: Weak driver (01) and 50 Ω ODT (03)	-800/-80E/-667 -53E/-40E	03 01	03 01
23	SDRAM cycle time, t_{CK} , MAX CL - 1	-80E/-667 -800 -53E/-40E	3D 30 50	3D 30 50
24	SDRAM access from CK, t_{AC} , MAX CL - 1	-80E/-800 -667 -53E -40E	40 45 50 60	40 45 50 60
25	SDRAM cycle time, t_{CK} , MAX CL - 2	-80E -800 -667 -53E/-40E	00 3D 50 00	00 3D 50 00
26	SDRAM access from CK, t_{AC} , MAX CL - 2	-80E -800 -667 -53E/-40E	00 40 45 00	00 40 45 00

Table 13: Serial Presence-Detect Matrix (continued)

Byte	Description	Entry (Version)	1GB	2GB
27	MIN row precharge time, t_{RP}	-80E -800/-667-53E/-40E	32 3C	32 3C
28	MIN row active-to-row active, t_{RRD}		1E	1E
29	MIN RAS#-to-CAS# delay, t_{RCD}	-80E -800/-667-53E/-40E	32 3C	32 3C
30	MIN active-to-active precharge time, t_{RAS}	-800/-80E/-667/-53E -40E	2D 28	2D 28
31	Module rank density	512MB, 1GB	80	01
32	Address and command setup time, t_{IS_b}	-800/-80E -667 -53E -40E	17 20 25 35	17 20 25 35
33	Address and command hold time, t_{IH_b}	-800/-80E -667 -53E -40E	25 27 37 47	25 27 37 47
34	Data/data mask input setup time, t_{DS_b}	-800/-80E -667/-53E -40E	05 10 15	05 10 15
35	Data/data mask input hold time, t_{DH_b}	-800/-80E -667 -53E -40E	12 17 22 27	12 17 22 27
36	Write recovery time, t_{WR}		3C	3C
37	WRITE-to-READ command delay, t_{WTR}	-80E/-667/-53E -800/-40E	1E 28	1E 28
38	READ-to-PRECHARGE command delay, t_{RTP}		1E	1E
39	Memory analysis probe		00	00
40	Extension for bytes 41 and 42	-80E -800/-667/-53E/-40E	30 00	36 06
41	MIN active-to-active/refresh time, t_{RC}^1	-80E -800/-667/-53E -40E	39 3C 37	39 3C 37
42	MIN AUTO REFRESH to ACTIVE/ AUTO REFRESH command period, t_{RFC}		69	7F
43	SDRAM device MAX cycle time, $t_{CK} (MAX)$		80	80
44	SDRAM device MAX DQS-DQ skew time, t_{DQSQ}	-800/-80E -667 -53E -40E	14 18 1E 23	14 18 1E 23
45	SDRAM device MAX read data hold skew factor, t_{QHS}	-800/-80E -667 -53E -40E	1E 22 28 2D	1E 22 28 2D
46	PLL relock time	n/a	00	00
47-61	Optional features, not supported		00	00
62	SPD revision	Release 1.2	12	12

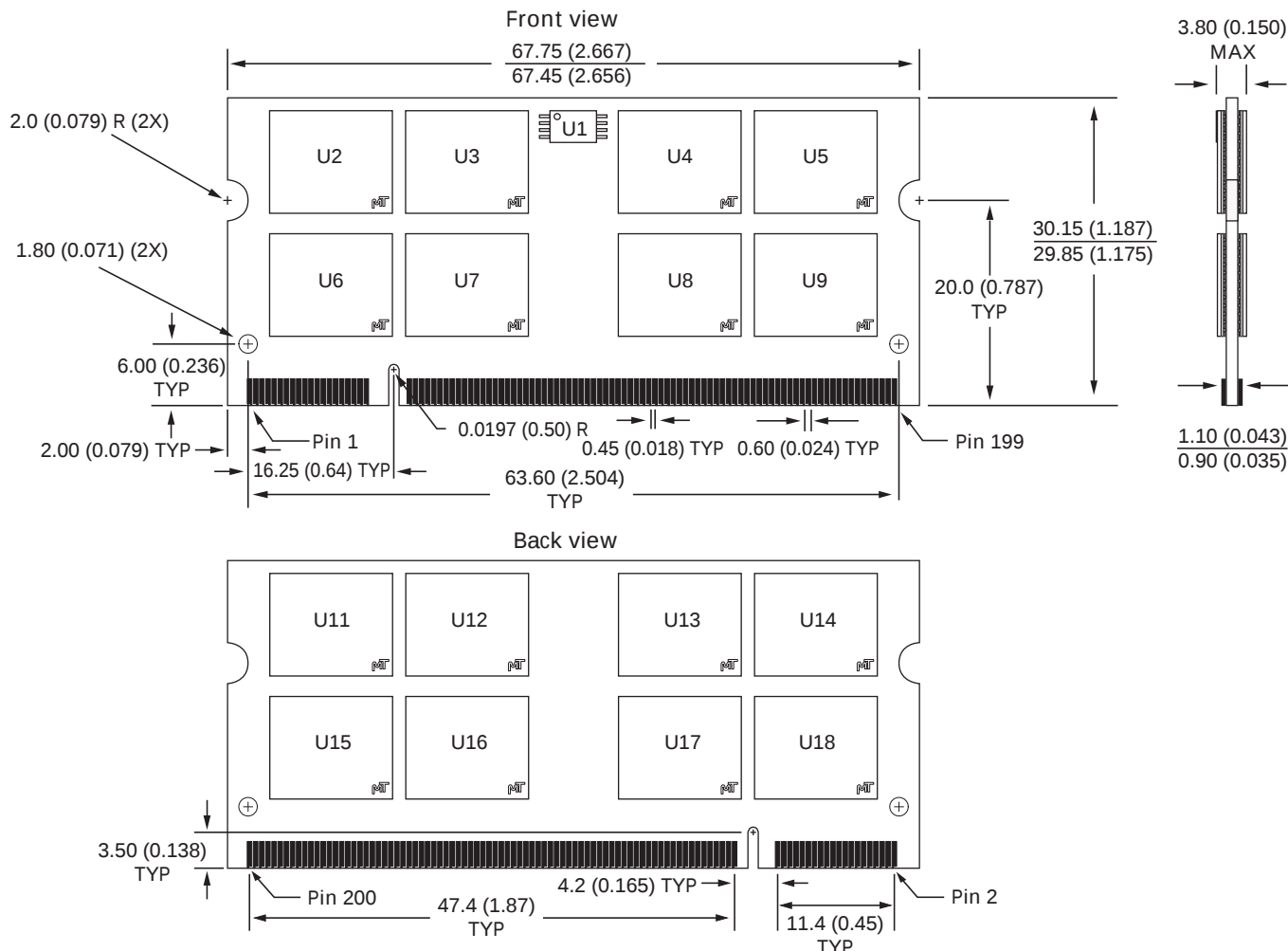
Table 13: Serial Presence-Detect Matrix (continued)

Byte	Description	Entry (Version)	1GB	2GB
63	Checksum for bytes 0–62	-80E -800 -667 -53E -40E	92 33 4E F9 60	33 D4 EF 9A 01
64	Manufacturer's JEDEC ID code	MICRON	2C	2C
65–71	Manufacturer's JEDEC ID code	(continued)	00	00
72	Manufacturing location	1–12	01–0C	01–0C
73–90	Module part number (ASCII)	–	Variable data	Variable data
91	PCB identification code	1–9	01–09	01–09
92	Identification code (continued)	0	00	00
93	Year of manufacture in BCD	–	Variable data	Variable data
94	Week of manufacture in BCD	–	Variable data	Variable data
95–98	Module serial number	–	Variable data	Variable data
99–127	Reserved for manufacturer-specific data		00	00
128–255	Reserved for customer-specific data		FF	FF

Notes: 1. The ^tRC SPD values shown are JEDEC DDR2 device specification values. The actual Micron DDR2 device specification is ^tRC = 55ns for all speed grades.

Module Dimensions

Figure 3: 200-Pin DDR2 SODIMM



- Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

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This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.