Freescale Semiconductor
Technical Data

Document Number: MRF6VP2600H
Rev. 2.1, 11/2008

RoHS

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

MRF6VP2600HR6

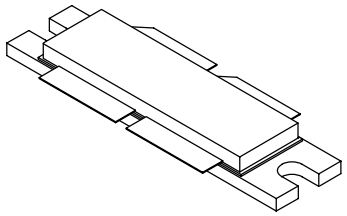
10-250 MHz, 600 W, 50 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET

Designed primarily for wideband applications with frequencies up to 250 MHz. Device is unmatched and is suitable for use in broadcast applications.

- Typical DVBT OFDM Performance: V_{DD} = 50 Volts, I_{DQ} = 2600 mA, P_{out} = 125 Watts Avg., f = 225 MHz, Channel Bandwidth = 7.61 MHz, Input Signal PAR = 9.3 dB @ 0.01% Probability on CCDF.
  - Power Gain — 25 dB
  - Drain Efficiency — 28.5%
  - ACPR @ 4 MHz Offset — -61 dBc @ 4 kHz Bandwidth
- Typical Pulsed Performance: V_{DD} = 50 Volts, I_{DQ} = 2600 mA, P_{out} = 600 Watts Peak, f = 225 MHz, Pulse Width = 100 μsec, Duty Cycle = 20%
  - Power Gain — 25.3 dB
  - Drain Efficiency — 59%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 225 MHz, 600 Watts Peak Power, Pulse Width = 100 μsec, Duty Cycle = 20%

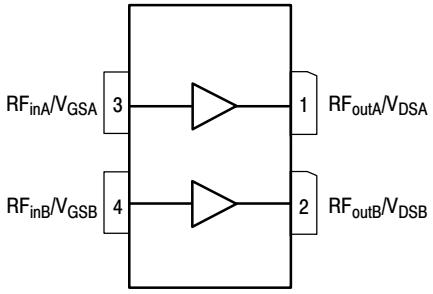
Features

- Integrated ESD Protection
- Excellent Thermal Stability
- Designed for Push-Pull Operation
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.



CASE 375D-05, STYLE 1
NI-1230

PART IS PUSH-PULL



(Top View)

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +110	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 99°C, 125 W CW	$R_{\theta JC}$	0.20	°C/W

1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

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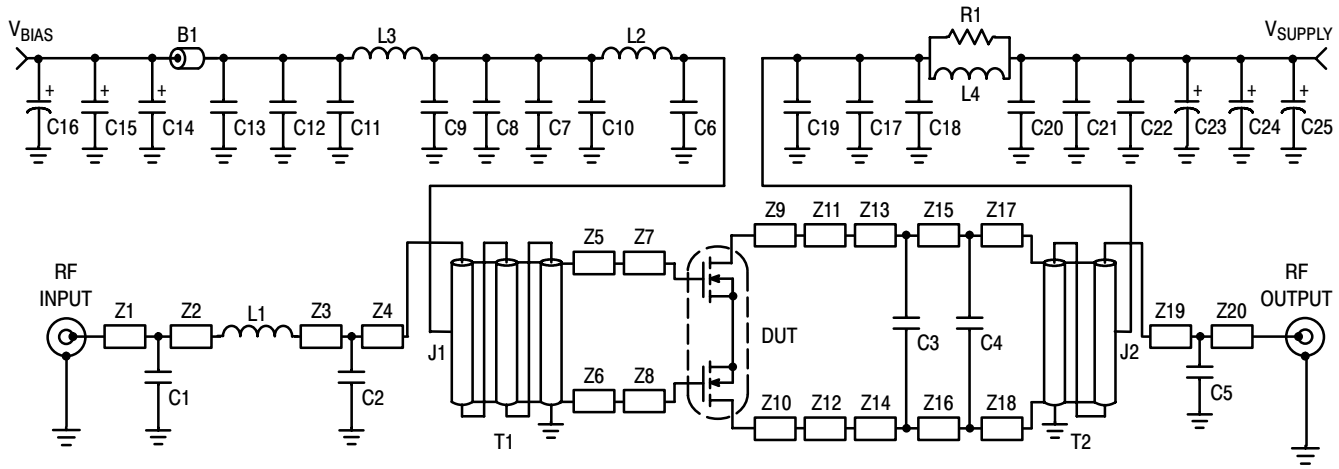
Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (1)					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	10	μAdc
Drain-Source Breakdown Voltage (I_D = 150 mA, V_{GS} = 0 Vdc)	$V_{(BR)DSS}$	110	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	50	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	2.5	mA
On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 800 μAdc)	$V_{GS(th)}$	1	1.65	3	Vdc
Gate Quiescent Voltage (2) (V_{DD} = 50 Vdc, I_D = 2600 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	2.7	3.5	Vdc
Drain-Source On-Voltage (1) (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.25	—	Vdc
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1.7	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	101	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	287	—	pF
Functional Tests (2) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 2600 mA, P_{out} = 125 W Avg., f = 225 MHz, DVBT OFDM Single Channel. ACPR measured in 7.61 MHz Channel Bandwidth @ ±4 MHz Offset.					
Power Gain	G_{ps}	24	25	27	dB
Drain Efficiency	η_D	27	28.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-61	-59	dBc
Input Return Loss	IRL	—	-18	-9	dB

1. Each side of device measured separately.
2. Measurement made with device in push-pull configuration.



Z1	1.049″ x 0.080″ Microstrip	Z13, Z14	0.224″ x 0.253″ Microstrip
Z2*	0.143″ x 0.080″ Microstrip	Z15*, Z16*	0.095″ x 0.253″ Microstrip
Z3*	0.188″ x 0.080″ Microstrip	Z17, Z18	0.052″ x 0.253″ Microstrip
Z4	0.192″ x 0.133″ Microstrip	Z19	0.053″ x 0.080″ Microstrip
Z5, Z6	0.418″ x 0.193″ Microstrip	Z20	1.062″ x 0.080″ Microstrip
Z7, Z8	0.217″ x 0.518″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030″, ε_r = 2.55
Z9, Z10	0.200″ x 0.518″ Microstrip		
Z11, Z12	0.375″ x 0.214″ Microstrip		

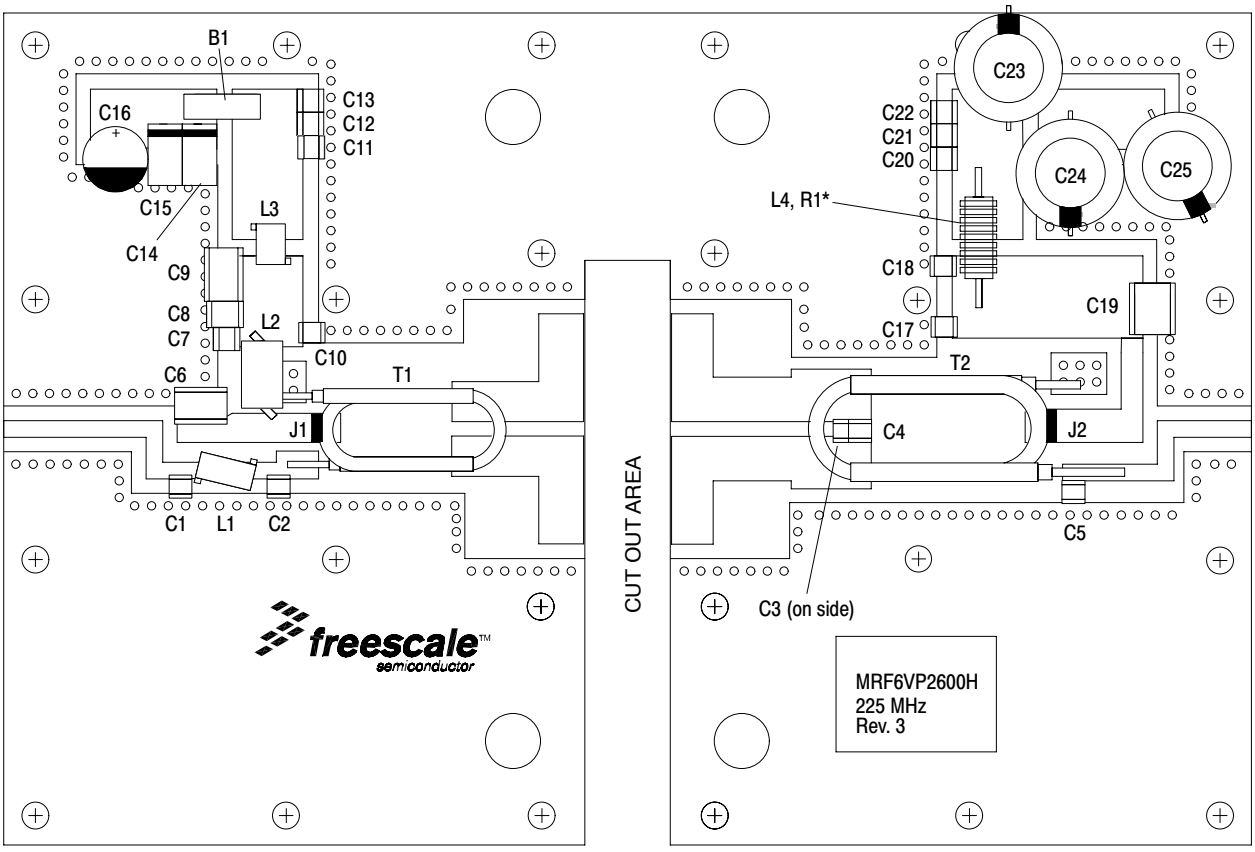
* Line length includes microstrip bends

Figure 2. MRF6VP2600HR6 Test Circuit Schematic

Table 5. MRF6VP2600HR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	95 Ω, 100 MHz Long Ferrite Bead	2743021447	Fair-Rite
C1	47 pF Chip Capacitor	ATC100B470JT500XT	ATC
C2, C4	43 pF Chip Capacitors	ATC100B430JT500XT	ATC
C3	100 pF Chip Capacitor	ATC100B101JT500XT	ATC
C5	10 pF Chip Capacitor	ATC100B7R5CT500XT	ATC
C6, C9	2.2 μF, 50 V Chip Capacitors	C1825C225J5RAC	Kemet
C7, C13, C20	10K pF Chip Capacitors	ATC200B103KT50XT	ATC
C8	220 nF, 50 V Chip Capacitor	C1812C224J5RAC	Kemet
C10, C17, C18	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C11, C22	0.1 μF, 50 V Chip Capacitors	CDR33BX104AKYS	Kemet
C12, C21	20K pF Chip Capacitors	ATC200B203KT50XT	ATC
C14	10 μF, 35 V Tantalum Capacitor	T491D106K035AT	Kemet
C15	22 μF, 35 V Tantalum Capacitor	T491X226K035AT	Kemet
C16	47 μF, 50 V Electrolytic Capacitor	476KXM050M	Illinois Cap
C19	2.2 μF, Chip Capacitor	2225X7R225KT3AB	ATC
C23, C24, C25	470 μF 63V Electrolytic Capacitors	EKME630ELL471MK25S	Multicomp
J1, J2	Jumpers from PCB to T1 & T2	Copper Foil	
L1	17.5 nH 6 Turn Inductor	B06T	CoilCraft
L2	8 Turns, #20 AWG ID = 0.125″ Inductor, Hand Wound	Copper Wire	
L3	82 nH Inductor	1812SMS-82NJ	CoilCraft
L4*	9 Turns, #18 AWG Inductor, Hand Wound	Copper Wire	
R1	20 Ω, 3 W Axial Leaded Resistor	5093NW20R00J	Vishay
T1	Balun	TUI-9	Comm Concepts
T2	Balun	TUO-4	Comm Concepts

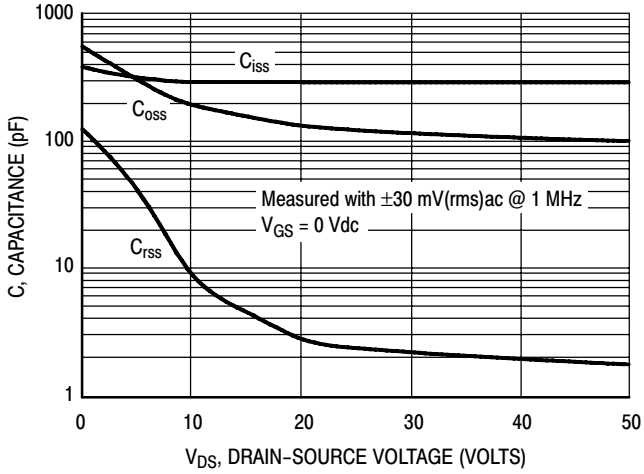
*L4 is wrapped around R1.



* L4 is wrapped around R1.

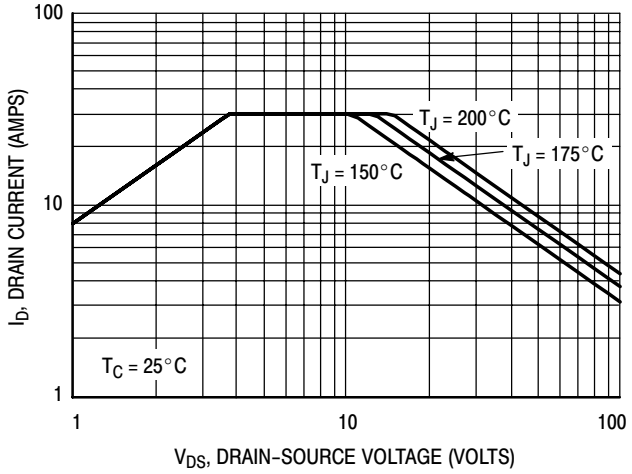
Figure 3. MRF6VP2600HR6 Test Circuit Component Layout

TYPICAL CHARACTERISTICS



Note: Each side of device measured separately.

Figure 4. Capacitance versus Drain-Source Voltage



Note: Each side of device measured separately.

Figure 5. DC Safe Operating Area

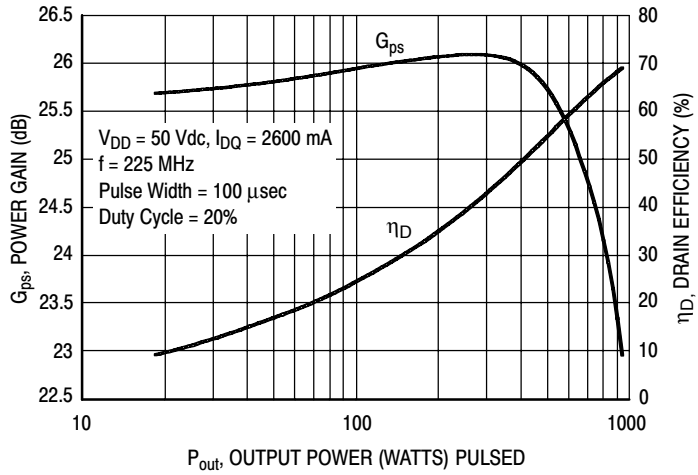


Figure 6. Pulsed Power Gain and Drain Efficiency versus Output Power

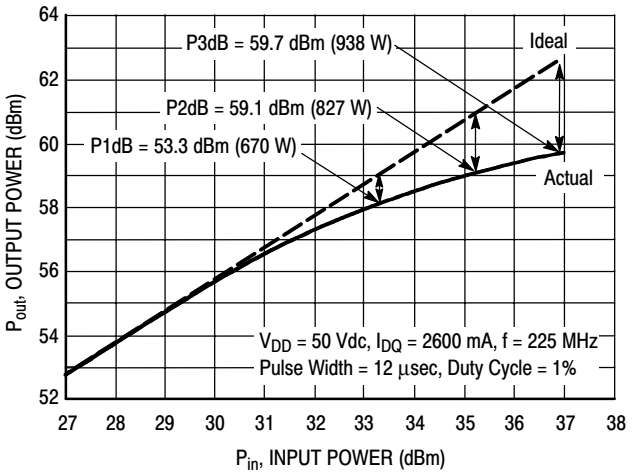


Figure 7. Pulsed CW Output Power versus Input Power

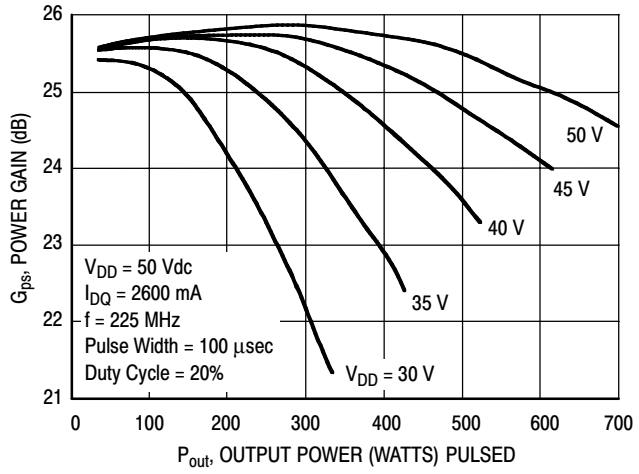


Figure 8. Pulsed Power Gain versus Output Power

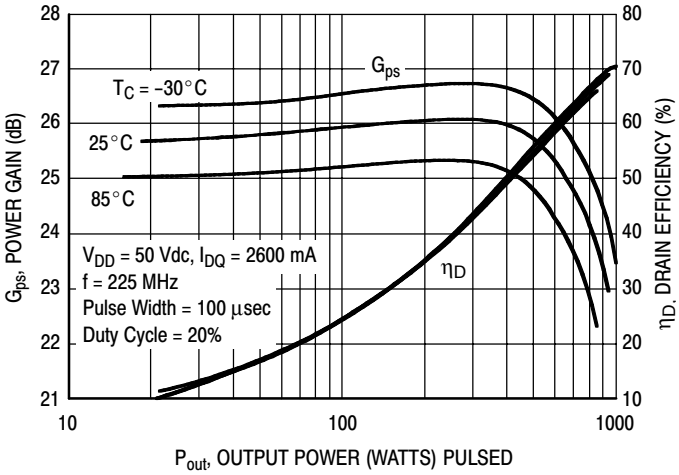


Figure 9. Pulsed Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS — TWO-TONE

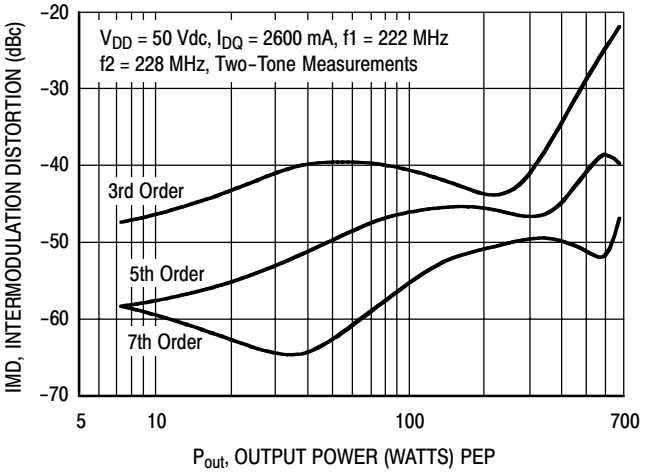


Figure 10. Intermodulation Distortion Products versus Output Power

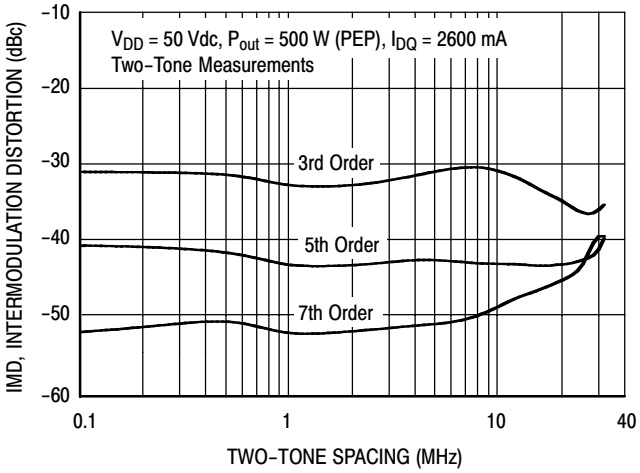


Figure 11. Intermodulation Distortion Products versus Tone Spacing

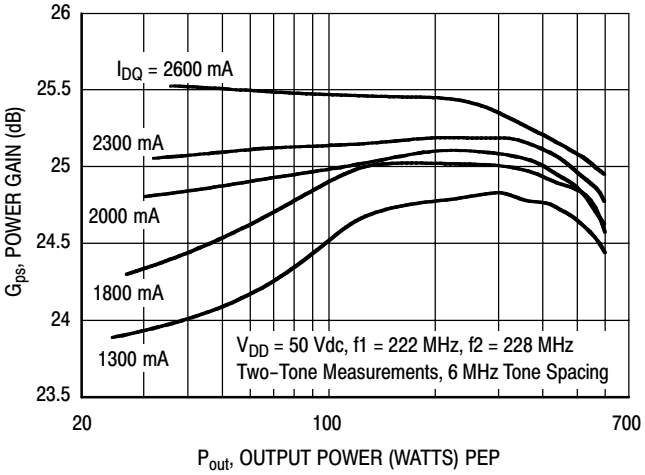


Figure 12. Two-Tone Power Gain versus Output Power

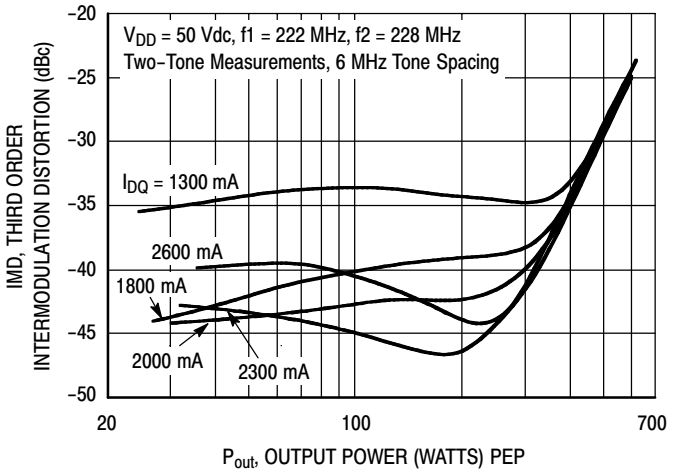


Figure 13. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS — OFDM

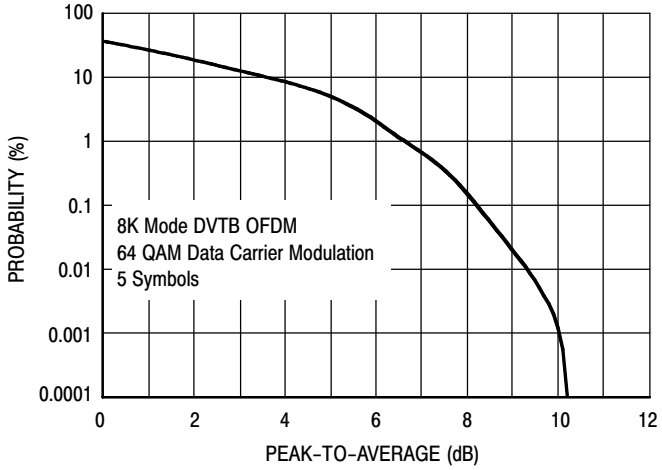


Figure 14. Single-Carrier DVTB OFDM

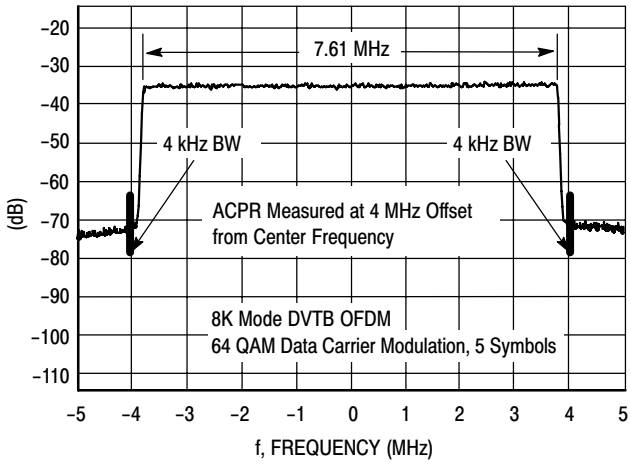


Figure 15. 8K Mode DVBT OFDM Spectrum

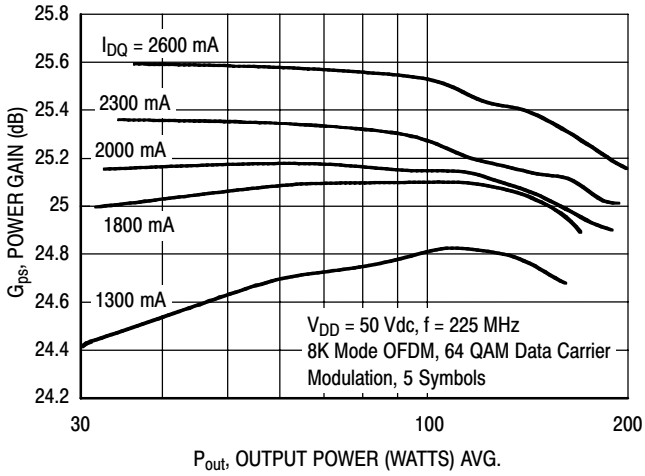


Figure 16. Single-Carrier DVBT OFDM Power Gain versus Output Power

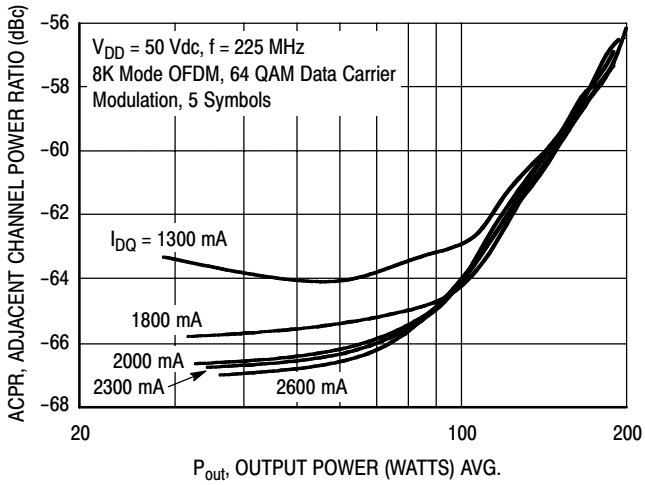


Figure 17. Single-Carrier DVBT OFDM ACPR versus Output Power

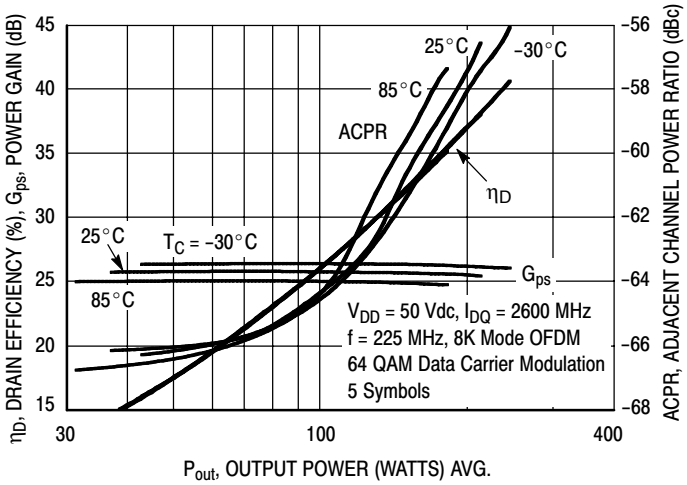
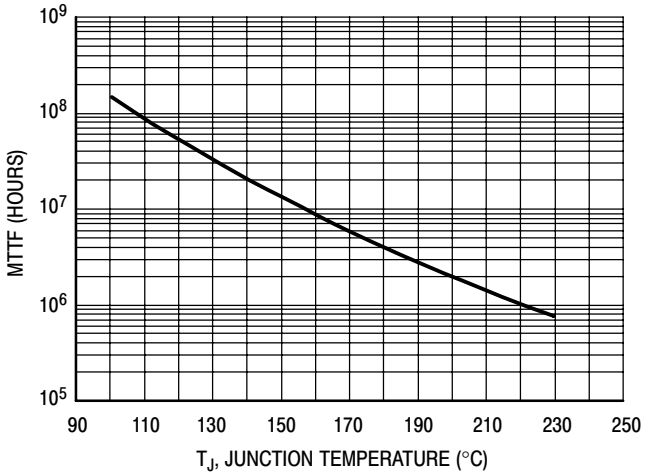


Figure 18. Single-Carrier DVBT OFDM ACPR Power Gain and Drain Efficiency versus Output Power

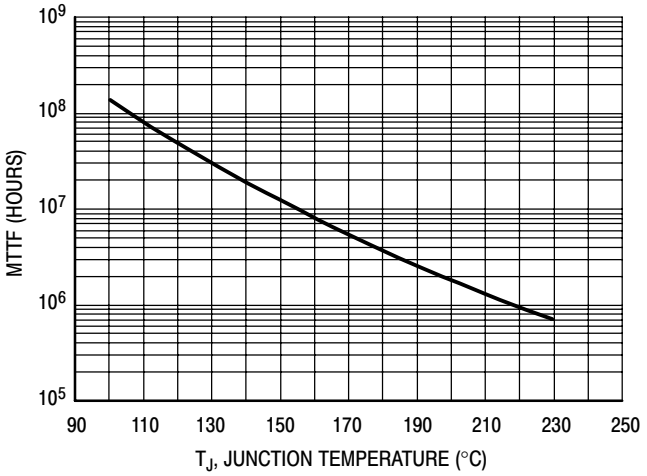
TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 50 Vdc, P_{out} = 125 W Avg., and η_D = 28.5%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

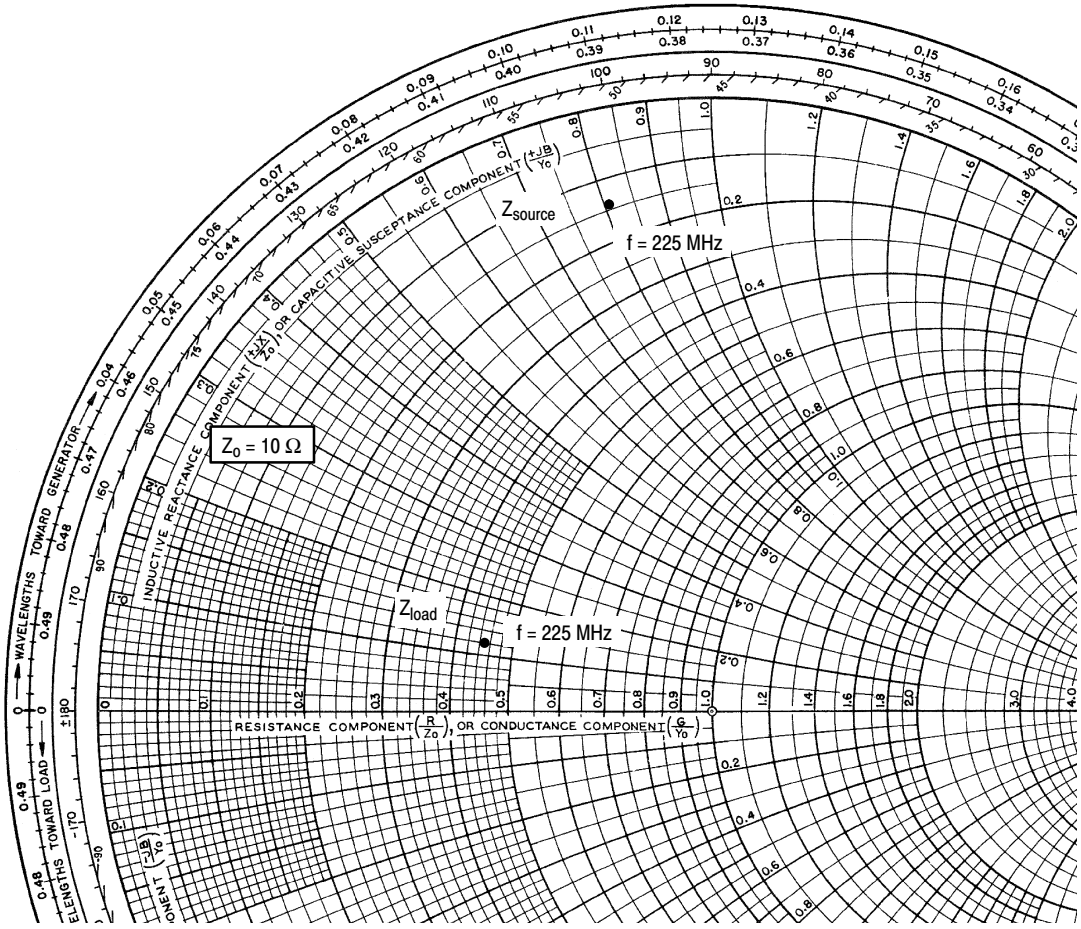
Figure 19. MTTF versus Junction Temperature - CW



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 50 Vdc, P_{out} = 600 W Peak, Pulse Width = 100 μsec, Duty Cycle = 20%, and η_D = 59%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 20. MTTF versus Junction Temperature - Pulsed



V_{DD} = 50 Vdc, I_{DQ} = 2600 mA, P_{out} = 125 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
225	1.42 + j8.09	4.45 + j1.16

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

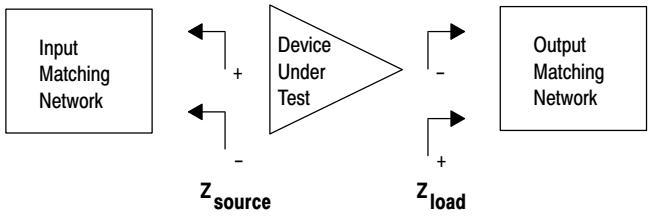
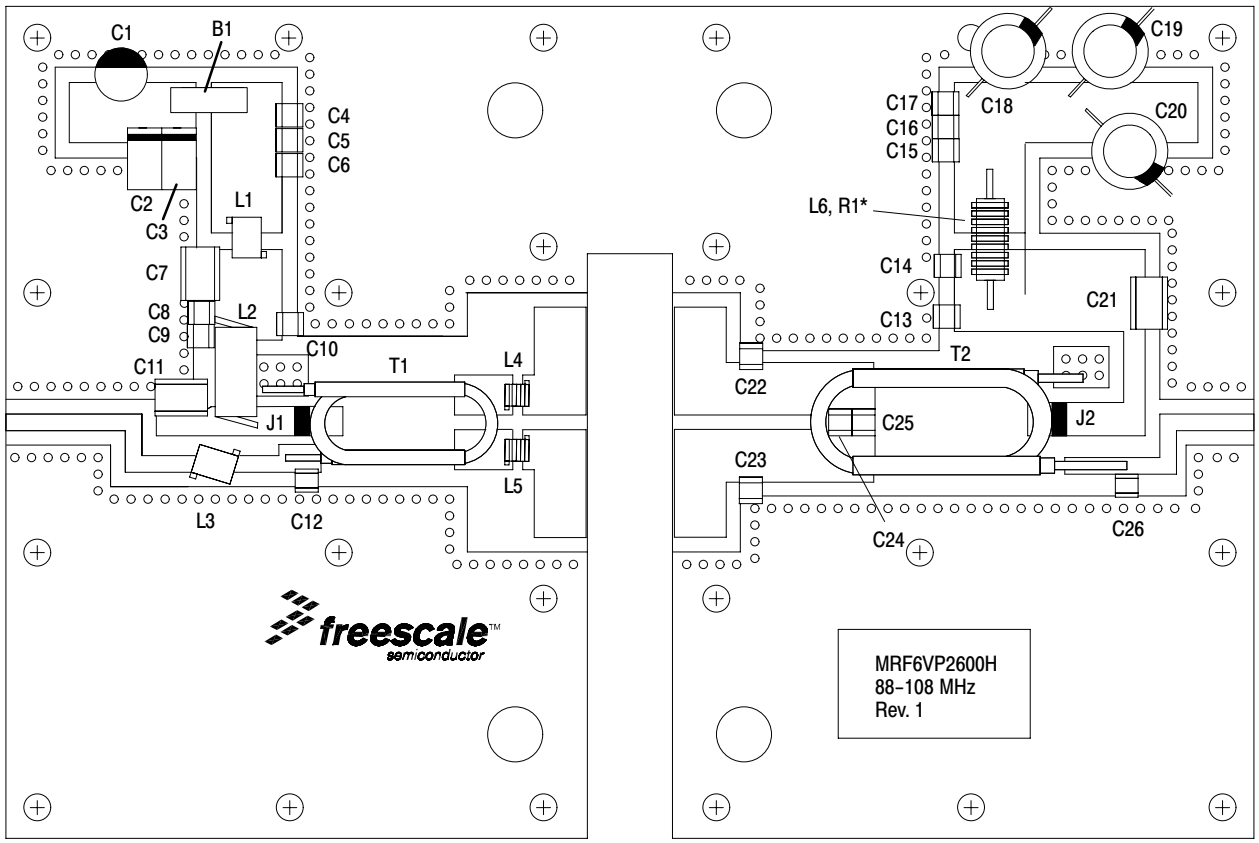


Figure 21. Series Equivalent Source and Load Impedance



* L6 is wrapped around R1.

Figure 22. MRF6VP2600HR6 Test Circuit Component Layout — 88-108 MHz

Table 6. MRF6VP2600HR6 Test Circuit Component Designations and Values — 88-108 MHz

Part	Description	Part Number	Manufacturer
B1	95 Ω, 100 MHz Long Ferrite Bead	2743021447	Fair-Rite
C1	47 μF, 50 V Electrolytic Capacitor	476KXM050M	Illinois Cap
C2	22 μF, 35 V Tantalum Capacitor	T491X226K035AT	Kemet
C3	10 μF, 35 V Tantalum Capacitor	T491D106K035AT	Kemet
C4, C9, C15	10K pF Chip Capacitors	ATC200B103KT50XT	ATC
C5, C16	20K pF Chip Capacitors	ATC200B203KT50XT	ATC
C6, C17	0.1 μF, 50 V Chip Capacitors	CDR33BX104AKYS	AVX
C7, C11	2.2 μF, 50 V Chip Capacitors	C1825C225J5RAC	Kemet
C8	220 nF, 50 V Chip Capacitor	C1812C224J5RAC	Kemet
C10, C13, C14	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C12	33 pF Chip Capacitor	ATC100B330JT500XT	ATC
C18, C19, C20	470 μF, 63 V Electrolytic Capacitors	EKME630ELL471MK25S	MultiComp
C21	2.2 μF, 100 V Chip Capacitor	G2225X7R225KT3AB	ATC
C22, C23	120 pF, Chip Capacitors	ATC100B121JT500XT	ATC
C24	150 pF Chip Capacitor	ATC100B151JT500XT	ATC
C25	100 pF Chip Capacitor	ATC100B101JT500XT	ATC
C26	15 pF Chip Capacitor	ATC100B150JT500XT	ATC
J1, J2	Jumpers from PCB to T1 & T2	Copper Foil	
L1	82 nH Inductor	1812SMS-82NJ	CoilCraft
L2	8 Turns, #20 AWG ID = 0.125″ Inductor, Hand Wound	Copper Wire	
L3	120 nH Inductor	1812SMS-R12J	CoilCraft
L4, L5	12.5 nH 4 Turn Inductor	A04T	CoilCraft
L6*	9 Turns, #18 AWG Inductor, Hand Wound	Copper Wire	
R1	20 Ω, 3 W Axial Leaded Resistor	5093NW20R00J	Vishay
T1	Balun Transformer	TUI-9	Comm Concepts
T2	Balun Transformer	TUO-9	Comm Concepts

*L6 is wrapped around R1.

TYPICAL CHARACTERISTICS — 88-108 MHz

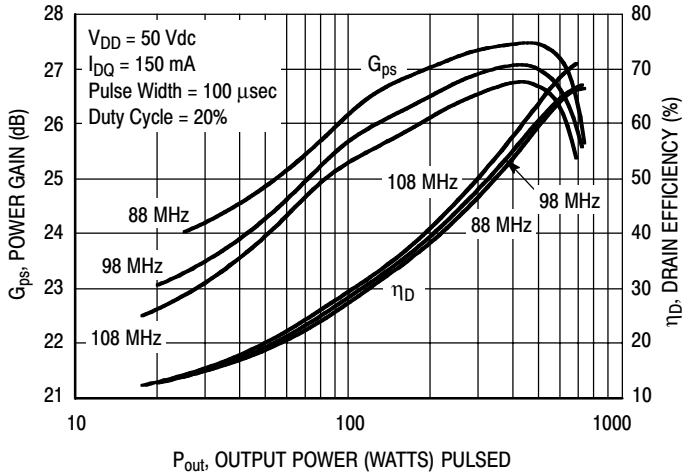


Figure 23. Broadband Pulsed Power Gain and Drain Efficiency versus Output Power — 88-108 MHz

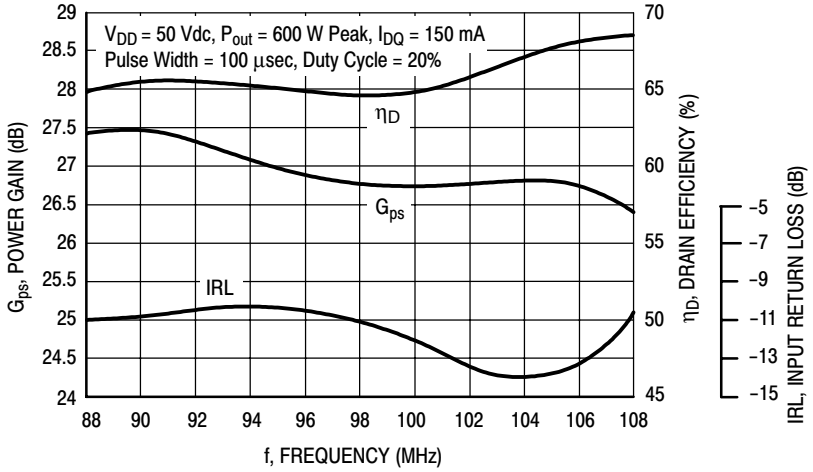


Figure 24. Pulsed Power Gain, Drain Efficiency and IRL versus Frequency — 88-108 MHz

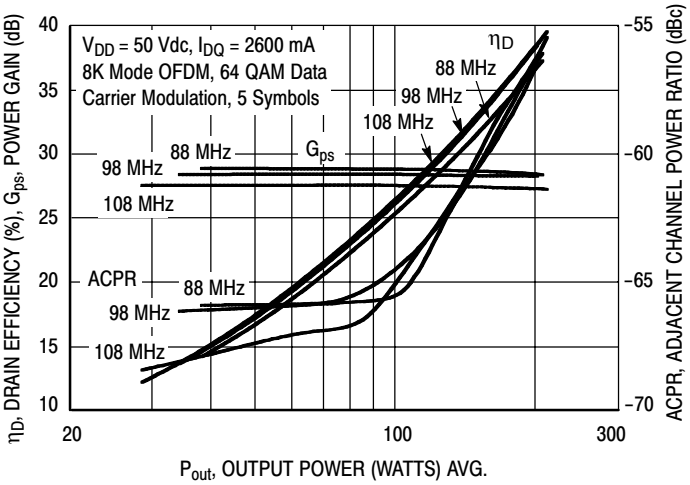


Figure 25. Single-Carrier DVBT OFDM ACPR, Power Gain and Drain Efficiency versus Output Power — 88-108 MHz

TYPICAL CHARACTERISTICS — 88-108 MHz

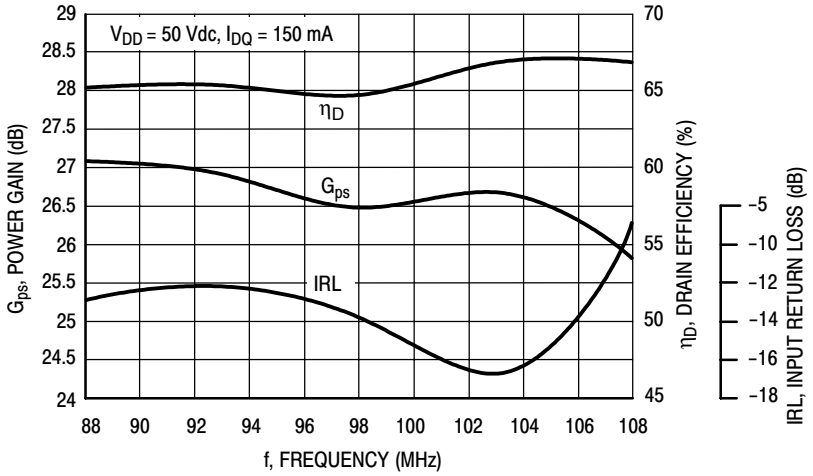
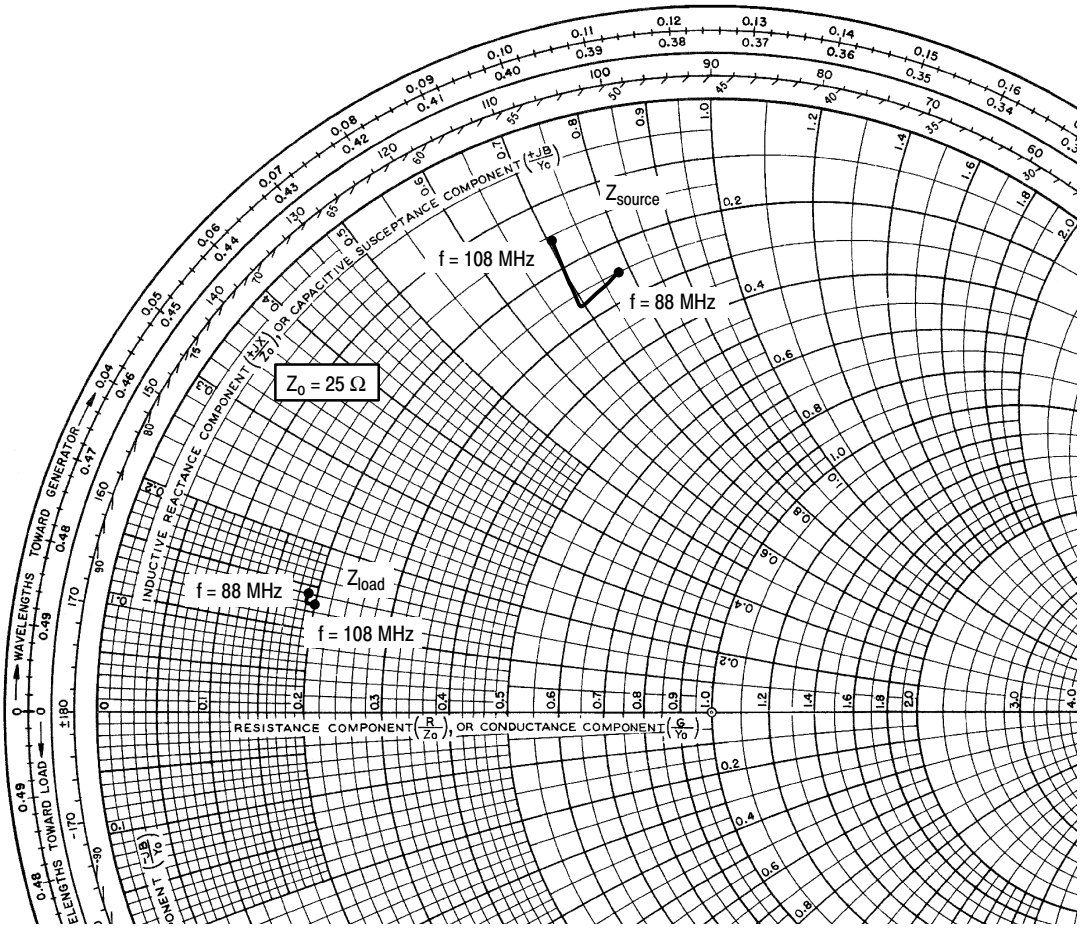


Figure 26. CW Power Gain, Drain Efficiency and IRL versus Frequency — 88-108 MHz



V_{DD} = 50 Vdc, I_{DQ} = 2600 mA, P_{out} = 125 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
88	6.3 + j19.4	4.75 + j3.45
98	6.8 + j17.2	4.82 + j3.22
108	4.0 + j17.8	4.96 + j3.18

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

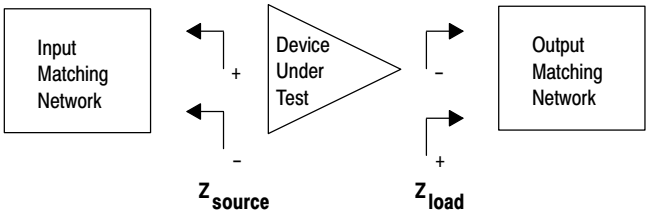
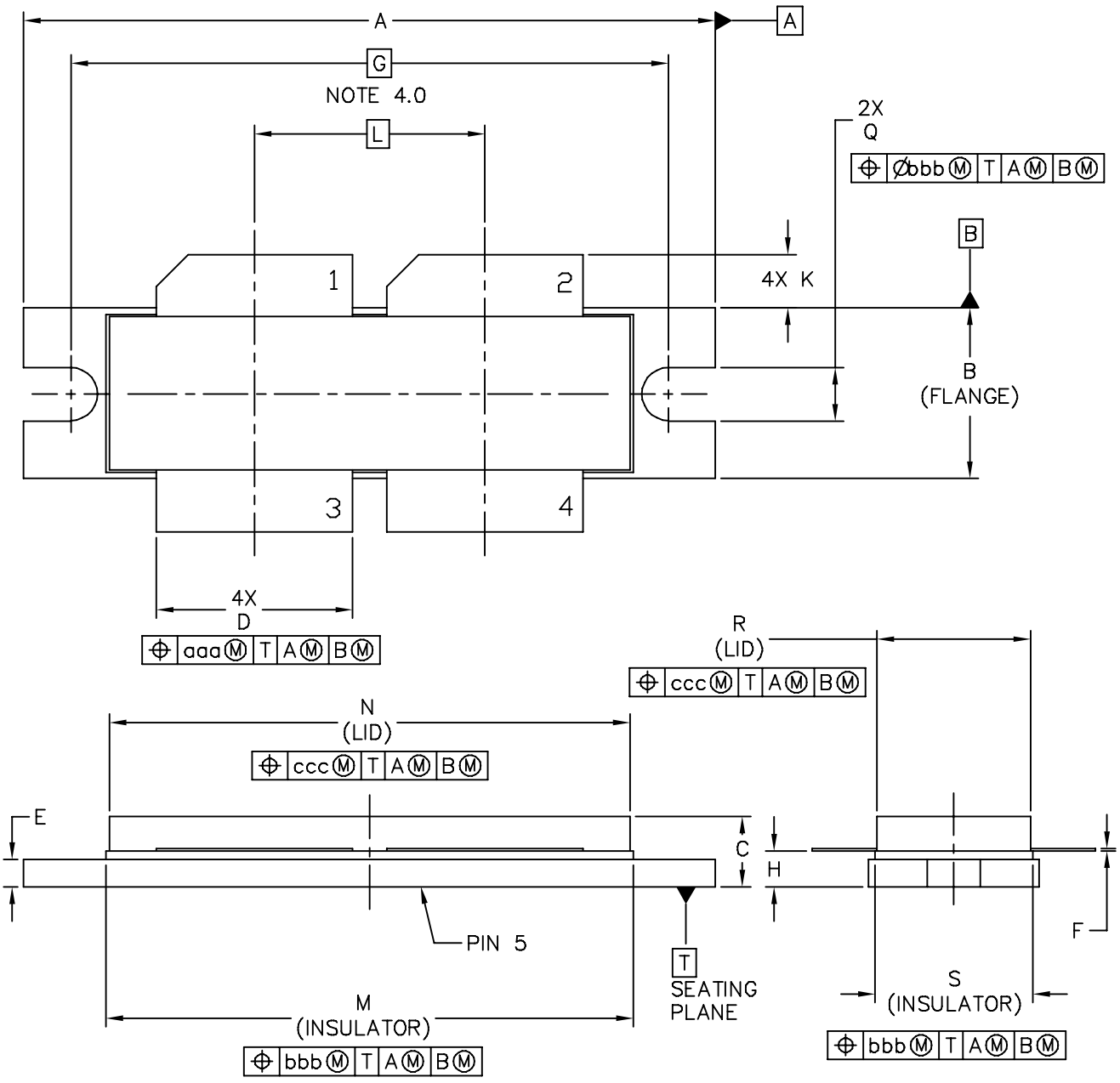


Figure 27. Series Equivalent Source and Load Impedance — 88-108 MHz

PACKAGE DIMENSIONS



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NOTES:

1. 0 INTERPRET DIMENSIONS AND TOLERANCES
PER ASME Y14. 5M–1994.

2. 0 CONTROLLING DIMENSION: INCH

3. 0 DIMENSION H IS MEASURED . 030 (0. 762)
AWAY FROM PACKAGE BODY.

4. 0 RECOMMENDED BOLT CENTER DIMENSION OF
1. 52 (38. 61) BASED ON M3 SCREW.

STYLE 1:
PIN 1 – DRAIN
2 – DRAIN
3 – GATE
4 – GATE
5 – SOURCE

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	1.615	1.625	41.02	41.28	N	1.218	1.242	30.94	31.55
B	.395	.405	10.03	10.29	Q	.120	.130	3.05	3.3
C	.150	.200	3.81	5.08	R	.355	.365	9.01	9.27
D	.455	.465	11.56	11.81	S	.365	.375	9.27	9.53
E	.062	.066	1.57	1.68					
F	.004	.007	0.1	0.18					
G	1.400 BSC		35.56 BSC		aaa	.013		0.33	
H	.082	.090	2.08	2.29	bbb	.010		0.25	
K	.117	.137	2.97	3.48	ccc	.020		0.51	
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					

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PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2008	• Initial Release of Data Sheet
1	July 2008	• Removed Capable of Handling 5:1 VSWR bullet, p. 1 • Corrected Z_{source} and Z_{load} values from 1.58 + j6.47 to 1.42 + j8.09 and 4.60 + j1.85 to 4.45 + j1.16 and replotted data in Fig. 21, Series Equivalent Source and Load Impedance, p. 9
2	Sept. 2008	• Added Note to Fig. 4, Capacitance versus Drain-Source Voltage and Fig. 5, DC Safe Operating Area to denote that each side of device is measured separately, p. 5 • Updated Fig. 5, DC Safe Operating Area, to show one side of the device, p. 5 • Figs. 21 and 27, Series Equivalent Source and Load Impedance, corrected Z_{source} copy to read “Test circuit impedance as measured from gate to gate, balanced configuration” and Z_{load} copy to read “Test circuit impedance as measured from gate to gate, balanced configuration”, p. 9, 14
2.1	Nov. 2008	• Corrected Figs. 21 and 27 Revision History Z_{load} copy to read ”Test circuit impedance as measured from drain to drain, balanced configuration”, p. 9, 14

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