Freescale Semiconductor
Technical Data

Document Number: MRF6VP11KH
Rev. 4, 12/2008

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

MRF6VP11KHR6

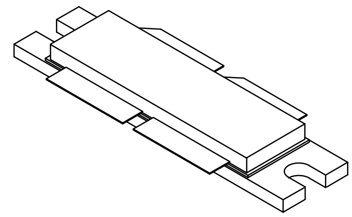
Designed primarily for pulsed wideband applications with frequencies up to 150 MHz. Device is unmatched and is suitable for use in industrial, medical and scientific applications.

- Typical Pulsed Performance at 130 MHz: V_{DD} = 50 Volts, I_{DQ} = 150 mA, P_{out} = 1000 Watts Peak (200 W Avg.), Pulse Width = 100 μsec, Duty Cycle = 20%
  - Power Gain — 26 dB
  - Drain Efficiency — 71%
- Capable of Handling 10:1 VSWR, @ 50 Vdc, 130 MHz, 1000 Watts Peak Power

Features

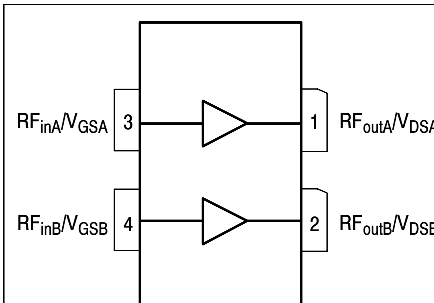
- Qualified Up to a Maximum of 50 V_{DD} Operation
- Integrated ESD Protection
- Excellent Thermal Stability
- Designed for Push-Pull Operation
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- RoHS Compliant
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.

10-150 MHz, 1000 W, 50 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFET



CASE 375D-05, STYLE 1
NI-1230

PART IS PUSH-PULL



(Top View)

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +110	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 1000 W Pulsed, 100 μsec Pulse Width, 20% Duty Cycle	$R_{\theta JC}$	0.03	°C/W

1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

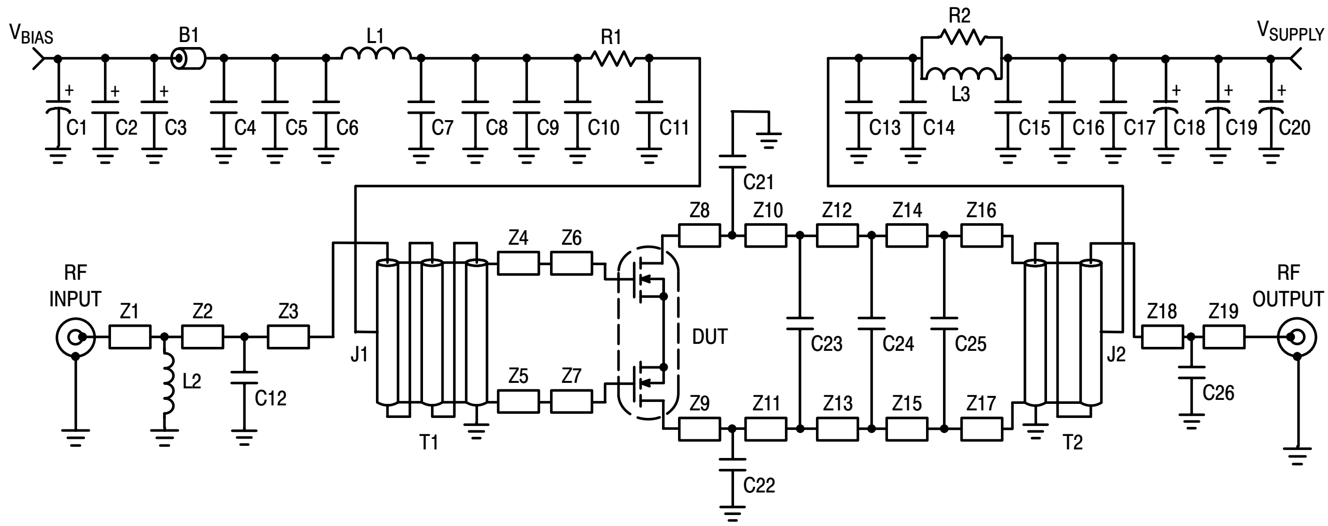
Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (1)					
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	10	μAdc
Drain-Source Breakdown Voltage (I_D = 300 mA, V_{GS} = 0 Vdc)	$V_{(BR)DSS}$	110	—	—	Vdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	100	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	mA
On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 1600 μAdc)	$V_{GS(th)}$	1	1.63	3	Vdc
Gate Quiescent Voltage (2) (V_{DD} = 50 Vdc, I_D = 150 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.5	2.2	3.5	Vdc
Drain-Source On-Voltage (1) (V_{GS} = 10 Vdc, I_D = 4 Adc)	$V_{DS(on)}$	—	0.28	—	Vdc
Dynamic Characteristics (1)					
Reverse Transfer Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	3.3	—	pF
Output Capacitance (V_{DS} = 50 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	147	—	pF
Input Capacitance (V_{DS} = 50 Vdc, V_{GS} = 0 Vdc ± 30 mV(rms)ac @ 1 MHz)	C_{iss}	—	506	—	pF
Functional Tests (2) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 150 mA, P_{out} = 1000 W Peak (200 W Avg.), f = 130 MHz, 100 μsec Pulse Width, 20% Duty Cycle					
Power Gain	G_{ps}	24	26	28	dB
Drain Efficiency	η_D	69	71	—	%
Input Return Loss	IRL	—	-16	-9	dB

1. Each side of device measured separately.
2. Measurement made with device in push-pull configuration.



Z1	0.175″ x 0.082″ Microstrip	Z14, Z15	0.116″ x 0.253″ Microstrip
Z2*	1.461″ x 0.082″ Microstrip	Z16*, Z17*	0.035″ x 0.253″ Microstrip
Z3*	0.080″ x 0.082″ Microstrip	Z18	0.275″ x 0.082″ Microstrip
Z4, Z5	0.133″ x 0.193″ Microstrip	Z19	0.845″ x 0.082″ Microstrip
Z6, Z7, Z8, Z9	0.500″ x 0.518″ Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030″, ε_r = 2.55
Z10, Z11	0.102″ x 0.253″ Microstrip		
Z12, Z13	0.206″ x 0.253″ Microstrip		

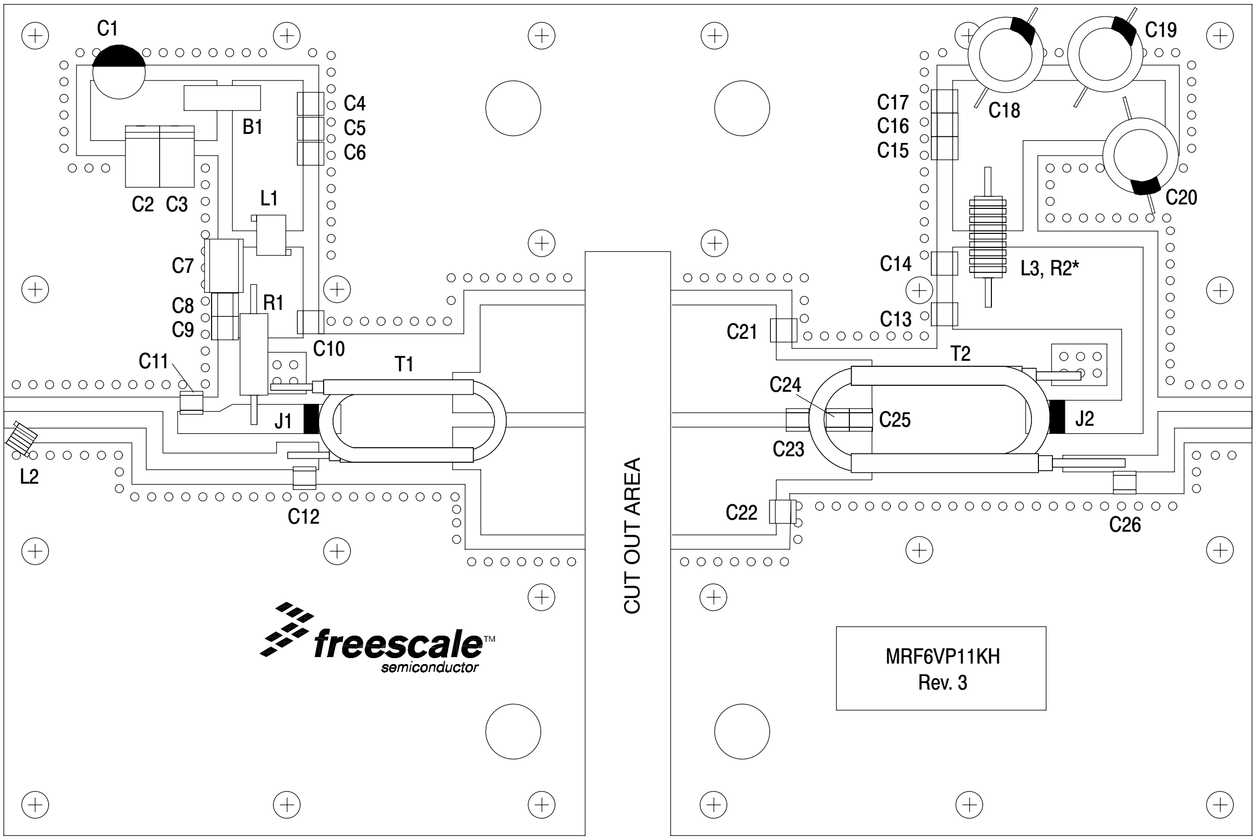
*Line length includes microstrip bends.

Figure 2. MRF6VP11KHR6 Test Circuit Schematic

Table 5. MRF6VP11KHR6 Test Circuit Component Designations and Values

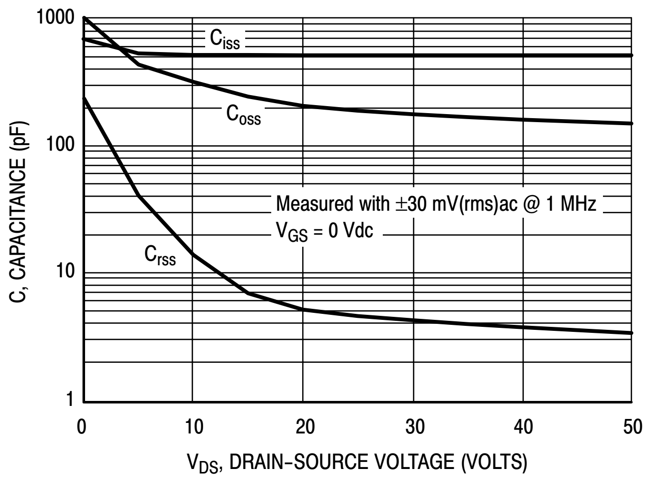
Part	Description	Part Number	Manufacturer
B1	95 Ω, 100 MHz Long Ferrite Bead	2743021447	Fair-Rite
C1	47 μF, 50 V Electrolytic Capacitor	476KXM050M	Illinois Cap
C2	22 μF, 35 V Tantalum Capacitor	T491X226K035AT	Kemet
C3	10 μF, 35 V Tantalum Capacitor	T491D106K035AT	Kemet
C4, C9, C17	10K pF Chip Capacitors	ATC200B103KT50XT	ATC
C5, C16	20K pF Chip Capacitors	ATC200B203KT50XT	ATC
C6, C15	0.1 μF, 50 V Chip Capacitors	CDR33BX104AKYS	Kemet
C7	2.2 μF, 50 V Chip Capacitor	C1825C225J5RAC	Kemet
C8	0.22 μF, 100 V Chip Capacitor	C1825C223K1GAC	Kemet
C10, C11, C13, C14	1000 pF Chip Capacitors	ATC100B102JT50XT	ATC
C12	18 pF Chip Capacitor	ATC100B180JT500XT	ATC
C18, C19, C20	470 μF, 63 V Electrolytic Capacitors	EKME630ELL471MK25S	Multicomp
C21, C22	47 pF Chip Capacitors	ATC100B470JT500XT	ATC
C23	75 pF Chip Capacitor	ATC100B750JT500XT	ATC
C24, C25	100 pF Chip Capacitors	ATC100B101JT500XT	ATC
C26	33 pF Chip Capacitor	ATC100B330JT500XT	ATC
J1, J2	Jumpers from PCB to T1 and T2	Copper Foil	
L1	82 nH Inductor	1812SMS-82NJLC	CoilCraft
L2	47 nH Inductor	1812SMS-47NJLC	CoilCraft
L3*	10 Turns, #18 AWG Inductor, Hand Wound	Copper Wire	
R1	1 KΩ, 1/4 W Axial Leaded Resistor	CMF601000R0FKEK	Vishay
R2	20 Ω, 3 W Chip Resistor	CPF320R000FKE14	Vishay
T1	Balun	TUI-9	Comm Concepts
T2	Balun	TUO-4	Comm Concepts

*L3 is wrapped around R2.



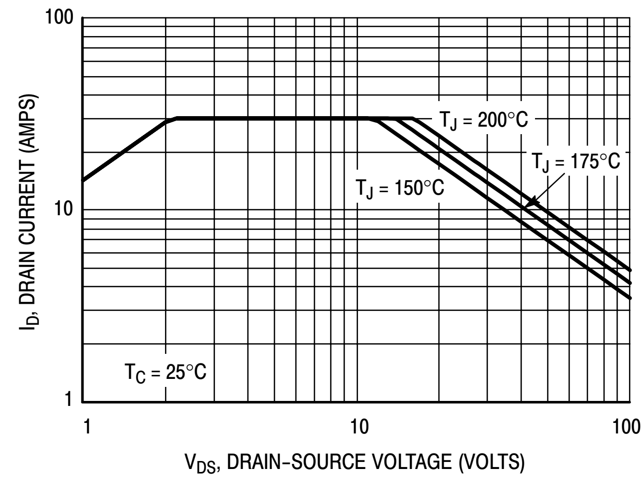
* L3 is wrapped around R2.

Figure 3. MRF6VP11KHR6 Test Circuit Component Layout



Note: Each side of device measured separately.

Figure 4. Capacitance versus Drain-Source Voltage



Note: Each side of device measured separately.

Figure 5. DC Safe Operating Area

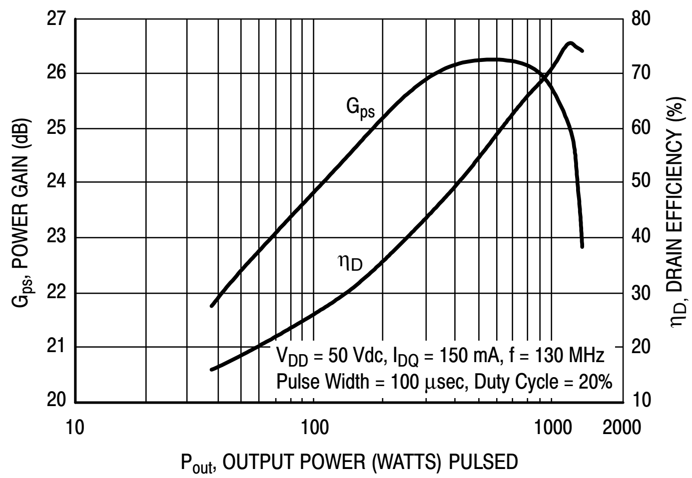


Figure 6. Pulsed Power Gain and Drain Efficiency versus Output Power

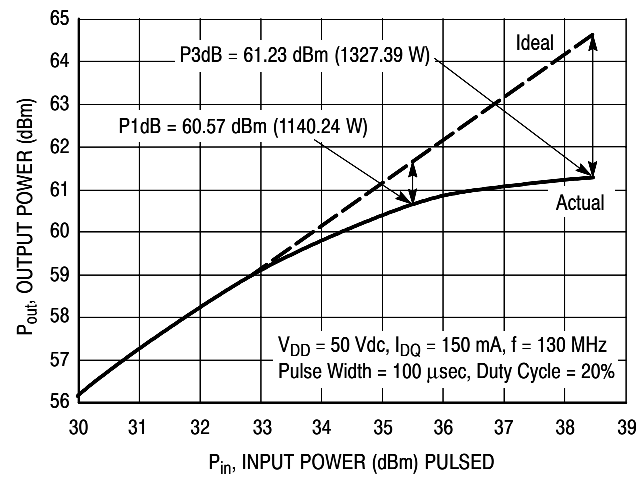


Figure 7. Pulsed Output Power versus Input Power

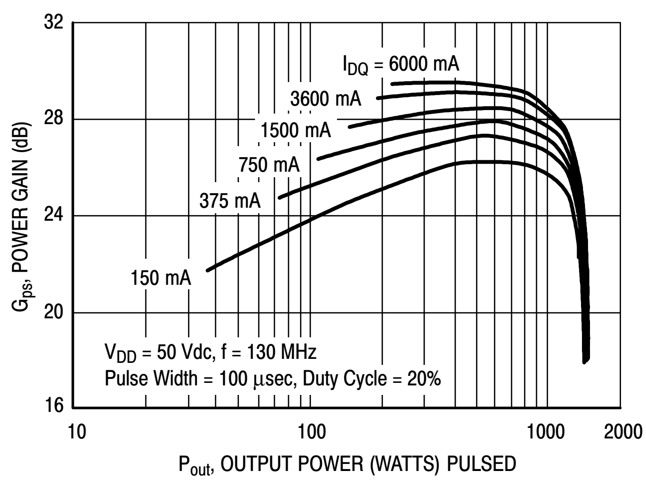


Figure 8. Pulsed Power Gain versus Output Power

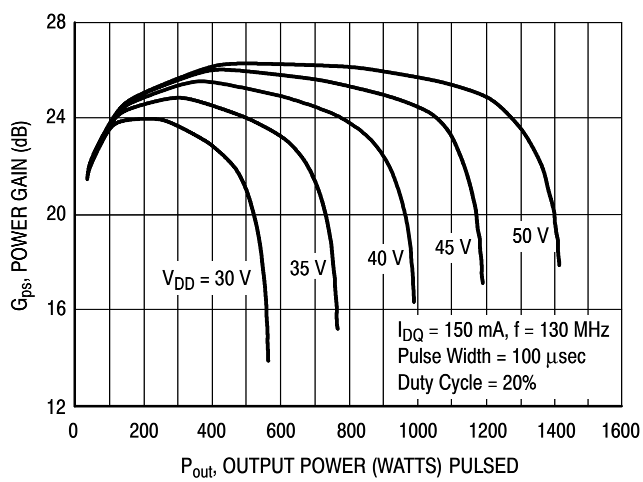


Figure 9. Pulsed Power Gain versus Output Power

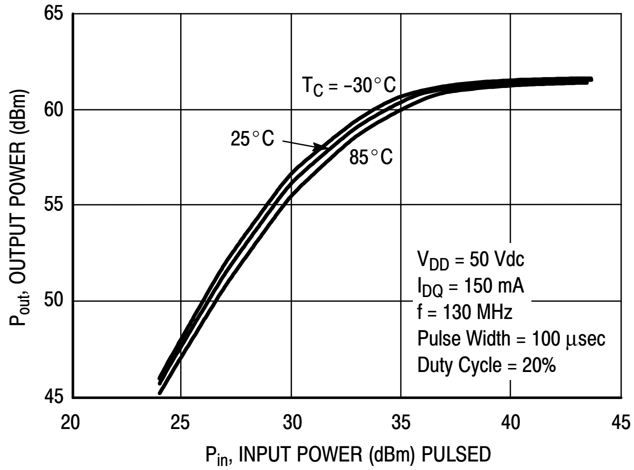


Figure 10. Pulsed Output Power versus Input Power

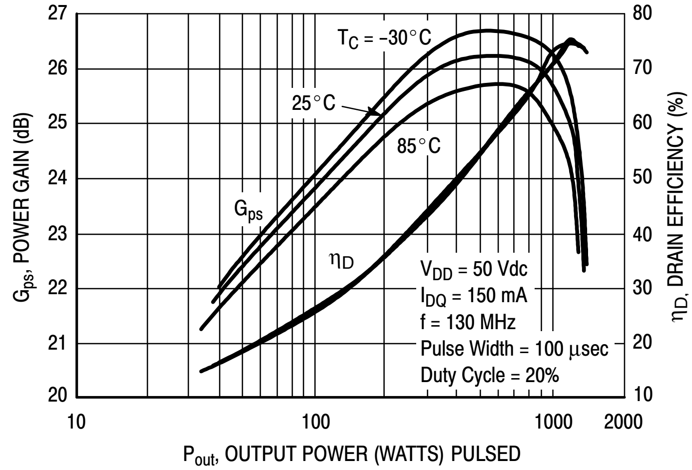


Figure 11. Pulsed Power Gain and Drain Efficiency versus Output Power

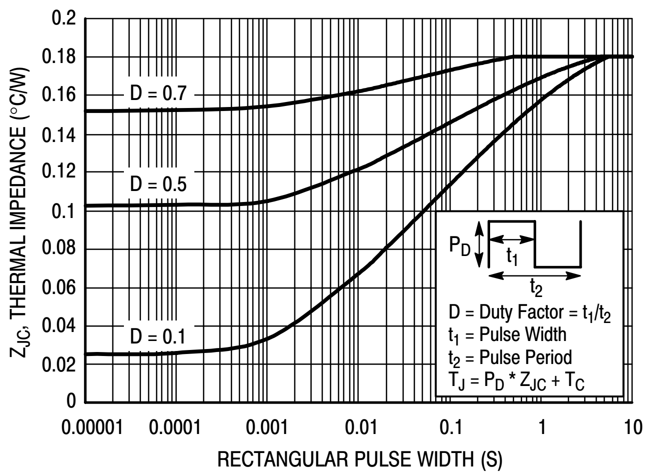
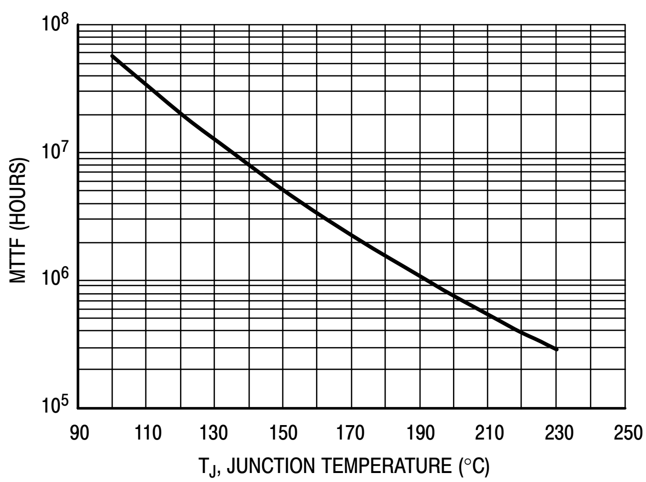


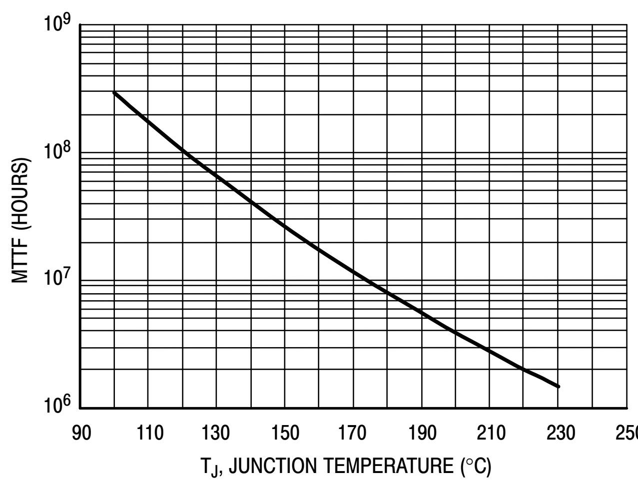
Figure 12. Maximum Transient Thermal Impedance



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 50 Vdc, P_{out} = 1000 W CW, and η_D = 70%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

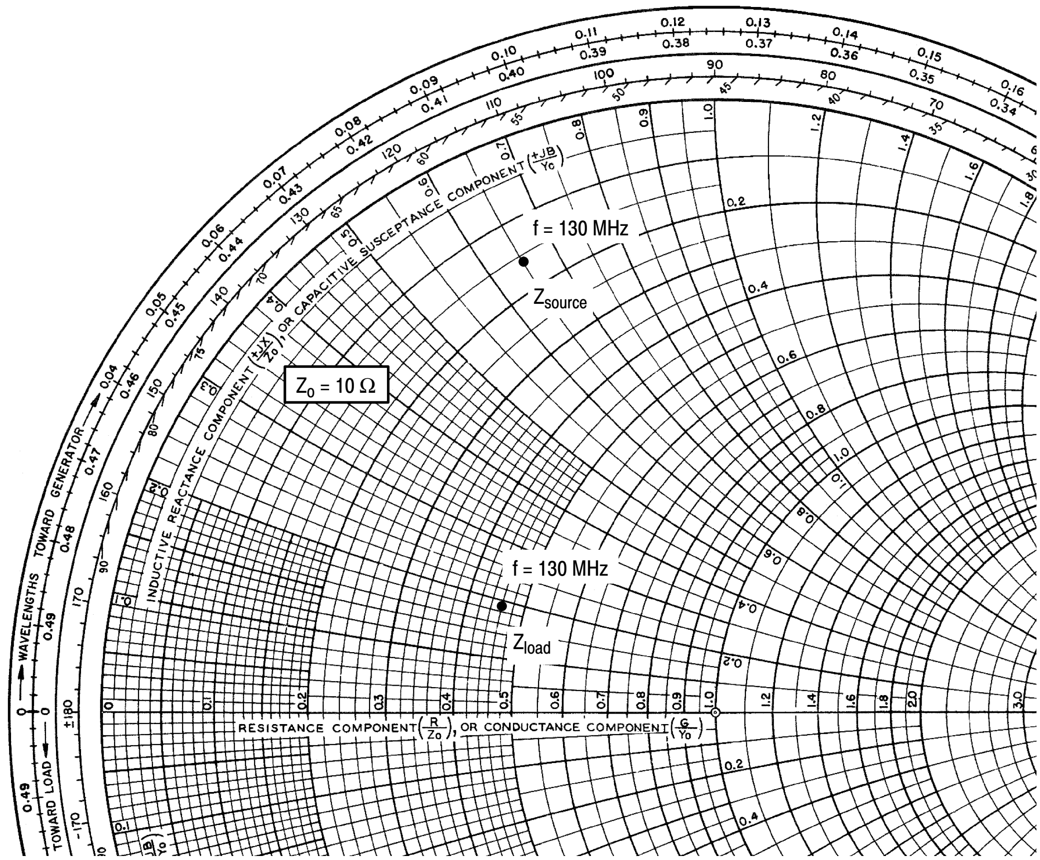
Figure 13. MTTF versus Junction Temperature - CW



This above graph displays calculated MTTF in hours when the device is operated at V_{DD} = 50 Vdc, P_{out} = 1000 W Peak, Pulse Width = 100 µsec, Duty Cycle = 20%, and η_D = 71%.

MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

Figure 14. MTTF versus Junction Temperature - Pulsed



V_{DD} = 50 Vdc, I_{DQ} = 150 mA, P_{out} = 1000 W Peak

f MHz	Z_{source} Ω	Z_{load} Ω
130	1.58 + j6.47	4.6 + j1.85

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

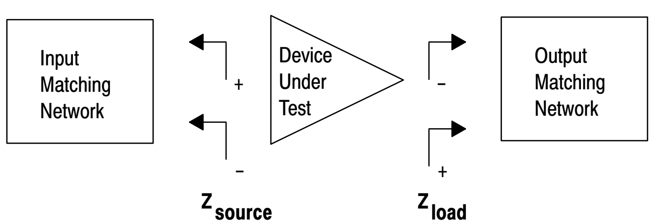
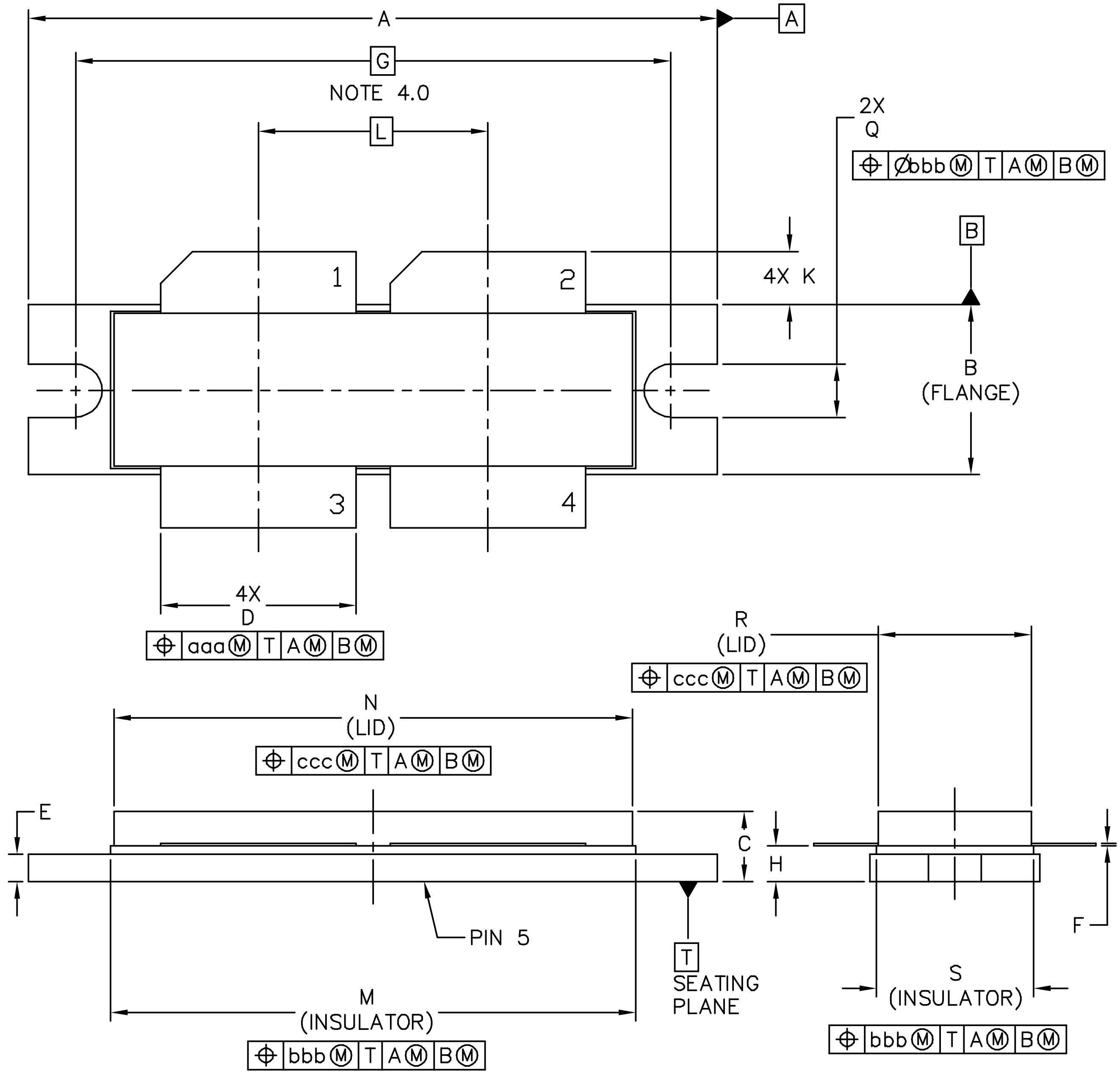


Figure 15. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



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	CASE NUMBER: 375D–05		31 MAR 2005
	STANDARD: NON–JEDEC		

NOTES:

1.0 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

2.0 CONTROLLING DIMENSION: INCH

3.0 DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

4.0 RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

STYLE 1:
PIN 1 - DRAIN
2 - DRAIN
3 - GATE
4 - GATE
5 - SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	1.615	1.625	41.02	41.28	N	1.218	1.242	30.94	31.55
B	.395	.405	10.03	10.29	Q	.120	.130	3.05	3.3
C	.150	.200	3.81	5.08	R	.355	.365	9.01	9.27
D	.455	.465	11.56	11.81	S	.365	.375	9.27	9.53
E	.062	.066	1.57	1.68					
F	.004	.007	0.1	0.18					
G	1.400 BSC		35.56 BSC		aaa	.013		0.33	
H	.082	.090	2.08	2.29	bbb	.010		0.25	
K	.117	.137	2.97	3.48	ccc	.020		0.51	
L	.540 BSC		13.72 BSC						
M	1.219	1.241	30.96	31.52					

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PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2008	• Initial Release of Data Sheet
1	Apr. 2008	• Corrected description and part number for the R1 resistor and updated R2 resistor to latest RoHS compliant part number in Table 5, Test Circuit Component Designations and Values, p. 3. • Added Fig. 12, Maximum Transient Thermal Impedance, p. 6
2	July 2008	• Added MTTF CW graph, Fig. 13, MTTF versus Junction Temperature, p. 6
3	Sept. 2008	• Added Note to Fig. 4, Capacitance versus Drain-Source Voltage, to denote that each side of device is measured separately, p. 5 • Updated Fig. 5, DC Safe Operating Area, to clarify that measurement is on a per-side basis, p. 5 • Corrected Fig. 13, MTTF versus Junction Temperature – CW, to reflect the correct die size and increased the MTTF factor accordingly, p. 6 • Corrected Fig. 14, MTTF versus Junction Temperature – Pulsed, to reflect the correct die size and increased the MTTF factor accordingly, p. 6
4	Dec. 2008	• Fig. 15, Series Equivalent Source and Load Impedance, corrected Z_{source} copy to read “Test circuit impedance as measured from gate to gate, balanced configuration” and Z_{load} copy to read “Test circuit impedance as measured from drain to drain, balanced configuration”, p. 7

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