MRF24J40

MRF24J40 Silicon Errata

The MRF24J40 parts you have received conform functionally to the Device Data Sheet (DS39776**A**), except for the anomalies described below. Any data sheet clarification issues related to this device will be reported in a separate data sheet errata. Please check the Microchip web site for any existing issues.

1. Module: RX MAC

If the RX filter is configured for Promiscuous mode, packets with a reserved packet type in the MAC frame type field may cause the RX module to put an incorrect packet length in the RX buffer.

Work around

When operating in Promiscuous mode, flush the RX buffer by setting the RXFLUSH bit (RXFLUSH<0>) after every RX interrupt.

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: SPI Interface

Following operations on the SPI interface, the SDO pin is not released to a high-impedance state after the $\overline{CS}$ pin returns to its inactive (high) state.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Security Module

When the device is performing encryption or decryption, there is a very small chance that the encryption or decryption result may be incorrect.

Work around

During decryption operations, repeat the decryption one or more times if a MIC error is indicated on the first attempt.

During encryption operations, verify the encryption by immediately decrypting the packet and checking it against the original for errors. If an error is found, repeat the encryption and verification.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: TX/RX PHY

The device does not always immediately lock on a new channel when a channel selection is made.

Work around

Set and then clear the RFRST bit (RFCTL<2>). This resets the RF module and causes the channel selection to lock immediately.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: SPI Interface

When reading from the RX FIFO or TX FIFO, there is a slight probability of reading an incorrect value.

Work around

Set bit 7 of Short register 0x18 to '0'.

This bit needs to be cleared after any device Reset.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (12/2006)

Original revision. Silicon errata issues 1 (RX MAC), 2 (SPI Interface), 3 (Security Module) and 4 (TX/RX PHY).

Rev B Document (4/2007)

Added silicon issue 5 (SPI Interface).

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