

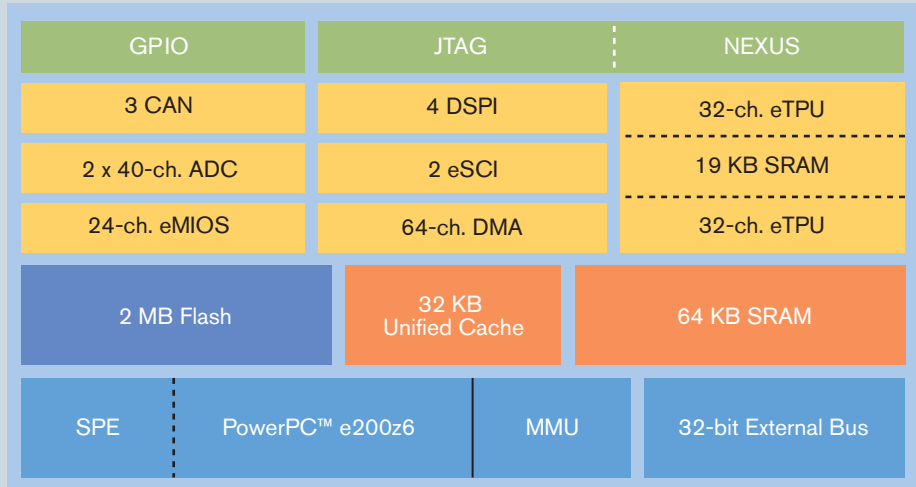
MPC5554

The MPC5554 32-bit embedded controller is the first device from Freescale Semiconductor's MPC55xx Family. Containing the Book E compliant PowerPC™ core, the MPC5554 is ideal for any application that requires complex, real-time control. It offers system performance of up to five times that of its MPC500 predecessors, while bringing you the reliability and familiarity of the proven PowerPC architecture. The MPC5554 helps you face the dual pressures of controlling costs while designing for increasingly complex applications. This high-performance MCU delivers more on-chip functionality than the current MPC500 Family; the largest amount of embedded Flash offered from Freescale to date; enhanced timer systems and a peripheral set specifically tailored for automotive and industrial applications. The MPC5554 offers a migration path from the market-leading MPC500 Family of 32-bit MCUs, facilitating reuse of legacy software architectures.

Applications

- > Multipoint fuel injection control
- > Electronically controlled transmissions
- > Direct diesel injection (DDI)
- > Gasoline direct injection (GDI)
- > Avionics
- > Robotics
- > Motion control
- > Turbine control
- > Utilities/power management
- > Alternative energies
- > Autonomous vehicles

MPC5554 BLOCK DIAGRAM



Features

Freescale's e200z6 Core

- > High-performance 132 MHz 32-bit PowerPC Book E-compliant core
- > Memory management unit (MMU) with 32-entry fully associative translation lookaside buffer (TLB)
- > Signal processing extension (SPE): DSP, SIMD and floating point capabilities

Memory

- > 2 MB of embedded Flash memory with Error Correction Coding (ECC) and Read While Write capability (RWW)
- > 64 KB on-chip static RAM with ECC
- > 32 KB of cache (with line-locking) that can be configured as additional RAM

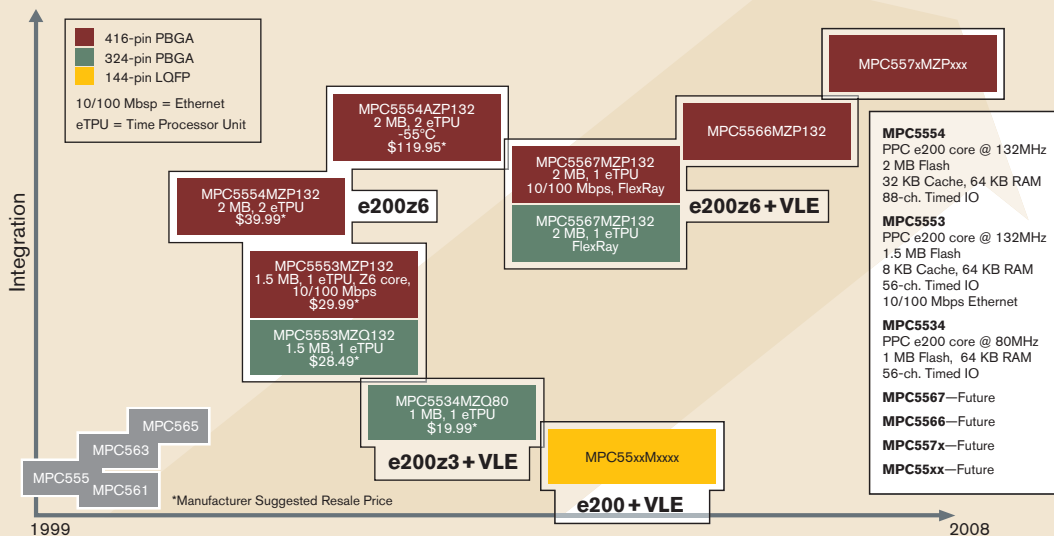
System

- > Two enhanced time processor units (eTPUs) with 64 I/O channels and 19 KB of designated SRAM

- > 64-channel eDMA (Enhanced Direct Memory Access) controller
- > Interrupt controller (INTC) capable of handling 286 selectable-priority interrupt sources
- > Frequency modulated phase-locked loop (FMPPLL) to assist in electromagnetic interference (EMI) management
- > MPC500 compatible external bus interface
- > Nexus IEEE-ISTO 5001™ Class 3+ multicore debug capabilities
- > 5/3.3V IO, 5V ADC, 3.3V/1.8V bus, 1.5V core
- > 416-pin PBGA package
- > Temperature range: -40 to 125°C
- > Optional temperature range: -55 to 125°C

- 416-pin PBGA
- 324-pin PBGA
- 144-pin LQFP

10/100 Mbps = Ethernet
eTPU = Time Processor Unit



Except for historical information, all of the expectations and assumptions contained in the foregoing are forward-looking statements involving risk and uncertainties. Important factors that could cause actual results to differ materially from such forward-looking statements include, but are not limited to, the competitive environment for our products, changes of rates of all related services, and legislation that may affect the industry. For additional information regarding these and other risks associated with the company's business, refer to the company's reports with the SEC.

- > 40-ch. dual enhanced queued analog-to-digital converter (eQADC—up to 12-bit resolution and up to 1.25ms conversions, six queues with triggering and DMA support
- > Four deserial serial peripheral interface (DSPI) modules—16 bits wide up to six chip selects each
- > Three controller area network (CAN) modules with 64 buffers each
- > Two enhanced serial communication interface (eSCI) modules
- > 24-ch. enhanced multiple I/O system (EMIOS) with unified channels

Excellent system performance:
Book E superscalar compliant with the PowerPC core includes integrated DSP features and upgraded interrupt control

Cost-effectiveness:
Integrates more functionality on-chip. Functions previously performed in external analog hardware have been moved into software.

Supports multiple protocols and customer requirements through intelligent subsystems

Core- and platform-based architecture enables simple derivative development. Leverages past engineering investments and existing PowerPC architecture knowledge to create a solid migration path for MPC500 users.

5V interfaces to allow use of legacy sensor and I/O systems

A comprehensive suite of hardware and software development tools for the MPC5554 is available to help simplify and speed system design. Development support is available through leading independent tools vendors providing compilers, debuggers, simulation environments, as well as other more advanced or specific development tools. In addition to the standard evaluation kit

For more information, please contact your local Freescale sales office.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.
The "PowerPC" name is a trademark of IBM Corp. and used under license.
© Freescale Semiconductor, Inc. 2005

Document Number:XXXXXXX
REV 0

