MIC22200

2A Integrated Switch Synchronous Buck Regulator with Frequency Programmable from 800kHz to 4MHz

General Description

The Micrel MIC22200 is a high efficiency, 2A integrated switch synchronous buck (step-down) regulator. The MIC22200 switching frequency is programmable from 800kHz to 4MHz, allowing the customer to optimize their designs either for efficiency or for the smallest footprint. The regulator achieves efficiencies as high as 95% while still switching at 1MHz over a broad load range.

The ultra high speed control loops keep the output voltage within regulation even under the extreme transient load swings commonly found in FPGAs and low-voltage ASICs.

The output voltage can be adjusted down to 0.7V to address all low voltage power needs.

The MIC22200 offers a full range of sequencing and tracking options. The Enable/Delay pin, combined with the POR pin, allows multiple outputs to be sequenced in many ways during turn on and turn off. The RC (ramp control) pin allows the device to be connected to another device in the MIC22X00 family of products to keep the output voltages within a certain delta V on start up.

The MIC22200 is available in a 3mm × 3mm 12-lead MLF® package with a junction operating range from –40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

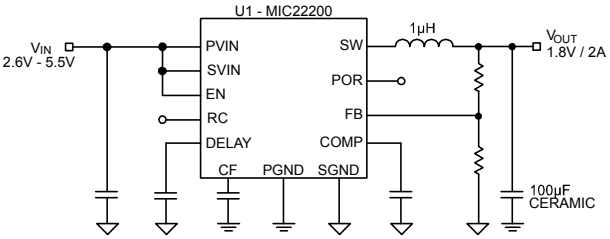
Features

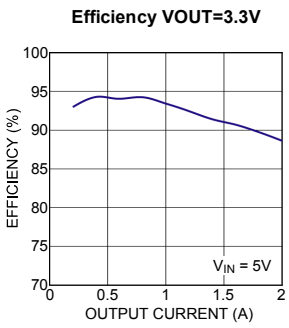
- Input voltage range: 2.6V to 5.5V
- Adjustable output voltage option down to 0.7V
- Output current to 2A
- Full sequencing and tracking capability
- Easy RC compensation
- Power On Reset
- Efficiency > 90% across a broad load range
- Operating frequency: Programmable from 800 kHz up to 4MHz
- Ultra fast transient response
- 100% maximum duty cycle
- Fully integrated MOSFET switches
- Micropower shutdown
- Thermal shutdown and current limit protection
- Available in Pb-free 3mm × 3mm MLF-12-lead MLF® Package
- –40°C to +125°C junction temperature range

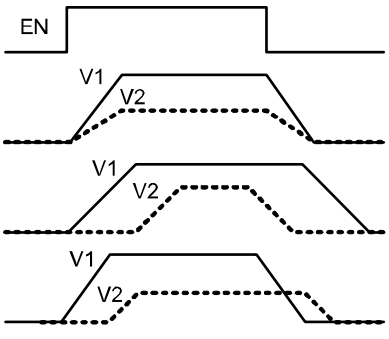
Applications

- High power density point of load conversion
- Servers/routers
- DVD recorders and multimedia players
- Computing peripherals
- Base stations
- FPGAs, DSP and low voltage ASIC devices

Typical Application







Ordering Information

Part Number	Nominal Output Voltage	Junction Temp. Range(1)	Package	Lead Finish
MIC22200YML	Adjustable	-40°C to +125°C	3mm×3mm 12-Lead MLF®	Lead Free(1)

Note.

1. MLF® is a green RoHs compliant package. Lead finish is NiPdAu. Mold compound is halogen free.

Pin Configuration

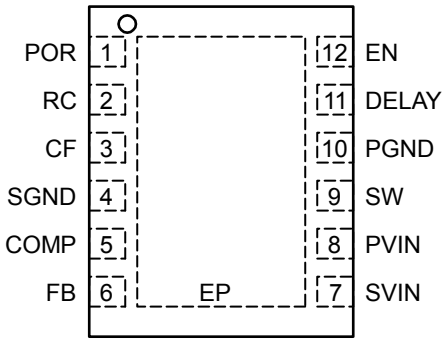


Figure 2. 12-Lead MLF® (ML)

Pin Description

Pin Number	Pin Name	Pin Function
1	POR	Power On Reset (output): Open drain output device indicates when the output is out of regulation and is active after the delay set by the delay pin.
2	RC	Ramp Control. Capacitor to GND from this pin determines the slew rate of output voltage during start-up. This can be used for tracking capability as well as for soft start.
3	CF	External capacitor to adjust switching frequency.
4	SGND	Signal Ground (signal): Ground (GND)
5	COMP	Compensation Pin (input): Placing an RC to GND will compensate the device. See Applications section.
6	FB	Feedback (input): Input to the error amplifier; connected to the external resistor divider network to set the output voltage.
7	SVIN	Signal Power Supply Voltage (input): Requires bypass capacitor to GND.
8	PVIN	Power Supply Voltage (input): Requires bypass capacitor to GND.
9	SW	Switch (output): From internal power MOSFET output switches.
10	PGND	Power Ground (power): Ground (GND)
11	DELAY	Delay (input)
12	EN	Enable (Input): When this pin is pulled higher than the enable threshold, the part will start up. Below this voltage the device is in its low quiescent current mode. The pin has a 1µA current source charging it to VIN. By adding a capacitor to this pin a delay may easily be generated. The enable function will not operate with an input voltage lower than the min specified.
EPad	GND	Exposed Pad (Power): You must make a full connection to a GND plane for full output power to be released.

Absolute Maximum Ratings[1]

Supply Voltage (P_{VIN}, S_{VIN}).....+6V
Output Switch (SW).....6V
Logic Voltage (EN, POR, DELAY) .....VIN to -0.3V
Control Voltage (CF, RC, COMP, FB) .....VIN to -0.3V
Storage Temperature Range (Ts).....-65°C to +150°C
EDS Rating[3].....2kV

Operating Ratings[2]

Supply Voltage (V_{IN})..... +2.6V to +5.5V
Junction Temperature Range (T_J)..... -40°C ≤ T_J ≤ +125°C
Thermal Resistance
3mm × 3mm MLF-12L (θ_{JA}).....40°C/W

Electrical Characteristics[4]

T_A = 25°C with V_{IN} = V_{EN} = 3.3V, unless otherwise specified. Bold values indicate -40°C ≤ T_J ≤ +125°C

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage Range		**2.6**		**5.5**	V
Under-Voltage Lockout Threshold	(turn-on)	**2.4**	2.5	**2.6**	V
UVLO Hysteresis			280		mV
Quiescent Current, PWM mode	V_{EN} ≥1.34V; V_{FB} = 0.9V		1.2	**2**	mA
Shutdown Current	V_{EN} = 0V		3.7	**10**	µA
Feedback Voltage	± 2% (over temperature)	**0.686**	0.7	**0.714**	V
Oscillator Frequency		**0.8**	1	**1.2**	MHz
FB pin input current			1		nA
Current Limit in PWM Mode	V_{FB} = 0.9*VNOM	4.5	5.5	6.5	A
Output Voltage Line Regulation	V_{IN} = 2.6V to 5.5V		0.2		%
Output Voltage Load Regulation	100mA < I_{LOAD} < 2A, V_{IN} = 3.3V		0.2		%
Maximum Duty Cycle	VFB ≤ 0.5V	100			%
Switch ON-Resistance PFET Switch ON-Resistance NFET	I_{SW} = 1000mA V_{FB}=0.5V I_{SW} = -1000mA V_{FB}=0.9V		0.18 0.10		Ω
EN threshold voltage	V_{IN}=3.3V	**1.14**	1.24	**1.34**	V
EN hysteresis			12		mV
DLY threshold voltage	V_{IN}=3.3V	**1.14**	1.24	**1.34**	V
DLY hysteresis			6		mV
EN/DLY source current	V_{IN} = 2.6 to V_{IN} = 5.5V	**0.7**	1	**1.3**	µA
RC source current	Ramp Control Current	**0.7**	1	**1.3**	µA
Power On Reset IPG(LEAK)	V_{PORH} = 5.5V; POR = High			1 **2**	µA µA
Power On Reset VPG(LO)	Output Logic-Low Voltage (undervoltage condition), I_{POR} = 5mA		135		mV
Power On Reset VPG	Threshold, % of Vout below nominal	**7.5**	10	**12.5**	%
	Hysteresis		1		%
Over-temperature Shutdown			160		°C
Over-temperature Shutdown Hysteresis			25		°C

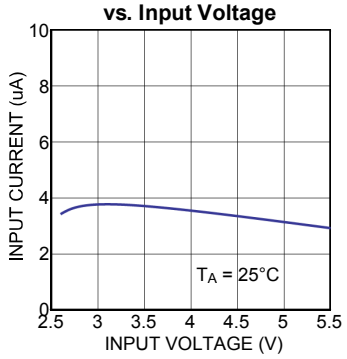
Notes:

1. Exceeding the absolute maximum rating may damage the device.

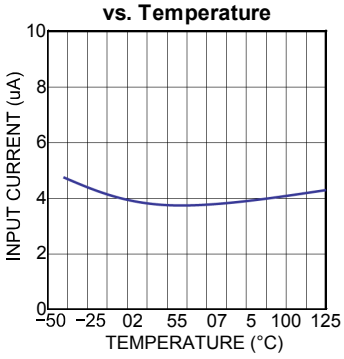
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Specification for packaged product only.

Typical Characteristics

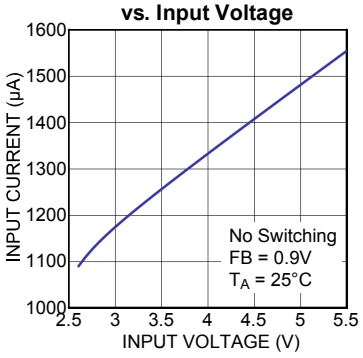
Shutdown Current vs. Input Voltage



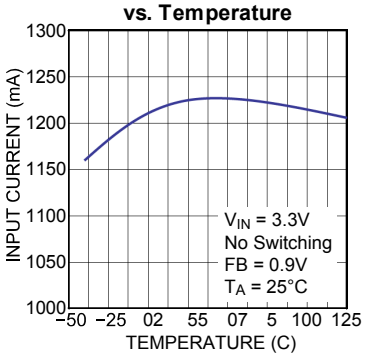
Shutdown Current vs. Temperature



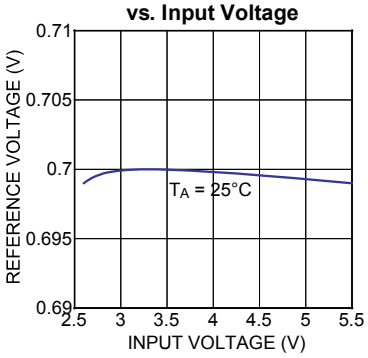
Operating Current vs. Input Voltage



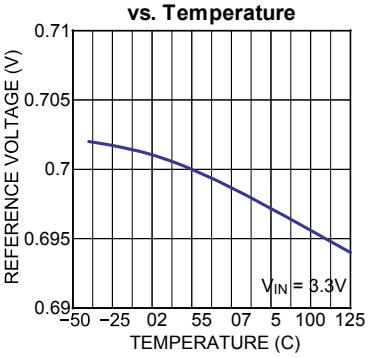
Operating Current vs. Temperature



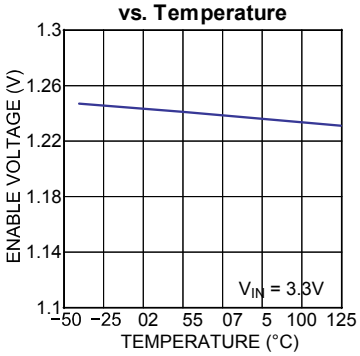
Reference Voltage vs. Input Voltage



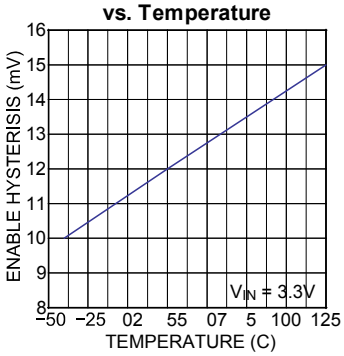
Reference Voltage vs. Temperature



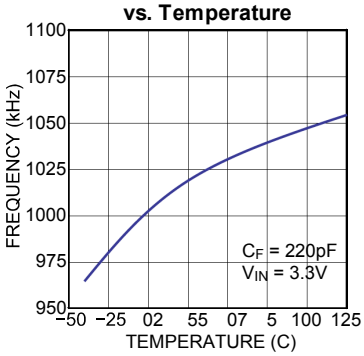
Enable Voltage vs. Temperature



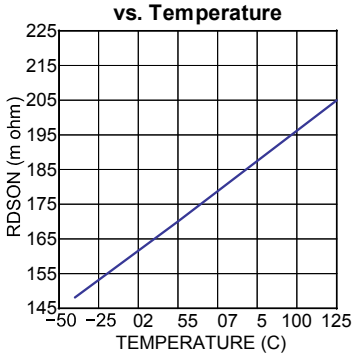
Enable Hysterisis vs. Temperature



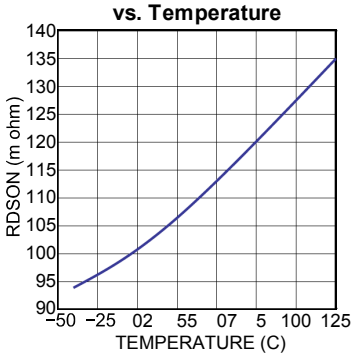
Frequency vs. Temperature



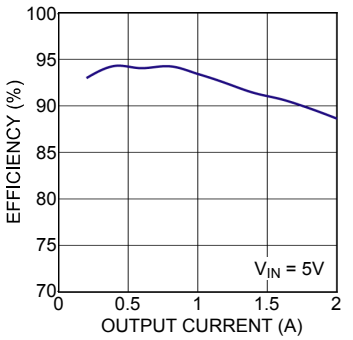
P-Channel RDSON vs. Temperature



N-Channel RDSON vs. Temperature

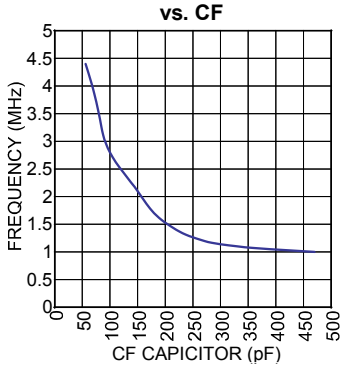


Efficiency VOUT=3.3V

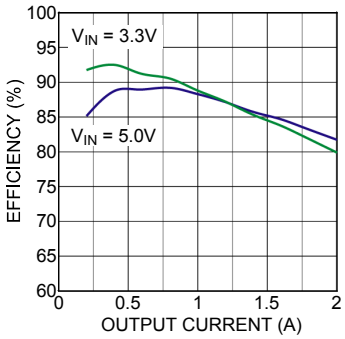


Typical Characteristics

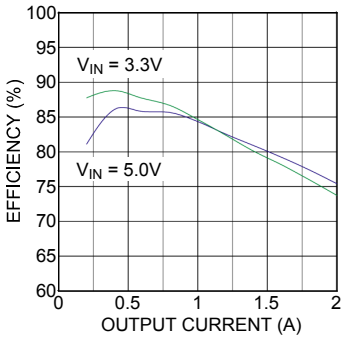
Frequency vs. CF



Efficiency VOUT=1.8V

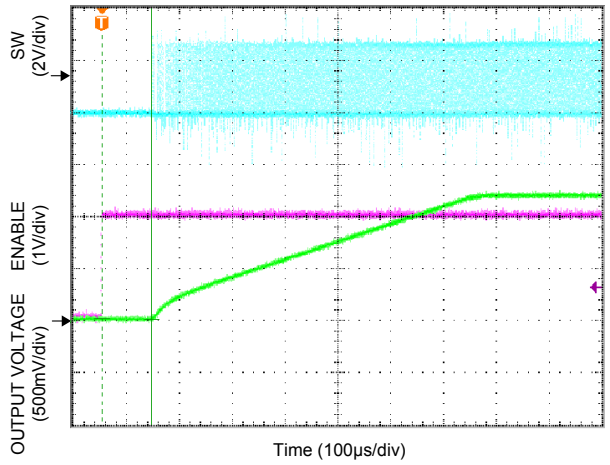


Efficiency VOUT=1.2V

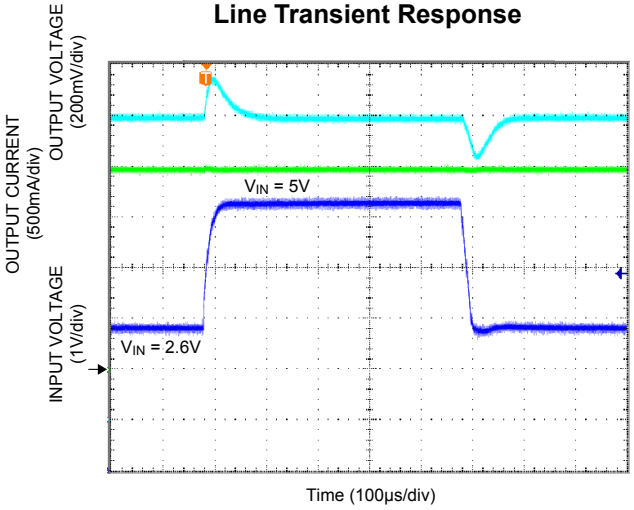


Functional Characteristics

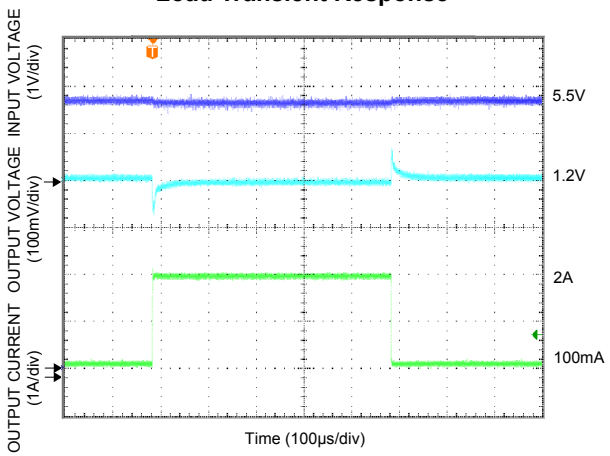
Enable On



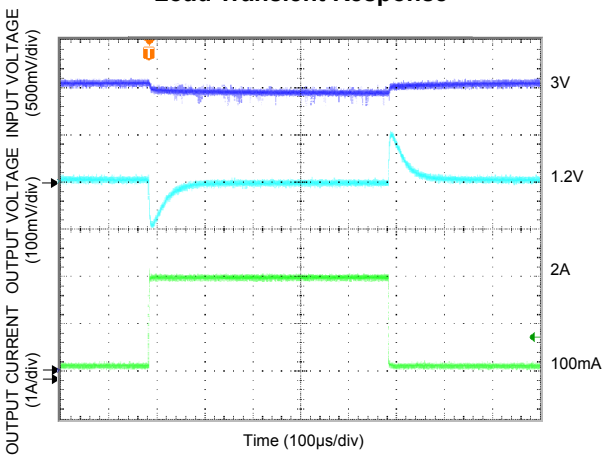
Line Transient Response



Load Transient Response



Load Transient Response



Functional Diagram

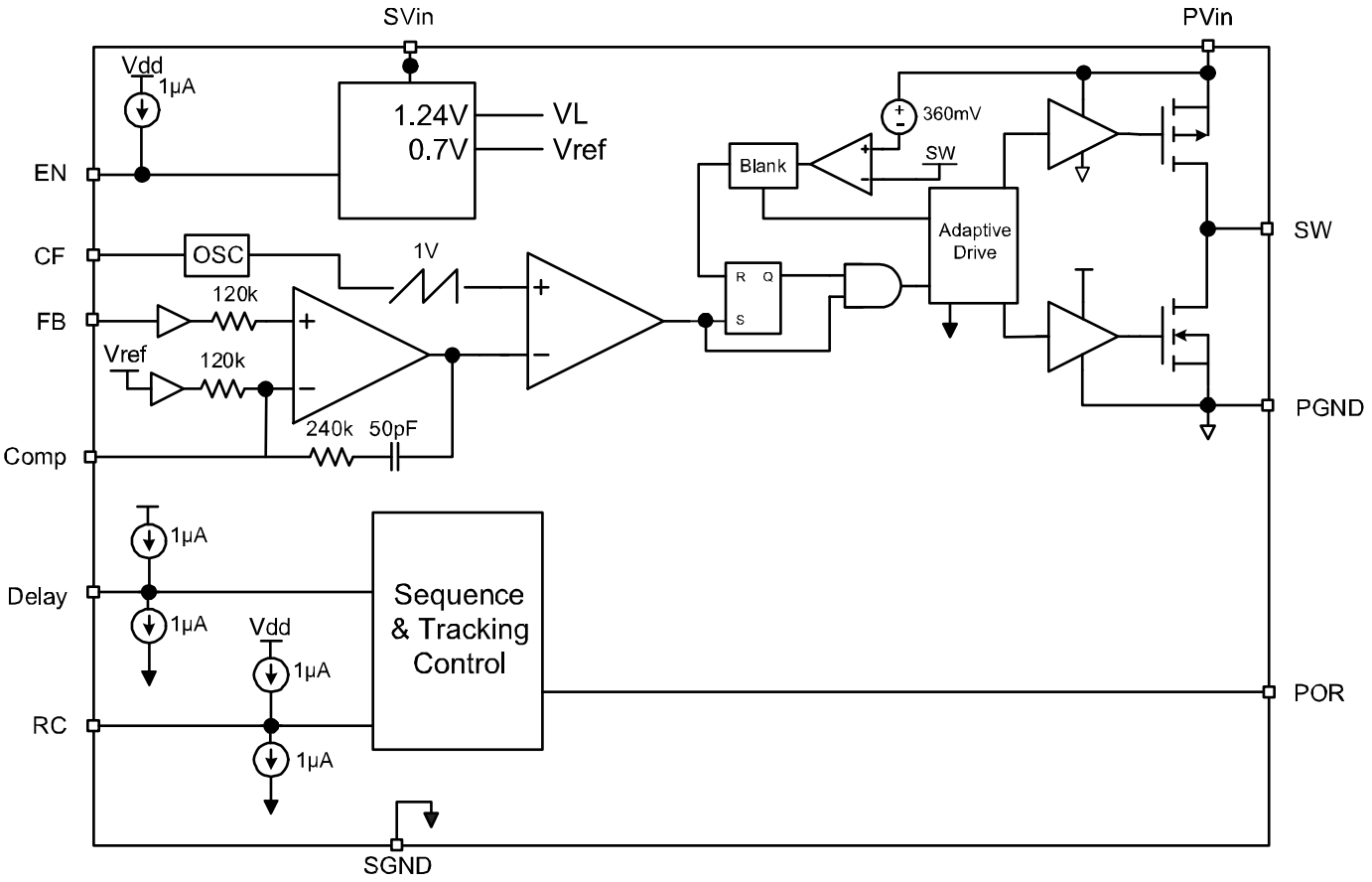


Figure 1. MIC22200 Functional Diagram

Functional Description

PVIN, SVIN

PVIN is the input supply to the internal 180mΩ P-Channel Power MOSFET. This should be connected externally to the SVIN pin. The supply voltage range is from 2.6V to 5.5V. A 10µF ceramic is recommended for bypassing the PVIN supply.

EN

This pin is internally fed with a 1µA current source to VIN. A delayed turn on is implemented by adding a capacitor to this pin. The delay is proportional to the capacitor value. The internal circuits are held off until EN reaches the enable threshold of 1.24V.

RC

RC allows the slew rate of the output voltage to be programmed by the addition of a capacitor from RC to ground. RC is internally fed with a 1µA current source and VOUT slew rate is proportional to the capacitor and the 1µA source.

Delay

Adding a capacitor to this pin allows the delay of the POR signal.

When VOUT reaches 90% of its nominal voltage, the Delay pin current source (1µA) starts to charge the external capacitor. At 1.24V, POR is asserted high.

Comp

The MIC22200 uses an internal compensation network containing a fixed frequency zero (phase lead response) and pole (phase lag response) which allows the external compensation network to be much simplified for stability. The addition of a single capacitor and resistor will add the necessary pole and zero for voltage mode loop stability using low value, low ESR ceramic capacitors.

FB

The feedback pin provides the control path to control the output. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage. Refer to the feedback section in the “Applications Information” section for more detail.

POR

This is an open drain output. A 47k resistor can be used for a pull up to this pin. POR is asserted high when output voltage reaches 90% of nominal set voltage and after the delay set by CDELAY. POR is asserted low without delay when enable is set low or when the output goes below the -10% threshold. For a Power Good (PG) function, the delay can be set to a minimum. This can be done by removing the Delay capacitor.

SW

This is the connection to the drain of the internal P-Channel MOSFET and drain of the N-Channel MOSFET. This is a high frequency high power connection; therefore traces should be kept as short and as wide as practical.

CF

Adding a capacitor to this pin can adjust switching frequency from 800kHz to 4MHz. The CF capacitor must be connected between the CF pin and power ground.

SGND

Internal signal ground for all low power sections.

PGND

Internal ground connection to the source of the internal N-Channel MOSFETs.

Application Information

The MIC22200 is a 2A Synchronous step down regulator IC with an adjustable switching frequency from 800kHz to 4MHz, voltage mode PWM control scheme. The other features include tracking and sequencing control for controlling multiple output power systems, power on reset.

Component Selection

Input Capacitor

A minimum 10µF ceramic is recommended on each of the PVIN pins for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics, aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

Output Capacitor

The MIC22200 was designed specifically for the use of ceramic output capacitors and 22µF is optimum output capacitor. 22µF can be increased to 100µF to improve transient performance. Since the MIC22200 is in voltage mode, the control loop relies on the inductor and output capacitor for compensation. For this reason, do not use excessively large output capacitors. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies. Using Y5V or Z5U capacitors can cause instability in the MIC22200.

Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

Inductance

Rated current value

Size requirements

DC resistance (DCR)

The MIC22200 is designed for use with a 0.47µH to 4.7µH inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. The ripple can add as much as 1.2A to the output current level. The RMS rating should be chosen to be equal or greater than the Current Limit of the MIC22200 to prevent overheating in a fault condition. For best electrical performance, the inductor should be placed very close to the SW nodes of the IC. For this reason, the heat of the inductor is somewhat coupled to the IC, so it offers some level of protection if the inductor gets too hot. It is important to test all operating limits before settling on the final inductor choice.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their datasheet.

DC resistance is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the “Efficiency Considerations” below for a more detailed description.

Enable Capacitor

Enable sources 1µA out of the IC to allow a startup delay to be implemented. The delay time is simply the time it takes 1µA to charge C_{DLY} to 1.25V. Therefore:

$$T_{DLY} = \frac{1.24 \cdot C_{DLY}}{1.10^{-6}}$$

CF Capacitor

Adding a capacitor to this pin can adjust switching frequency from 800kHz to 4MHz. CF sources 400µA out of the IC to charge the CF capacitor to set up the switching frequency. The switch period is simply the time it takes 400µA to charge CF to 1.0V (±2%). Therefore:

Capacitor CF	Frequency
56pF	4.4MHz
68pF	4MHz
82pF	3.4MHz
100pF	2.8MHz
150pF	2.1MHz
180pF	1.7MHz
220pF	1.4MHz
270pF	1.2MHz
330pF	1.1MHz
390pF	1.05MHz
470pF	1MHz

Table 1. CF vs. Frequency

It is necessary to connect the CF capacitor between the CF pin and power ground.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power consumed.

$$\text{Efficiency \%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

Maintaining high efficiency serves two purposes. It decreases power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it decreases consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time, critical in hand held devices.

There are mainly two loss terms in switching converters: static losses and switching losses. Static losses are simply the power losses due to VI or I^2R. For example, power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET RDS(ON) multiplied by the RMS Switch Current squared (ISW^2). During the off cycle, the low side N-Channel MOSFET conducts, also dissipating power. Similarly, the inductor's DCR and capacitor's ESR also contribute to the I^2R losses. Device operating current also reduces efficiency by the product of the quiescent (operating) current and the supply voltage. The current required to drive the gates on and in the frequency range from 800kHz to 4MHz and the switching transitions make up the switching losses.

Figure 2 shows an efficiency curve. The portion, from 0A to 0.2A, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. In this case, lower supply voltages yield greater efficiency in that they require less current to drive the MOSFETs and have reduced input power consumption.

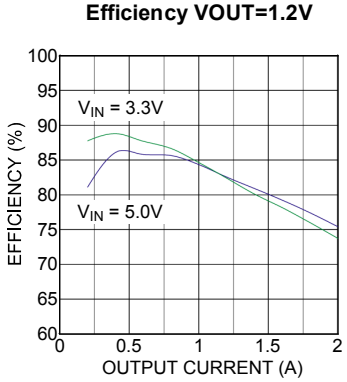


Figure 2. Efficiency Curve

The region, 0.2A to 2A, efficiency loss is dominated by MOSFET RDSON and inductor DC losses. Higher input supply voltages will increase the Gate-to-Source voltage on the internal MOSFETs, reducing the internal RDSON. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows;

$$L_{PD} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \cdot I_{OUT}}{(V_{OUT} \cdot I_{OUT}) + L_{PD}}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

Alternatively, under lighter loads, the ripple current due to the inductance becomes a significant factor. When light load efficiencies become more critical, a larger inductor value may be desired. Larger inductances reduce the peak-to-peak inductor ripple current, which minimize losses. The following graph in Figure 3 illustrates the effects of inductance value at light load.

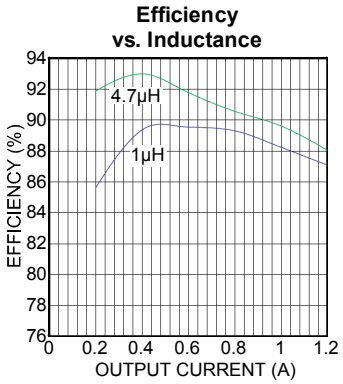


Figure 3. Efficiency vs. Inductance

Compensation

The MIC22200 has a combination of internal and external stability compensation to simplify the circuit for small, high efficiency designs. In such designs, voltage mode conversion is often the optimum solution. Voltage mode is achieved by creating an internal 1MHz ramp signal and using the output of the error amplifier to modulate the pulse width of the switch node, thereby maintaining output voltage regulation. With a typical gain bandwidth of 100-200kHz, the MIC22200 is capable of extremely fast transient responses.

The MIC22200 is designed to be stable with a typical application using a 1µH inductor and a 47µF ceramic (X5R) output capacitor. These values can be varied dependant upon the tradeoff between size, cost and efficiency, keeping the LC natural frequency $\left(\frac{1}{2 \cdot \Pi \cdot \sqrt{L \cdot C}}\right)$ ideally less than 26kHz to ensure stability

can be achieved. The minimum recommended inductor value is 0.47µH and minimum recommended output capacitor value is 22µF. The tradeoff between changing these values is that with a larger inductor, there is a reduced peak-to-peak current which yields a greater efficiency at lighter loads. A larger output capacitor will improve transient response by providing a larger hold up reservoir of energy to the output.

The integration of one pole-zero pair within the control loop greatly simplifies compensation. The optimum values for C_{COMP} (in series with a 20k resistor) are shown below.

C→ / L↓	22-47µF	47µF-100µF	100µF-470µF
0.47µH	0*-10pF	22pF	33pF
1µH	0†-15pF	15-22pF	33pF
2.2µH	15-33pF	33-47pF	100-220pF
* VOUT > 1.2V, † VOUT > 1V			

Table 2. Compensation Capacitor Selection

Feedback

The MIC22200 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.7V reference voltage and adjusts the output voltage to maintain regulation. The resistor divider network for a desired VOUT is given by:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

where VREF is 0.7V and VOUT is the desired output voltage. A 10kΩ or lower resistor value from the output to the feedback is recommended since large feedback resistor values increase the impedance at the feedback pin, making the feedback node more susceptible to noise pick-up. A small capacitor (50pF – 100pF) across the lower resistor can reduce noise pick-up by providing a low impedance path to ground.

PWM Operation

The MIC22200 is a voltage mode, pulse width modulation (PWM) controller. By controlling the ratio of on-to-off time, or duty cycle, a regulated DC output voltage is achieved. As load or supply voltage changes, so does the duty cycle to maintain a constant output voltage. In cases where the input supply runs into a dropout condition, the MIC22200 will run at 100% duty cycle.

The MIC22200 provides constant switching from 800kHz to 4MHz with synchronous internal MOSFETs. The internal MOSFETs include a 180mΩ high-side P-Channel MOSFET from the input supply to the switch pin and a 100mΩ N-Channel MOSFET from the switch pin-to-ground. Since the low-side N-Channel MOSFET provides the current during the off cycle, a freewheeling Schottky diode from the switch node-to-ground is not required.

PWM control provides fixed frequency operation. By maintaining a constant switching frequency, predictable fundamental and harmonic frequencies are achieved. Other methods of regulation, such as burst and skip modes, have frequency spectrums that change with load that can interfere with sensitive communication equipment.

Sequencing and Tracking

The MIC22200 provides additional pins to provide up/down sequencing and tracking capability for connecting multiple voltage regulators together.

Enable Pin

The Enable pin contains a trimmed, 1µA current source which can be used with a capacitor to implement a fixed desired delay in some sequenced power systems. The threshold level for power on is 1.24V with a hysteresis of 20mV.

Delay Pin

The Delay pin also has a 1µA trimmed current source and a 1µA current sink which acts with an external capacitor to delay the operation of the Power On Reset (POR) output. This can be used also in sequencing outputs in a sequenced system, but with the addition of a conditional delay between supplies; allowing a first up, last down power sequence.

After Enable is driven high, VOUT will start to rise (rate determined by RC capacitor). As the FB voltage goes above 90% of its nominal set voltage, Delay begins to rise as the 1µA source charges the external capacitor. When the threshold of 1.24V is crossed, POR is asserted high and Delay continues to charge to a voltage VDD. When FB falls below 90% of nominal, POR is asserted low immediately. However, if enable is driven low, POR will fall immediately to the low state and Delay will begin to fall as the external capacitor is discharged by the 1µA current sink. When the threshold of VDD-1.24V is crossed, VOUT will begin to fall at a rate determined by the RC capacitor. As the voltage change in both cases is 1.24V, both rising and falling delays are matched at

$$T_{POR} = \frac{1.24 \cdot C_{DLY}}{1.10^{-6}}$$

RC Pin

The RC pin provides a trimmed 1µA current source/sink similar to the Delay Pin for accurate ramp up (soft start) and ramp down control. This allows the MIC22200 to be used in systems requiring voltage tracking or ratio-metric voltage tracking at startup.

There are two ways of using the RC pin:

Externally driven from a voltage source

Externally attached capacitor sets output ramp up/down rate

In the first case, driving RC with a voltage from 0V to VREF will program the output voltage between 0 and 100% of the nominal set voltage.

In the second case, the external capacitor sets the ramp up and ramp down time of the output voltage. The time is given by $T_{RAMP} = \frac{0.7 \cdot C_{RC}}{1.10^{-6}}$ where TRAMP is the time from 0 to 100% nominal output voltage.

Sequencing and Tracking examples

There are four distinct variations which are easily implemented using the MIC22200. The two sequencing variations are Windowed and Delayed. The two tracking variants are Normal and Ratio Metric. The following diagrams illustrate methods for connecting two MIC22200's to achieve these requirements.

Sequencing:

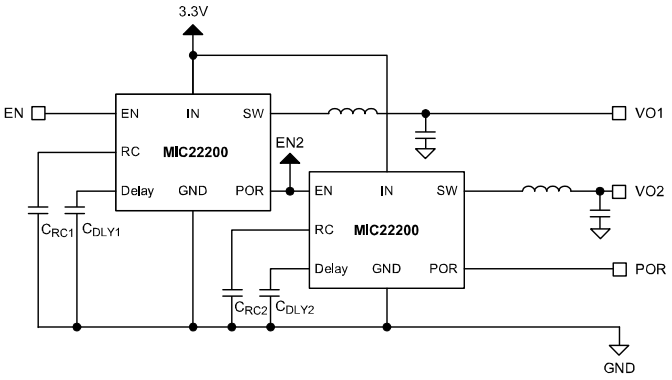


Figure 4. Sequencing MIC22200 Circuit

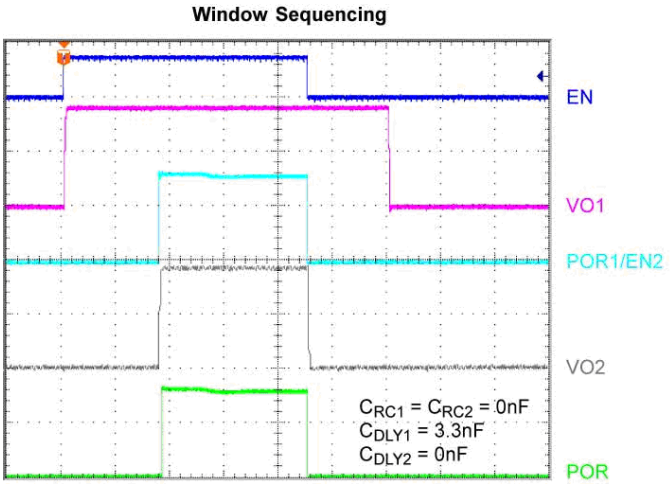


Figure 5. Window Sequencing Example

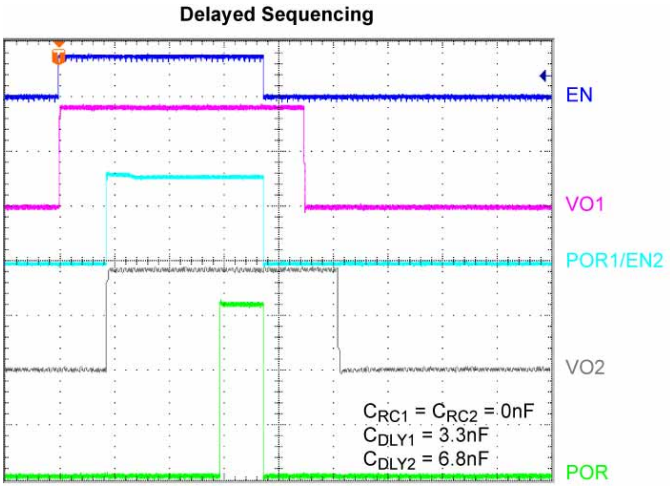


Figure 6. Delayed Sequencing Example

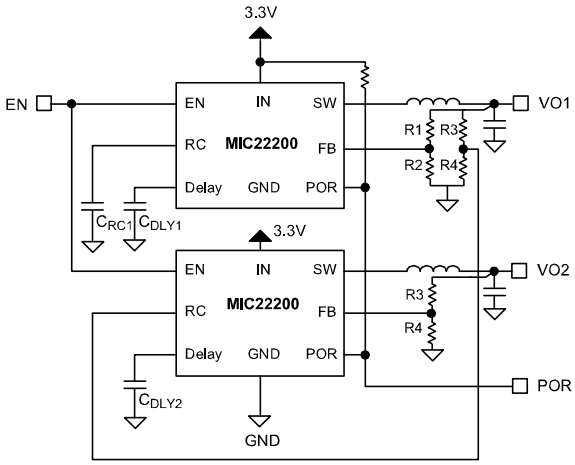


Figure 7. Normal Tracking Circuit

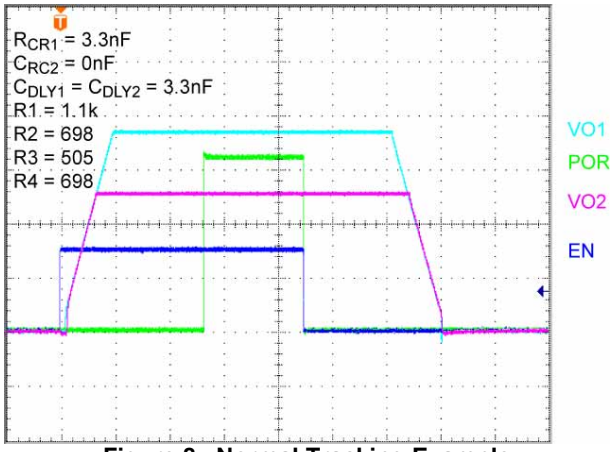


Figure 8. Normal Tracking Example

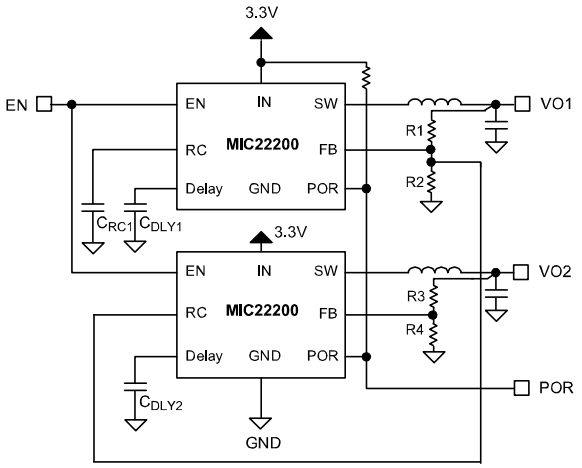


Figure 9. Radio Metric Tracking Circuit

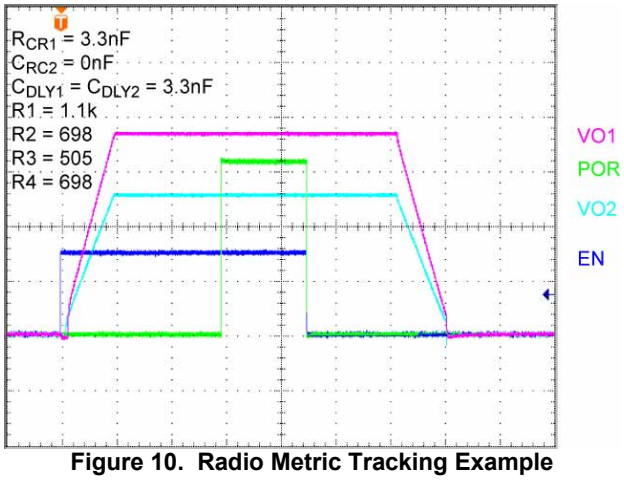


Figure 10. Radio Metric Tracking Example

An alternative method here shows an example of a VDDQ and VTT solution for a DDR memory power supply. Note that POR is taken from Vo1 as POR2 will not go high. This is because POR is set high when FB > 0.9·VREF. In this example, FB2 is regulated to ½·VREF.

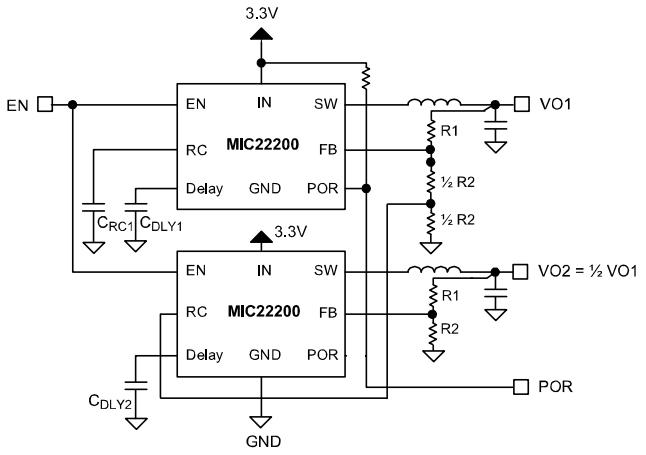


Figure 11. DDR Memory Tracking Circuit

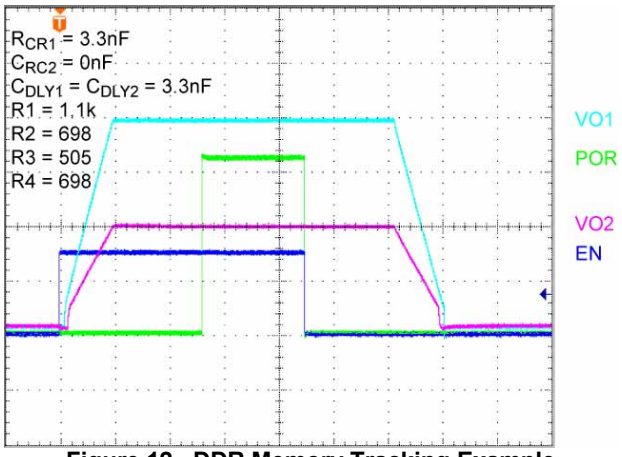


Figure 12. DDR Memory Tracking Example

Current Limit

The MIC22200 is protected against overload in two stages. The first is to limit the current in the P-channel switch; the second is over temperature shutdown.

Current is limited by measuring the current through the high side MOSFET during its power stroke and immediately switching off the driver when the preset limit is exceeded.

Figure 13 describes the operation of the current limit circuit. Since the actual RDSON of the P-Channel MOSFET varies part-to-part, over temperature and with input voltage, simple IR voltage detection is not employed. Instead, a smaller copy of the Power MOSFET (Reference FET) is fed with a constant current which is a directly proportional to the factory set current limit. This sets the current limit as a current ratio and thus, is not dependant upon the RDSON value. Current limit is set to 5.5A nominal. Variations in the scale factor K between the Power PFET and the reference PFET

used to generate the limit threshold account for a relatively small inaccuracy.

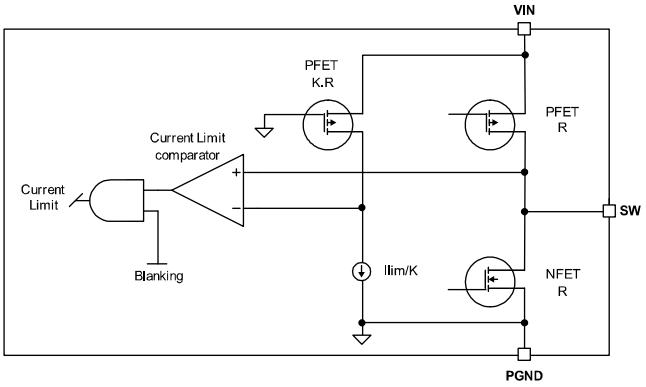


Figure 13. Current Limit Detail

Thermal Considerations

The MIC22200 is packaged in the MLF® 3mm x 3mm, a package that has excellent thermal performance equaling that of the larger TSSOP packages. This maximizes heat transfer from the junction to the exposed pad (ePAD) which connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board. The junction temperature for a given ambient temperature can be calculated using:

$$T_J = T_A + P_D \cdot R\theta_{JA}$$

Where

P_D is the power dissipated within the MLF® package and is typically 0.8W at 2A for V_{IN} = 5V and V_{OUT} = 1.8V load. This has been calculated for a 1µH inductor and details can be found in table 1 below for reference.

$R\theta_{JA}$ is a combination of junction to case thermal resistance ($R\theta_{JC}$) and Case-to-Ambient thermal resistance ($R\theta_{CA}$), since thermal resistance of the solder connection from the ePAD to the PCB is negligible; $R\theta_{CA}$ is the thermal resistance of the ground plane to ambient, so $R\theta_{JA} = R\theta_{JC} + R\theta_{CA}$.

VOUT @2A	VIN 3V	VIN 3.5V	VIN 4V	VIN 4.5V	VIN 5V
1	0.86822	0.81512	0.7836	0.77014	0.76194
1.2	0.87796	0.8247	0.79362	0.77956	0.76842
1.8	0.93972	0.86722	0.82568	0.8095	0.80076
2.5	0.91848	0.90504	0.85466	0.83296	0.81846
3.3	—	—	0.8764	0.842	0.8326

Table 3. Power Dissipation (W) for 4A Output

T_A is the Operating Ambient temperature.

Example:

To calculate the junction temperature for a 50°C ambient:

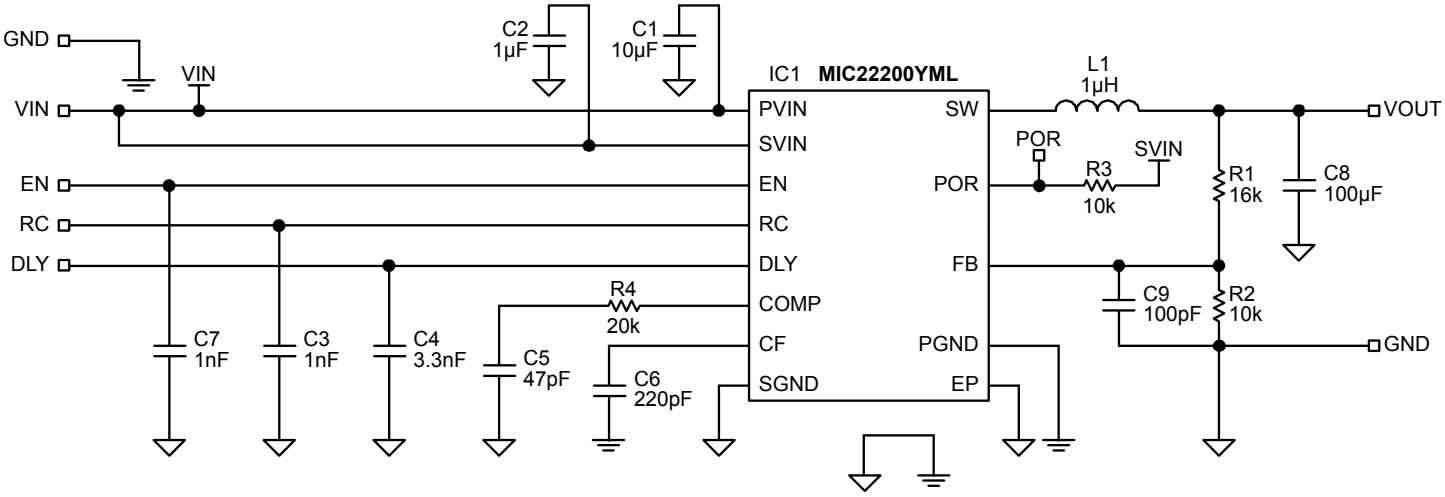
$T_J = T_A + P_{DI} . R\theta_{JA}$

$T_J = 50 + 0.8 \times 40$

$T_J = 82°C$

This is below the maximum of 125°C.

Design Example



MIC22200YML Evaluation Board Schematic

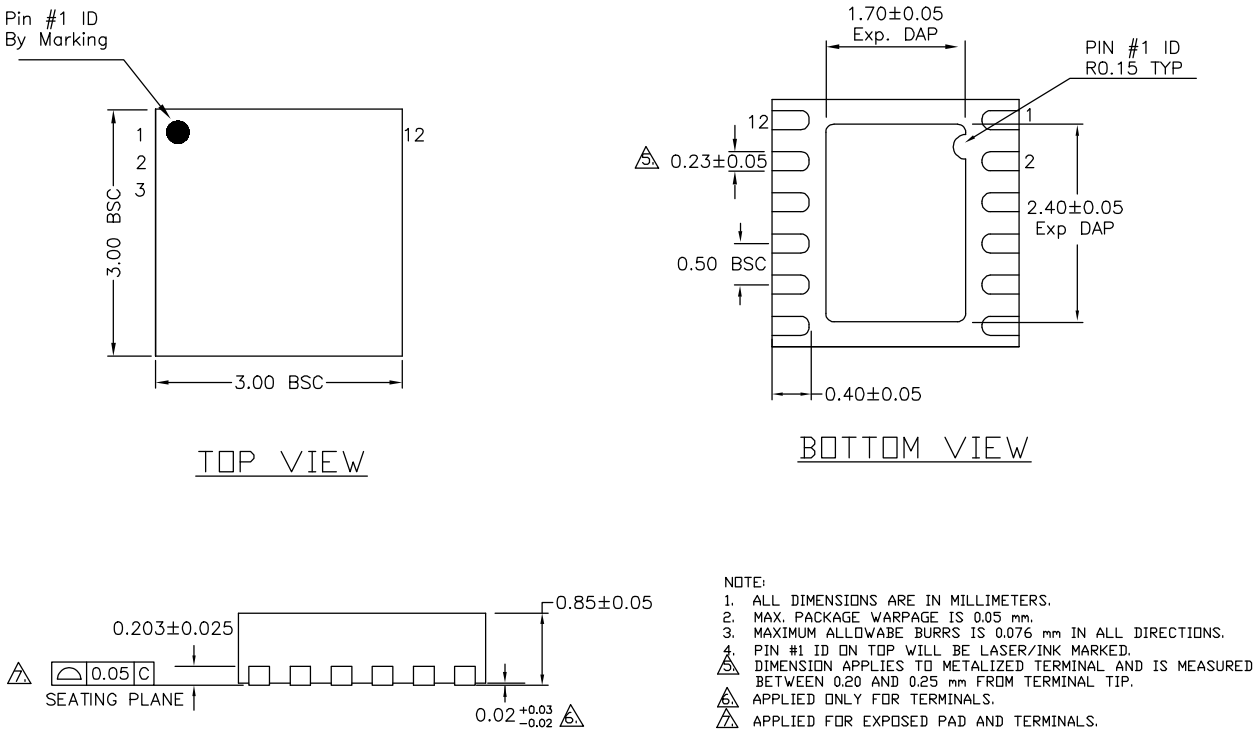
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty
C1	C2012X5R0J106K	TDK[1]	10uF/6.3V , 0805, XR5	1
	VJ0805G106KXYAT	Vishay[2]		
C2	C1608X7R1C105K	TDK	1uF /6.3V, 0603, X7R	1
	VJ0603Y105KXYAT	Vishay		
C3, C7	C1608C0G1H102J	TDK	1nF/50V , 0603, NPO	2
	VJ0603A102KXXAT	Vishay		
C4	C1608C0G1H332J	TDK	3.3nF /50V, 0603, NPO	1
	VJ0603A332KXXAT	Vishay		
C5	C1608C0G1H470J	TDK	47pF/50V , 0603, NPO	1
	VJ0603A470KXXAT	Vishay		
C6	C1608C0G1H221J.	TDK	220pF/50V , 0603, NPO	1
	VJ0603A221KXXAT	Vishay		
C8	C3225X7R0J107M	TDK	100uF/6.3V , 1210, X7R	1
	GRM32ER60J17ME20L	Murata[3]		
C9	C1608COG1H101J	TDK	100pF/50V, 0603	1
	VJ0603Y101KXAAT	Vishay		
L1	C1608COG1H101J	TDK	3A Inductor	1
R1	CRCW06031602FKEA	Vishay	16K , 1/16W , 0603 , 1%	1
R2, R3	CRCW06031002FKEA	Vishay	10K , 1/16W , 0603 , 1%	2
R4	CRCW060320K0FKEA	Vishay	20K , 1/16W , 0603 , 1%	1
U1	**MIC22200YML**	**Micrel**[4]	**Integrated 2A Synchronous Buck Regulator**	**1**

Notes:

1. TDK: www.tdk.com
2. Murata: www.murata.com
3. Vishay: www.vishay.com
4. **Micrel, Inc.: www.micrel.com**

Package Information



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