

MC10H604, MC100H604

Registered Hex TTL to ECL Translator

Description

The MC10H/100H604 is a 6-bit, registered, dual supply TTL to ECL translator. The device features differential ECL outputs as well as a choice between either a differential ECL clock input or a TTL clock input. The asynchronous master reset control is an ECL level input.

With its differential ECL outputs and TTL inputs the H604 device is ideally suited for the transmit function of a HPPI bus type board-to-board interface application. The on-chip registers simplify the task of synchronizing the data between the two boards.

The device is available in either ECL standard: the 10H device is compatible with MECL 10KH logic levels while the 100H device is compatible with 100K logic levels.

Features

- Differential 50 Ω ECL Outputs
- Choice Between Differential ECL or TTL Clock Input
- Dual Power Supply
- Multiple Power and Ground Pins to Minimize Noise
- Specified Within-Device Skew
- Pb-Free Packages are Available*



ON Semiconductor®

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**PLCC-28
FN SUFFIX
CASE 776**

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC10H604, MC100H604

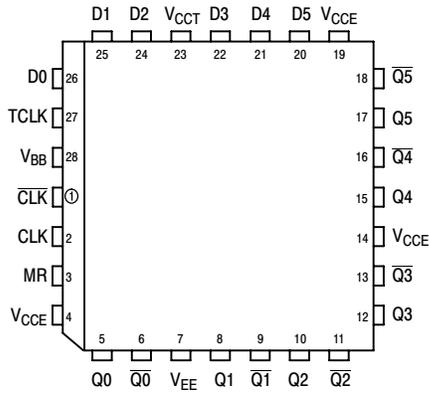


Figure 1. PLCC-28 Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
D0-D5	TTL Data Inputs
CLK, $\overline{\text{CLK}}$	Differential ECL Clock Input
TCLK	TTL Clock Input
MR	ECL Master Reset Input
Q0-Q5	True ECL Outputs
$\overline{\text{Q0-Q5}}$	Inverted ECL Outputs
V _{CCE}	ECL V _{CC} (0V)
V _{CCT}	TTL V _{CC} (+5.0 V)
V _{EE}	ECL V _{EE} (-5.2 V)

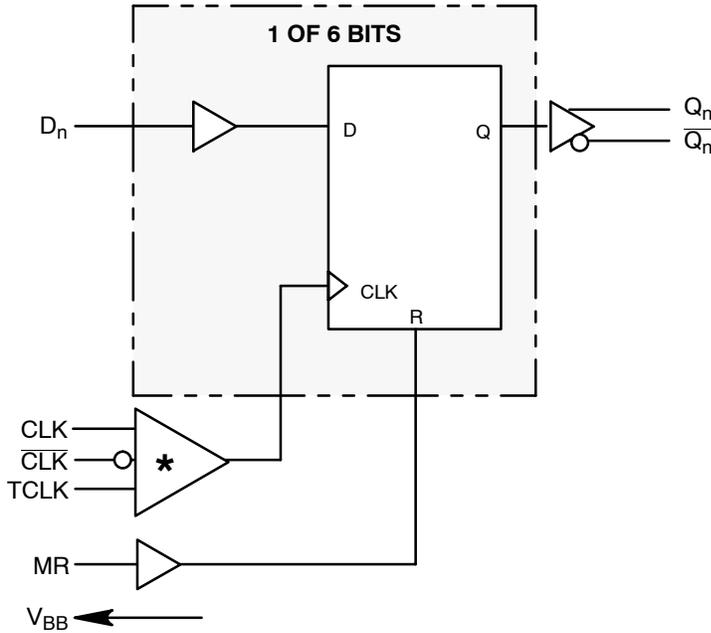


Table 2. TRUTH TABLE

D _n	MR	TCLK/CLK	Q _{n+1}
L	L	Z	L
H	L	Z	H
X	H	X	L

Z = LOW to HIGH Transition

- * 1. When using MECL inputs, TCLK must be tied to ground (0 V).
- 2. When using only one MECL input, the unused MECL input must be tied to V_{BB}, and TCLK must be tied to ground (0 V).
- 3. When using TCLK, both MECL inputs must be tied to V_{EE} (-5.2 V).

Figure 2. Logic Symbol

Table 3. DC CHARACTERISTICS: V_{EE} = V_{EE}(Min) to V_{EE}(Max); V_{CCE} = GND; V_{CCT} = 5.0 V +10%

Symbol	Parameter	0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
I _{EE}	ECL Power Supply Current	10H	130	130	130	130	130	mA
		100H	130		140		150	
I _{CCH} I _{CCL}	TTL Power Supply Current		35	35	35	35	35	mA
			45	45	45	45	45	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

MC10H604, MC100H604

Table 4. 10H ECL DC CHARACTERISTICS: $V_{CC} = +5.0\text{ V} \pm 10\%$; $V_{EE} = -5.20\text{ V} \pm 5\%$

Symbol	Parameter	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current		0.5	255	0.5	175	0.5	175	μA μA
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		-1170 -1950	-840 -1480	-1130 -1950	-810 -1480	-1060 -1950	-720 -1480	mV
V_{BB}	Output Bias Voltage		-1400	-1290	-1370	-1270	-1330	-1210	mV
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	50 Ω to -2.0 V	-1020 -1950	-840 -1630	-980 -1950	-810 -1630	-910 -1950	-720 -1595	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. 100H ECL DC CHARACTERISTICS: $V_{CC} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -4.2\text{ V}$ to -5.5 V

Symbol	Parameter	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current		0.5	255	0.5	175	0.5	175	μA μA
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	-1165 -1810	-880 -1475	mV
V_{BB}	Output Bias Voltage		-1400	-1280	-1400	-1280	-1400	-1280	mV
V_{OH} V_{OL}	Output HIGH Voltage Output LOW Voltage	50 Ω to -2.0 V	-1025 -1810	-880 -1620	-1025 -1810	-880 -1620	-1025 -1810	-880 -1620	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. TTL DC CHARACTERISTICS: $V_{CC} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H); $V_{EE} = -4.2\text{ V}$ to -5.5 V (100H)

Symbol	Parameter	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage		2.0	0.8	2.0	0.8	2.0	0.8	V V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7\text{ V}$ $V_{IN} = 7.0\text{ V}$		20 100		20 100		20 100	μA
I_{IL}	Input LOW Current	$V_{IN} = 0.5\text{ V}$		-0.6		-0.6		-0.6	mA
V_{IK}	Input Clamp Voltage	$I_{IN} = -18\text{ mA}$		-1.2		-1.2		-1.2	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

MC10H604, MC100H604

Table 7. AC CHARACTERISTICS: $V_{CCT} = 5.0\text{ V} \pm 10\%$; $V_{EE} = -5.2\text{ V} \pm 5\%$ (10H); $V_{EE} = -4.2\text{ V}$ to -5.5 V (100H)

Symbol	Parameter	Condition	0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation Delay to Output	CLK to Q TCLK to Q MR to Q	1.5 2.0 1.5		3.5 4.0 4.0	1.5 2.0 1.5		3.5 4.0 4.0	1.5 2.0 1.5		3.5 4.0 4.0	ns
t_s	Setup Time	50 Ω to -2.0 V	1.5	0.5		1.5	0.5		1.5	0.5		ns
t_H	Hold Time	50 Ω to -2.0 V	1.5	0.5		1.5	0.5		1.5	0.5		ns
t_{PW}	Minimum Pulse Width	50 Ω to -2.0 V CLK, MR		1.0			1.0			1.0		ns
V_{PP}	Minimum Input Swing						150					mV
t_r t_f	Rise/Fall Times	20% – 80%	0.3	1.0	2.0	0.3	1.0	2.0	0.3	1.0	2.0	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

ORDERING INFORMATION

Device	Package	Shipping [†]
MC10H604FN	PLCC-28	37 Units / Rail
MC10H604FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC10H604FNR2	PLCC-28	500 / Tape & Reel
MC10H604FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel
MC100H604FN	PLCC-28	37 Units / Rail
MC100H604FNG	PLCC-28 (Pb-Free)	37 Units / Rail
MC100H604FNR2	PLCC-28	500 / Tape & Reel
MC100H604FNR2G	PLCC-28 (Pb-Free)	500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

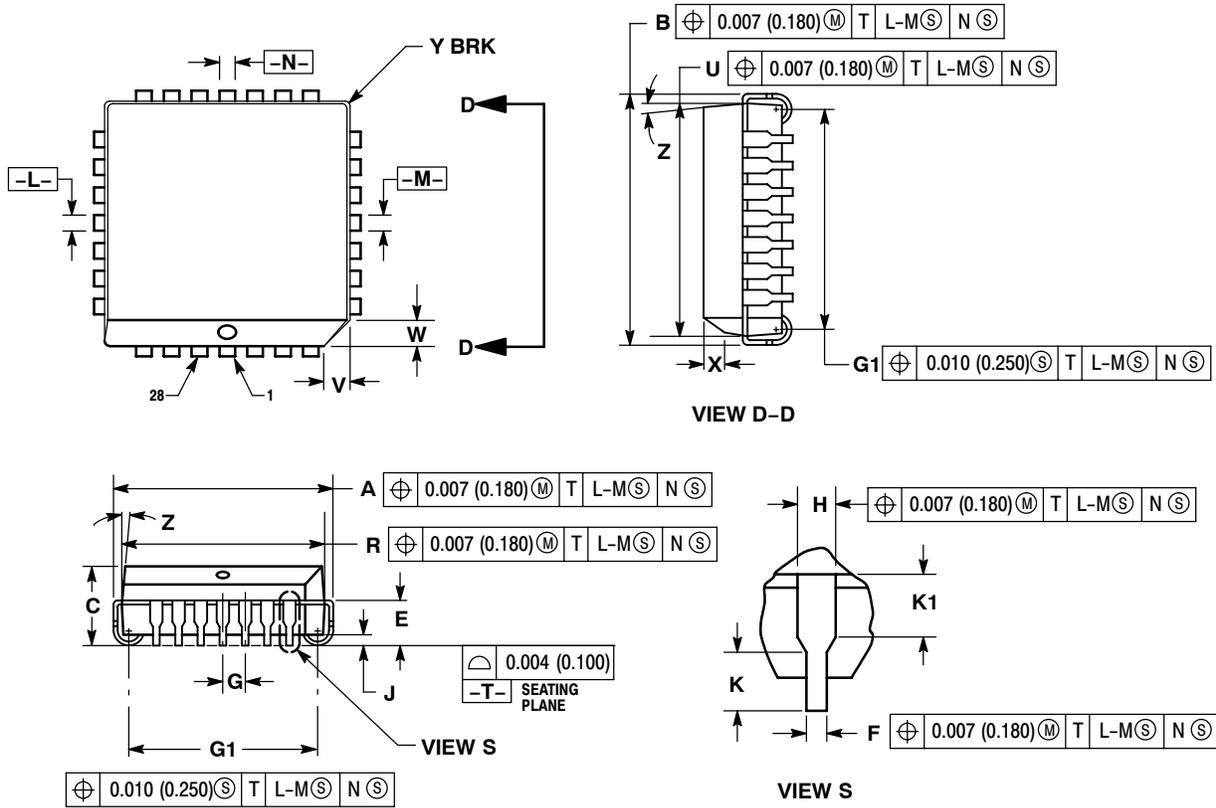
Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

MC10H604, MC100H604

PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE BOTTOM MAY BE SMALLER THAN THE PACKAGE TOP BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2° 10°		2° 10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

MC10H604, MC100H604

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