M41T00S

Serial access real-time clock

Features

- 2.0 to 5.5 V clock operating voltage
- Counters for seconds, minutes, hours, day, date, month, year, and century
- Software clock calibration
- Automatic switchover and deselect circuitry (fixed reference)
  - V_{CC} = 2.7 to 5.5 V
    2.5V ≤ V_{PFD} ≤ 2.7 V
- Serial interface supports I^2C bus (400 kHz protocol)
- Low operating current of 300 µA
- Oscillator stop detection
- Battery or SuperCap™ backup
- Operating temperature of –40 to 85°C
- Ultra-low battery supply current of 1 µA

SO8 (M)
8-pin SOIC

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1 Description

The M41T00S Serial Access TIMEKEEPER® SRAM is a low power serial RTC with a built-in 32.768 kHz oscillator (external crystal controlled). Eight bytes of the SRAM (see *Table 2 on page 13*) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. Addresses and data are transferred serially via a two line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte.

The M41T00S has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the clock operations can be supplied by a small lithium button supply when a power failure occurs. The eight clock address locations contain the century, year, month, date, day, hour, minute, and second in 24-hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically.

The M41T00S is supplied in an 8-pin SOIC.

Figure 1. Logic diagram

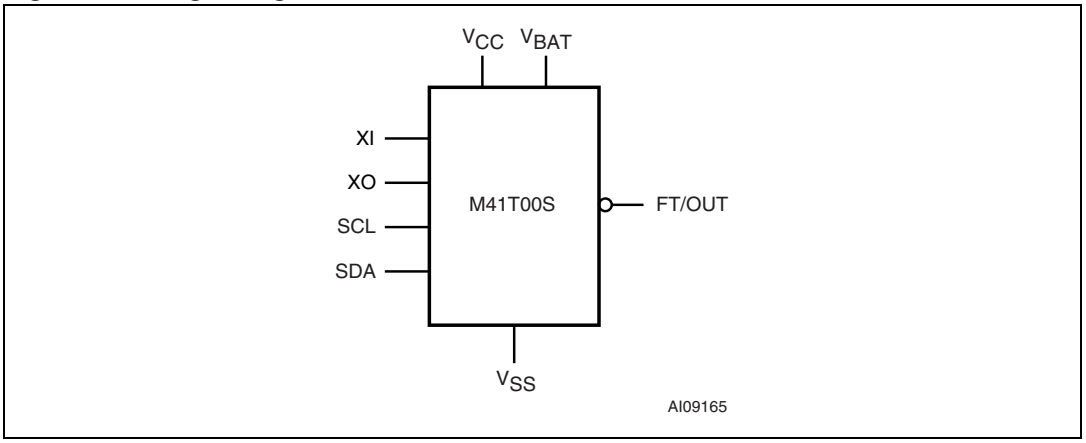
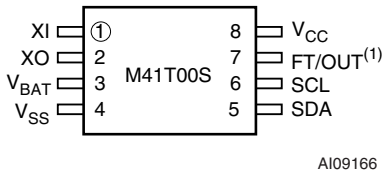


Table 1. Signal names

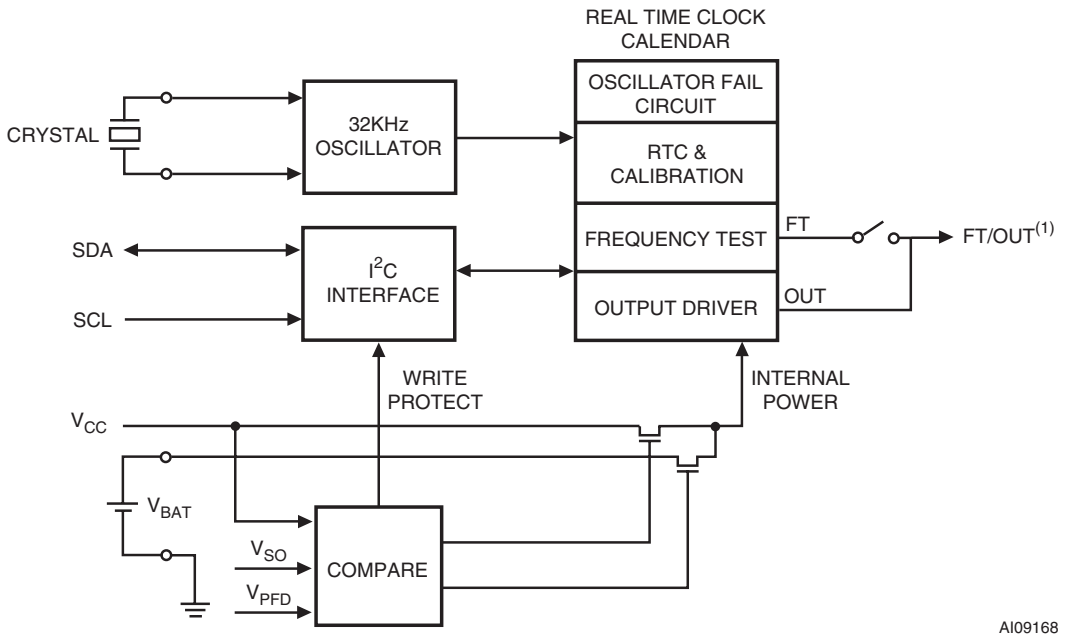
XI	Oscillator input
XO	Oscillator output
FT/OUT	Frequency test / output driver (open drain)
SDA	Serial data input/output
SCL	Serial clock input
V_{BAT}	Battery supply voltage
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 2. 8-pin SOIC (M) connections



1. Open drain output

Figure 3. Block diagram



1. Open drain output

2 Operation

The M41T00S clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 8 bytes contained in the device can then be accessed sequentially in the following order:

1. Seconds register
2. Minutes register
3. Century/hours register
4. Day register
5. Date register
6. Month register
7. Year register
8. Calibration register

The M41T00S clock continually monitors V_{CC} for an out-of-tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system. Once V_{CC} falls below the switchover voltage (V_{SO}), the device automatically switches over to the battery and powers down into an ultra-low current mode of operation to preserve battery life. If V_{BAT} is less than V_{PFD}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{BAT}. If V_{BAT} is greater than V_{PFD}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{PFD}. Upon power-up, the device switches from battery to V_{CC} at V_{SO}. When V_{CC} rises above V_{PFD}, it will recognize the inputs.

For more information on battery storage life refer to Application Note AN1012.

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bidirectional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. this acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 4. Serial bus data transfer sequence

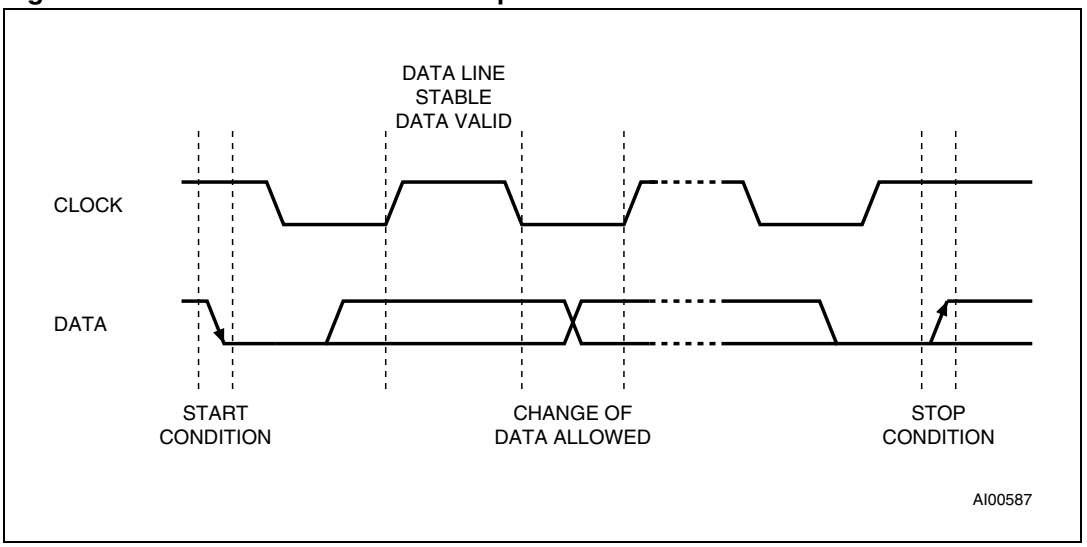
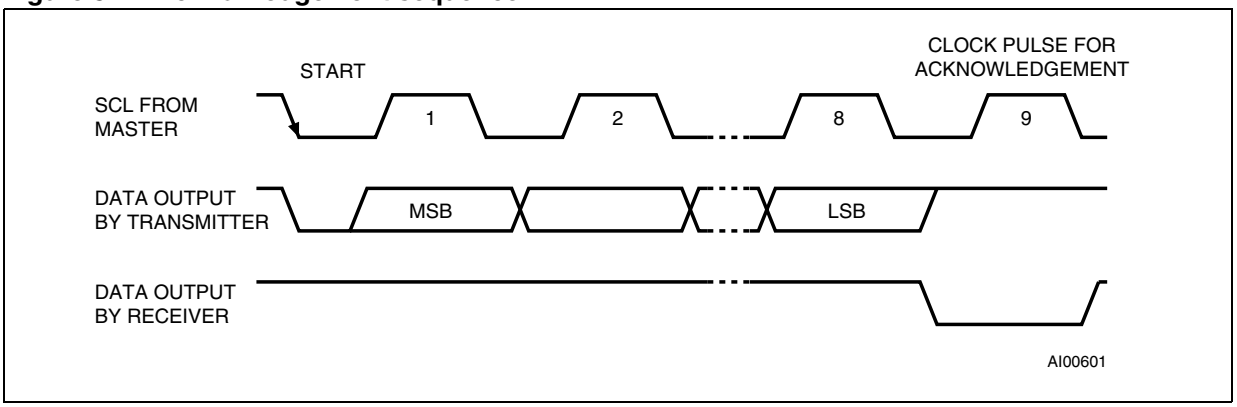


Figure 5. Acknowledgement sequence



2.2 READ mode

In this mode the master reads the M41T00S slave after setting the slave address (see *Figure 7 on page 10*). Following the WRITE mode control bit (R/$\overline{W}$=0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/$\overline{W}$=1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41T00S slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to “An+2.”

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 06h). The update will resume due to a stop condition or when the pointer increments to any non-clock address (07h).

Note: This is true both in READ mode and WRITE mode.

An alternate READ mode may also be implemented whereby the master reads the M41T00S slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 8 on page 10*).

Figure 6. Slave address location

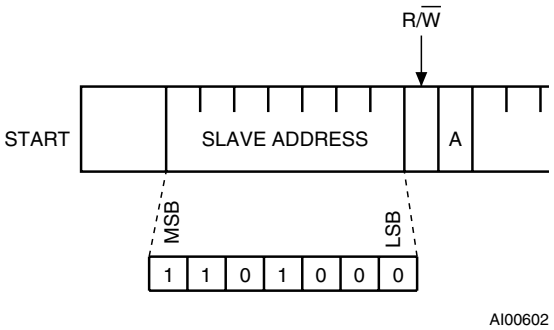


Figure 7. READ mode sequence

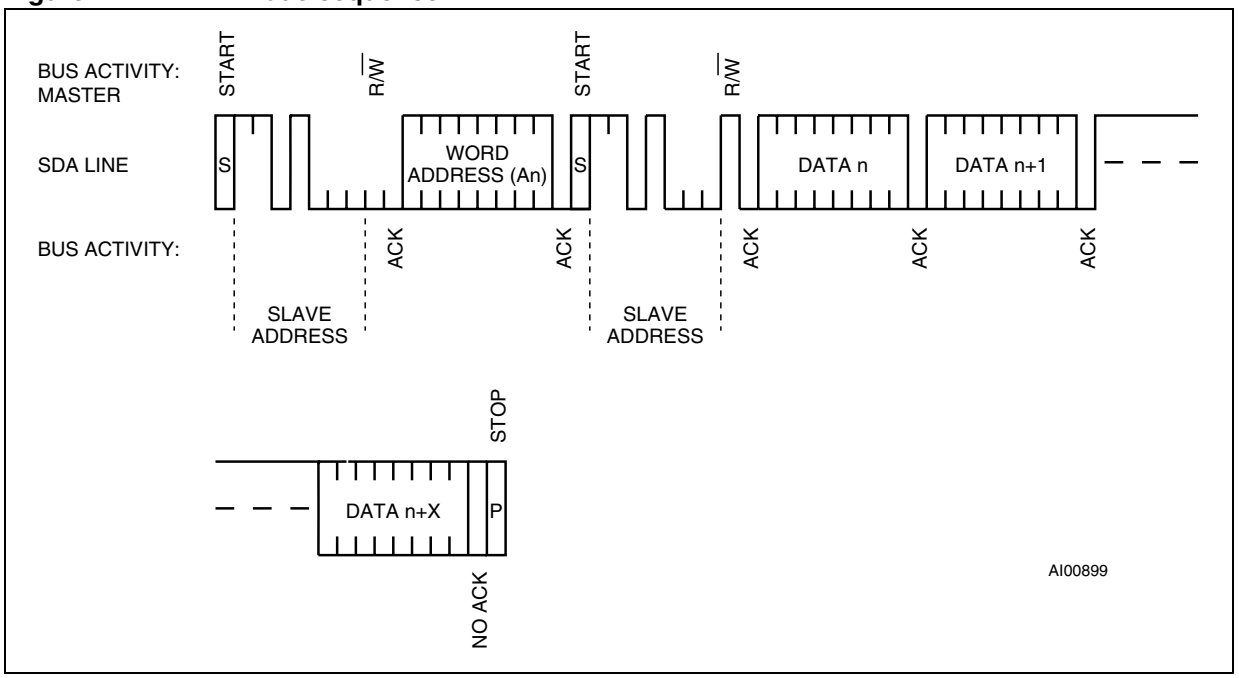
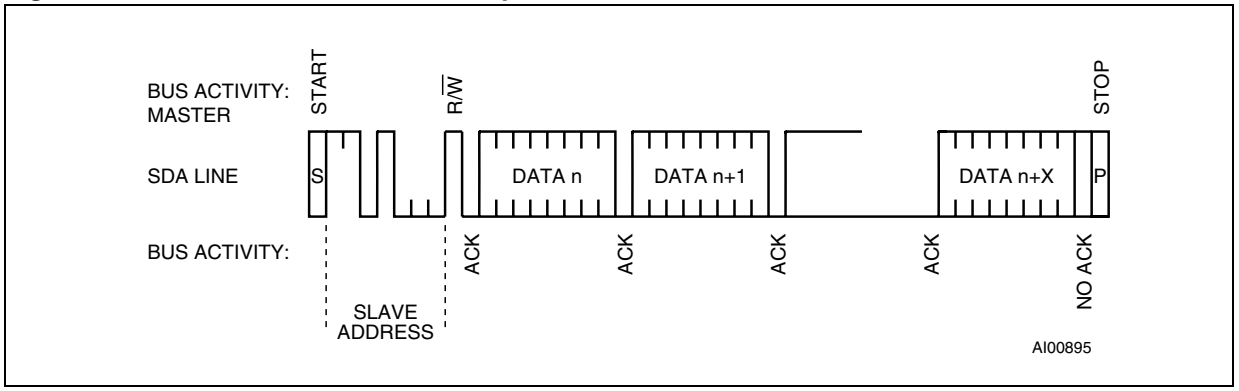


Figure 8. Alternative READ mode sequence



2.3 WRITE mode

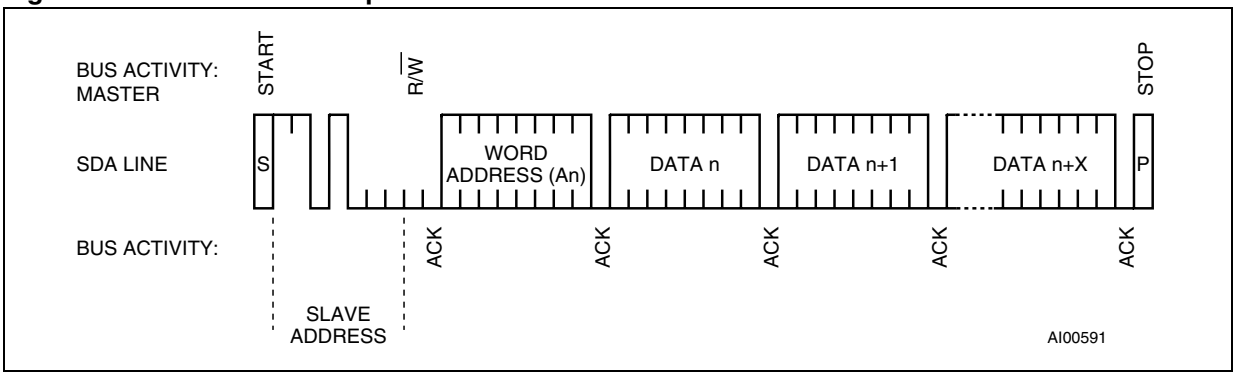
In this mode the master transmitter transmits to the M41T00S slave receiver. Bus protocol is shown in *Figure 9*. Following the START condition and slave address, a logic '0' (R/$\overline{W}$=0) is placed on the bus and indicates to the addressed device that word address “An” will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T00S slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address see *Figure 6 on page 9* and again after it has received the word address and each data byte.

2.4 Data retention mode

With valid V_{CC} applied, the M41T00S can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the power input will be switched from the V_{CC} pin to the battery when V_{CC} falls below the battery backup switchover voltage (V_{SO}). At this time the clock registers will be maintained by the attached battery supply. On power-up, when V_{CC} returns to a nominal value, write protection continues for t_{REC}.

For a further, more detailed review of lifetime calculations, please see Application Note AN1012.

Figure 9. WRITE mode sequence



3 Clock operation

The 8-byte register map (see *Table 2*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Seconds, minutes, and hours are contained within the first three registers.

Bits D6 and D7 of clock register 02h (century/hours register) contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle. Bits D0 through D2 of Register 03h contain the Day (day of week). Registers 04h, 05h, and 06h contain the date (day of month), month and years. The eighth clock register is the calibration register (this is described in the clock calibration section). Bit D7 of register 00h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The seven clock registers may be read one byte at a time, or in a sequential block. The calibration register (address location 07h) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the seven clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

3.1 Clock registers

The M41T00S offers 8 internal registers which contain clock and calibration data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 06h). The update will resume either due to a stop condition or when the pointer increments to any non-clock address (07h).

Clock registers store data in BCD. The calibration register stores data in binary format.

Table 2. TIMEKEEPER® register map

Addr									Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
00h	ST	10 seconds			Seconds				Seconds	00-59
01h	OF	10 minutes			Minutes				Minutes	00-59
02h	CEB	CB	10 hours		Hours (24-hour format)				Century/hours	0-1/00-23
03h	0	0	0	0	0	Day of week			Day	01-7
04h	0	0	10 date		Date: day of month				Date	01-31
05h	0	0	0	10M	Month				Month	01-12
06h	10 years				Year				Year	00-99
07h	OUT	FT	S	Calibration					Calibration	

Keys:

0 = must be set to '0'

CB = century bit

CEB = century enable bit

FT = frequency test bit

OF = oscillator fail bit

OUT = output level

S = sign bit

ST = stop bit

3.2 Calibrating the clock

The M41T00S is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not exceed ±35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month (see *Figure 10 on page 15*). When the calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25°C.

The oscillation rate of crystals changes with temperature. The M41T00S design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 11 on page 15*. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the calibration register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the calibration register 07h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register (see *Figure 11 on page 15*). Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41T00S may require.

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934, “TIMEKEEPER® calibration.” This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the FT/OUT pin. The pin will toggle at 512Hz, when the Stop bit (ST, D7 of 00h) is '0,' and the Frequency Test bit (FT, D6 of 07h) is '1.'

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction. Note that setting or changing the Calibration Byte does not affect the frequency test output frequency.

The FT/OUT pin is an open drain output which requires a pull-up resistor to V_{CC} for proper operation. A 500-10k resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

Figure 10. Crystal accuracy across temperature

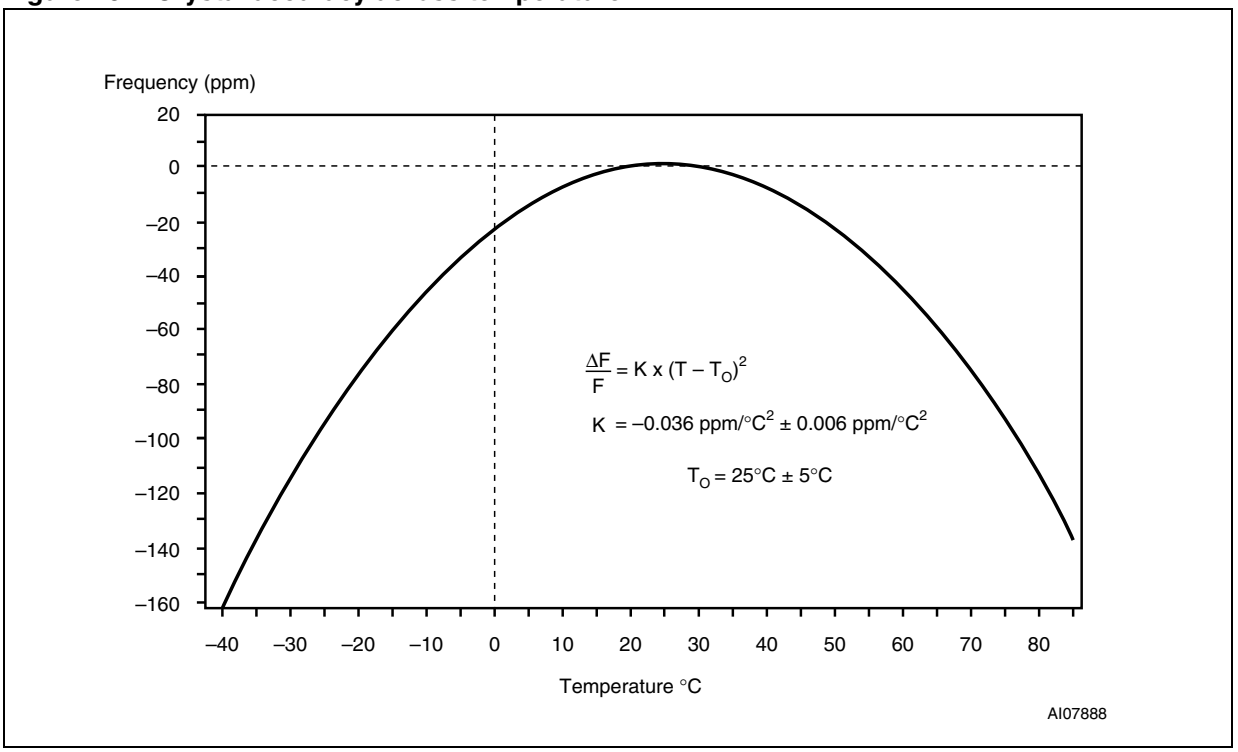
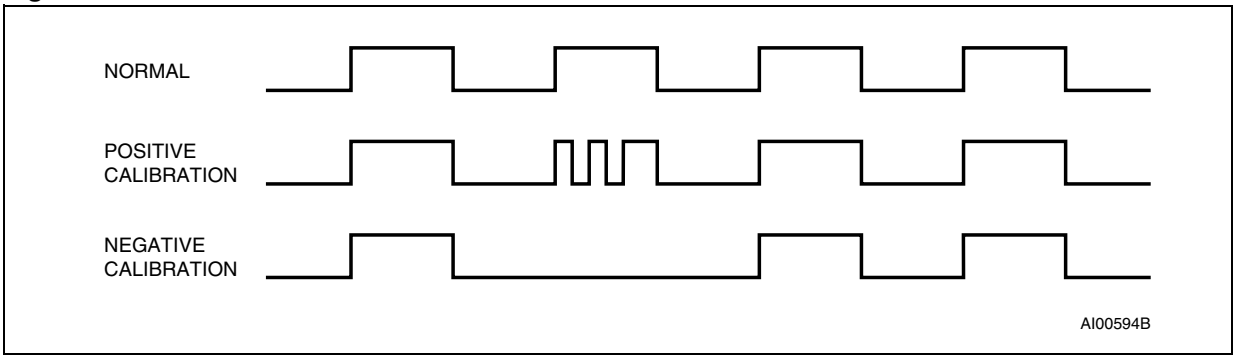


Figure 11. Clock calibration



3.2.1 Century bit

Bits D7 and D6 of Clock Register 02h contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

3.2.2 Oscillator fail detection

If the Oscillator Fail bit (OF) is internally set to '1,' this indicates that the oscillator has either stopped, or was stopped for some period of time and can be used to judge the validity of the clock and date data.

In the event the OF bit is found to be set to '1' at any time other than the initial power-up, the STOP bit (ST) should be written to a '1,' then immediately reset to '0.' This will restart the oscillator.

The following conditions can cause the OF bit to be set:

- The first time power is applied (defaults to a '1' on power-up).
- The voltage present on V_{CC} is insufficient to support oscillation.
- The ST bit is set to '1.'
- External interference of the crystal.

The OF bit will remain set to '1' until written to logic '0.' The oscillator must start and have run for at least 4 seconds before attempting to reset the OF Bit to '0.'

3.2.3 Output driver pin

When the FT bit is not set, the FT/OUT pin becomes an output driver that reflects the contents of D7 of the calibration register. In other words, when D7 (OUT Bit) and D6 (FT bit) of address location 07h are a '0,' then the FT/OUT pin will be driven low.

Note: The FT/OUT pin is an open drain which requires an external pull-up resistor.

3.2.4 Preferred initial power-on default

Upon initial application of power to the device, the ST and FT bits are set to a '0' state, and the OF and OUT bits will be set to a '1.' All other register bits will initially power-on in a random state (see *Table 3*).

Table 3. Preferred default values

Condition	ST	Out	FT	OF
Initial power-up(1)	0	1	0	1
Subsequent power-up (with battery backup)(2)	UC	UC	0	UC

1. State of other control bits undefined.
2. UC = Unchanged

4 Maximum ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Sym	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off, oscillator off)	–55 to 125	°C
V_{CC}	Supply voltage	–0.3 to 7	V
T_{SLD}(1)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltages	–0.3 to V_{CC}+0.3	V
I_O	Output current	20	mA
P_D	Power dissipation	1	W

1. Reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

Caution: Negative undershoots below –0.3 volts are not allowed on any pin while in the battery backup mode

5 DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 5. Operating and AC measurement conditions

Parameter	M41T00S
Supply voltage (V_{CC})	2.7 to 5.5 V
Ambient operating temperature (T_A)	–40 to 85°C
Load capacitance (C_L)	100 pF
Input rise and fall times	≤ 50 ns
Input pulse voltages	$0.2V_{CC}$ to $0.8\ V_{CC}$
Input and output timing ref. voltages	$0.3V_{CC}$ to $0.7\ V_{CC}$

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 12. AC measurement I/O waveform

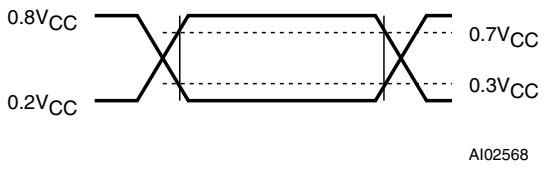


Table 6. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance		7	pF
C_{OUT}[3]	Output capacitance		10	pF
t_{LP}	Low-pass filter input time constant (SDA and SCL)		50	ns

1. Effective capacitance measured with power supply at 5V; sampled only, not 100% tested.
2. At 25°C, f = 1 MHz
3. Outputs deselected.

Table 7. DC characteristics

Sym	Parameter	Test condition(1)	Min	Typ	Max	Unit
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$			±1	µA
I_{LO}	Output leakage current	$0V \le V_{OUT} \le V_{CC}$			±1	µA
I_{CC1}	Supply current	Switch freq = 400 kHz			300	µA
I_{CC2}	Supply current (standby)	SCL = 0Hz All Inputs $\ge V_{CC} - 0.2$ V $\le V_{SS} + 0.2$ V			70	µA
V_{IL}	Input low voltage		–0.3		$0.3V_{CC}$	V
V_{IH}	Input high voltage		$0.7V_{CC}$		$V_{CC} + 0.3$	V
V_{OL}	Output low voltage	I_{OL} = 3.0mA			0.4	V
	Output low voltage (open drain)(2)	I_{OL} = 10mA			0.4	V
	Pull-up supply voltage (open drain)	FT/OUT			5.5	V
V_{BAT}(3)	Backup supply voltage		2.0		3.5(4)	V
I_{BAT}	Battery supply current	T_A = 25°C, V_{CC} = 0 V Oscillator ON, V_{BAT} = 3 V		0.6	1	µA

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 5.5 V (except where noted).
2. For FT/OUT pin (open drain).
3. STMicroelectronics recommends the RAYOVAC BR1225 or BR1632 (or equivalent) as the battery supply.
4. For rechargeable backup, V_{BAT} (max) may be considered to be V_{CC}.

Table 8. Crystal electrical characteristics

Sym	Parameter(1)(2)	Min	Typ	Max	Units
f_O	Resonant frequency		32.768		kHz
R_S	Series resistance			60(3)	kΩ
C_L	Load capacitance		12.5		pF

1. Externally supplied if using the SO8 package. STMicroelectronics recommends the KDS DT-38: 1TA/1TC252E127, Tuning Fork Type (thru-hole) or the DMX-26S: 1TJS125FH2A212, (SMD) quartz crystal for industrial temperature operations. KDS can be contacted at kouhou@kdsj.co.jp or http://www.kdsj.co.jp for further information on this crystal type.
2. Load capacitors are integrated within the M41T00S. Circuit board layout considerations for the 32.768 kHz crystal of minimum trace lengths and isolation from RF generating signals should be taken into account.
3. For applications requiring backup supply operation below 2.5 V, R_S (max) should be considered 40 kΩ.

Figure 13. Power down/up mode AC waveforms

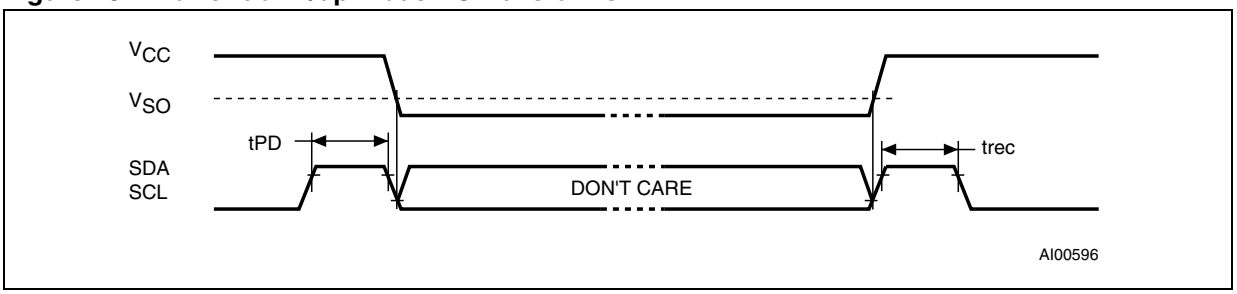


Table 9. Power down/up AC characteristics

Symbol	Parameter[1][2]	Min	Typ	Max	Unit
t_{PD}	SCL and SDA at V_{IH} before power down	0			nS
t_{rec}	SCL and SDA at V_{IH} after power up	10			µS

1. V_{CC} fall time should not exceed 5 mV/µs.
2. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 5.5 V (except where noted).

Table 10. Power down/up trip points DC characteristics

Sym	Parameter[1][2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect		2.5	2.6	2.7	V
	Hysteresis			25		mV
V_{SO}	Battery backup switchover voltage ($V_{CC} < V_{BAT}$; $V_{CC} < V_{PFD}$)	$V_{BAT} < V_{PFD}$		V_{BAT}		V
		$V_{BAT} > V_{PFD}$		V_{PFD}		V
	Hysteresis			40		mV

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 5.5 V (except where noted).

Figure 14. Bus timing requirements sequence

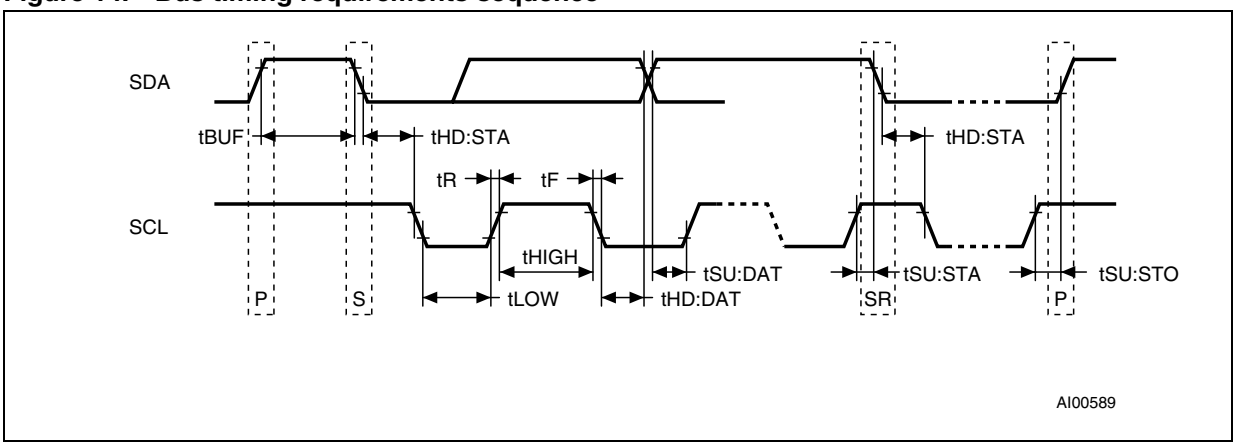


Table 11. AC characteristics

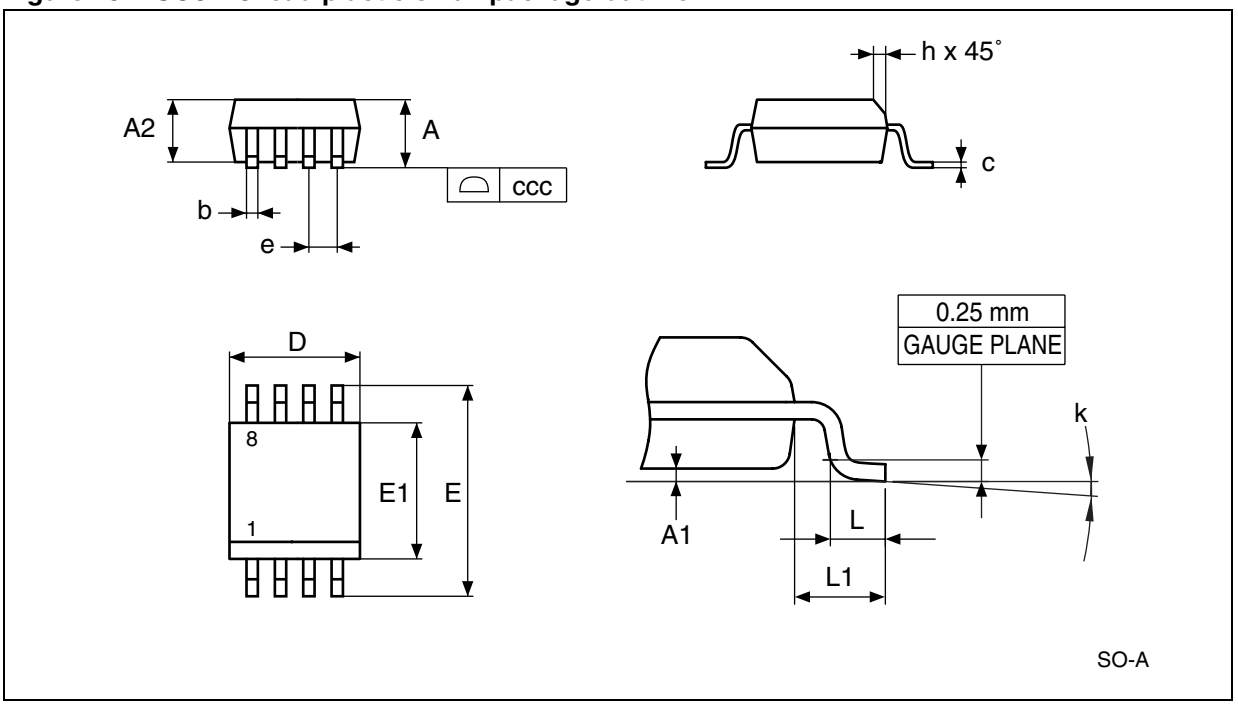
Sym	Parameter[1]	Min	Typ	Max	Units
f_{SCL}	SCL clock frequency	0		400	kHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_R	SDA and SCL rise time			300	ns
t_F	SDA and SCL fall time			300	ns
$t_{HD:STA}$	START condition hold time (after this period the first clock pulse is generated)	600			ns
$t_{SU:STA}$	START condition setup time (only relevant for a repeated start condition)	600			ns
$t_{SU:DAT}$[2]	Data setup time	100			ns
$t_{HD:DAT}$	Data hold time	0			µs
$t_{SU:STO}$	STOP condition setup time	600			ns
t_{BUF}	Time the bus must be free before a new transmission can start	1.3			µs

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 5.5 V (except where noted).
2. Transmitter must internally provide a hold time to bridge the undefined region (300 ns max) of the falling edge of SCL.

6 Package mechanical information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 15. SO8 – 8-lead plastic small package outline



Note: Drawing is not to scale.

Table 12. SO8 – 8-lead plastic small outline (150 mils body width), package mechanical data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.069
A1		0.10	0.25		0.004	0.010
A2		1.25			0.049	
B		0.28	0.48		0.011	0.019
C		0.17	0.23		0.007	0.009
D	4.90	4.80	5.00		0.189	0.197
E	6.00	5.80	6.20		0.228	0.244
E1	3.90	3.80	4.00		0.150	0.157
e	1.27			0.050		
h		0.25	0.50		0.010	0.020
L		0.40	1.27		0.016	0.050
L1	1.04			0.041		
k		0°	8°		0°	8°
N	8			8		
ccc			0.10			0.004

7 Part numbering

Table 13. Ordering information scheme

Example: M41T 00S M 6 E

Device type

M41T

Supply voltage and write protect voltage

00S = V_{CC} = 2.7 to 5.5 V

Package

M = SO8

Temperature range

6 = –40°C to 85°C

Shipping method

E = ECOPACK® package, tubes

F = ECOPACK® package, tape & reel

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

8 Revision history

Table 14. Document revision history

Date	Revision	Changes
10-Feb- 2004	0.1	First draft
20-Feb-2004	0.2	Update characteristics (*Table 9*, *10*, *5*, *7*, *13*)
14-Apr-2004	1.0	Product promoted; reformatted; update characteristics, including Lead-free package information (*Figure 4*, *10*; *Table 4*, *11*, *13*)
05-May-2004	1.1	Update DC characteristics (*Table 7*)
16-Jun-2004	1.2	Added package shipping (*Table 13*)
13-Sep-2004	2.0	Update maximum ratings (*Table 4*)
26-Nov-2004	3.0	Promote document; update characteristics; remove references to SOX18 package (cover page, *Figure 4*; *Table 14*)
14-May-2008	4	Reformatted document; updated *Section 6*, *Figure 1*, *15*, *Table 1*, *4*, *12*, *13*.

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