

1. Overview

The M32C/83 Group (M32C/83, M32C/83T) microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 Series CPU core. The M32C/83 Group (M32C/83, M32C/83T) is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It includes a multiplier and DMAC adequate for office automation, communication devices and industrial equipments, and other high-speed processing applications.

1.1 Applications

Automobiles, audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Overview

Tables 1.1 and 1.2 list performance overview of the M32C/83 Group (M32C/83, M32C/83T).

Table 1.1 M32C/83 Group (M32C/83, M32C/83T) Performance (144-Pin Package)

Characteristic		Performance	
		M32C/83	M32C/83T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, Vcc=4.2 to 5.5 V) ⁽³⁾ 50 ns (f(BCLK)=20 MHz, Vcc=3.0 to 5.5 V)	31.3 ns (f(BCLK)=32 MHz, Vcc=4.2 to 5.5 V) ⁽³⁾
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	123 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function: 16 bits x 12 channels Waveform generating function: 16 bits x 28 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus ⁽¹⁾ , 8-bit or 16-bit Clock synchronous serial I/O)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C bus ⁽²⁾	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 2 circuit, 34 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	DRAM	CAS before RAS refresh, Self-refresh, EDO, EP	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	42 internal and 8 external sources, 5 software sources, Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
Electrical Characteristics	Supply Voltage	4.2 to 5.5 V (f(BCLK)=32 MHz) 3.0 to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 to 3.6 V (f(BCLK)=20 MHz, not through VDC)	4.2 to 5.5 V (f(BCLK)=32 MHz)
	Power Consumption	41 mA (Vcc=5 V, f(BCLK)=32 MHz) 38 mA (Vcc=5 V, f(BCLK)=30 MHz) 26 mA (Vcc=3.3 V, f(BCLK)=20 MHz) 470 μ A (Vcc=5 V, f(XCIN)=32 kHz, in wait mode) 340 μ A (Vcc=3.3 V, f(XCIN)=32 kHz, through VDC, in wait mode) 5.0 μ A (Vcc=3.3 V, f(XCIN)=32 kHz, not through VDC, in wait mode) 0.4 μ A (Vcc=5 V, stop mode) 0.4 μ A (Vcc=3.3 V, stop mode)	41 mA (Vcc=5 V, f(BCLK)=32 MHz) 38 mA (Vcc=5 V, f(BCLK)=30 MHz) 470 μ A (Vcc=5 V, f(XCIN)=32 kHz, in wait mode) 0.4 μ A (Vcc=5 V, stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 $\pm$ 0.3 V or 5.0 $\pm$ 0.5 V	5.0 $\pm$ 0.5 V
	Program and Erase Endurance	100 times	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C (optional)	-40 to 85°C (T version)
Package		144-pin plastic molded LQFP	

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact our sales office if 30-MHz or higher frequency is required.

All options are on a request basis.

Table 1.2 M32C/83 Group (M32C/83, M32C/83T) Performance (100-Pin Package)

Characteristic		Performance	
		M32C/83	M32C/83T
CPU	Basic Instructions	108 instructions	
	Minimum Instruction Execution Time	31.3 ns (f(BCLK) = 32 MHz, V _{CC} = 4.2 to 5.5 V) 50 ns (f(BCLK) = 20 MHz, V _{CC} = 3.0 to 5.5 V)	31.3 ns (f(BCLK) = 32 MHz, V _{CC} = 4.2 to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode and Microprocessor mode	Single-chip mode
	Address Space	16 Mbytes	
	Memory Capacity	See Table 1.3	
Peripheral Function	I/O Port	87 I/O pins and 1 input pin	
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit	
	Intelligent I/O	Time measurement function: 16 bits x 5 channels Waveform generating function: 16 bits x 10 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus ⁽¹⁾)	
	Serial I/O	5 Channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C bus ⁽²⁾	
	CAN Module	1 channel Supporting CAN 2.0B specification	
	A/D Converter	10-bit A/D converter: 2 circuits, 26 channels	
	D/A Converter	8 bits x 2 channels	
	DMAC	4 channels	
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, Calculation transfer and Chain transfer functions	
	CRC Calculation Circuit	CRC-CCITT	
	X/Y Converter	16 bits x 16 bits	
	Watchdog Timer	15 bits x 1 channel (with prescaler)	
	Interrupt	42 internal and 8 external sources, 5 software sources Interrupt priority level: 7	
	Clock Generation Circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally	
	Oscillation Stop Detect Function	Main clock oscillation stop detect function	
Electrical Characteristics	Supply Voltage	4.2 to 5.5 V (f(BCLK)=32 MHz) 3.0 to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 to 3.6 V (f(BCLK)=20 MHz, not through VDC)	4.2 to 5.5 V (f(BCLK)=32 MHz)
	Power Consumption	41 mA (V _{CC} =5 V, f(BCLK)=32 MHz) 38 mA (V _{CC} =5 V, f(BCLK)=30 MHz) 26 mA (V _{CC} =3.3 V, f(BCLK)=20 MHz) 470 μ A (V _{CC} =5 V, f(XCIN)=32 kHz, in wait mode) 340 μ A (V _{CC} =3.3 V, f(XCIN)=32 kHz, through VDC, in wait mode) 5.0 μ A (V _{CC} =3.3 V, f(XCIN)=32 kHz, not through VDC, in wait mode) 0.4 μ A (V _{CC} =5 V, stop mode) 0.4 μ A (V _{CC} =3.3 V, stop mode)	41 mA (V _{CC} =5 V, f(BCLK)=32 MHz) 38 mA (V _{CC} =5 V, f(BCLK)=30 MHz) 470 μ A (V _{CC} =5 V, f(XCIN)=32 kHz, in wait mode) 0.4 μ A (V _{CC} =5 V, stop mode)
Flash Memory	Program/Erase Supply Voltage	3.3 $\pm$ 0.3 V or 5.0 $\pm$ 0.5 V	5.0 $\pm$ 0.5 V
	Program and Erase Endurance	100 times	
Operating Ambient Temperature		-20 to 85°C, -40 to 85°C (optional)	-40 to 85°C (T version)
Package		100-pin plastic molded LQFP/QFP	

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
3. Contact our sales office if 30-MHz or higher frequency is required.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/83 Group (M32C/83, M32C/83T) microcomputer.

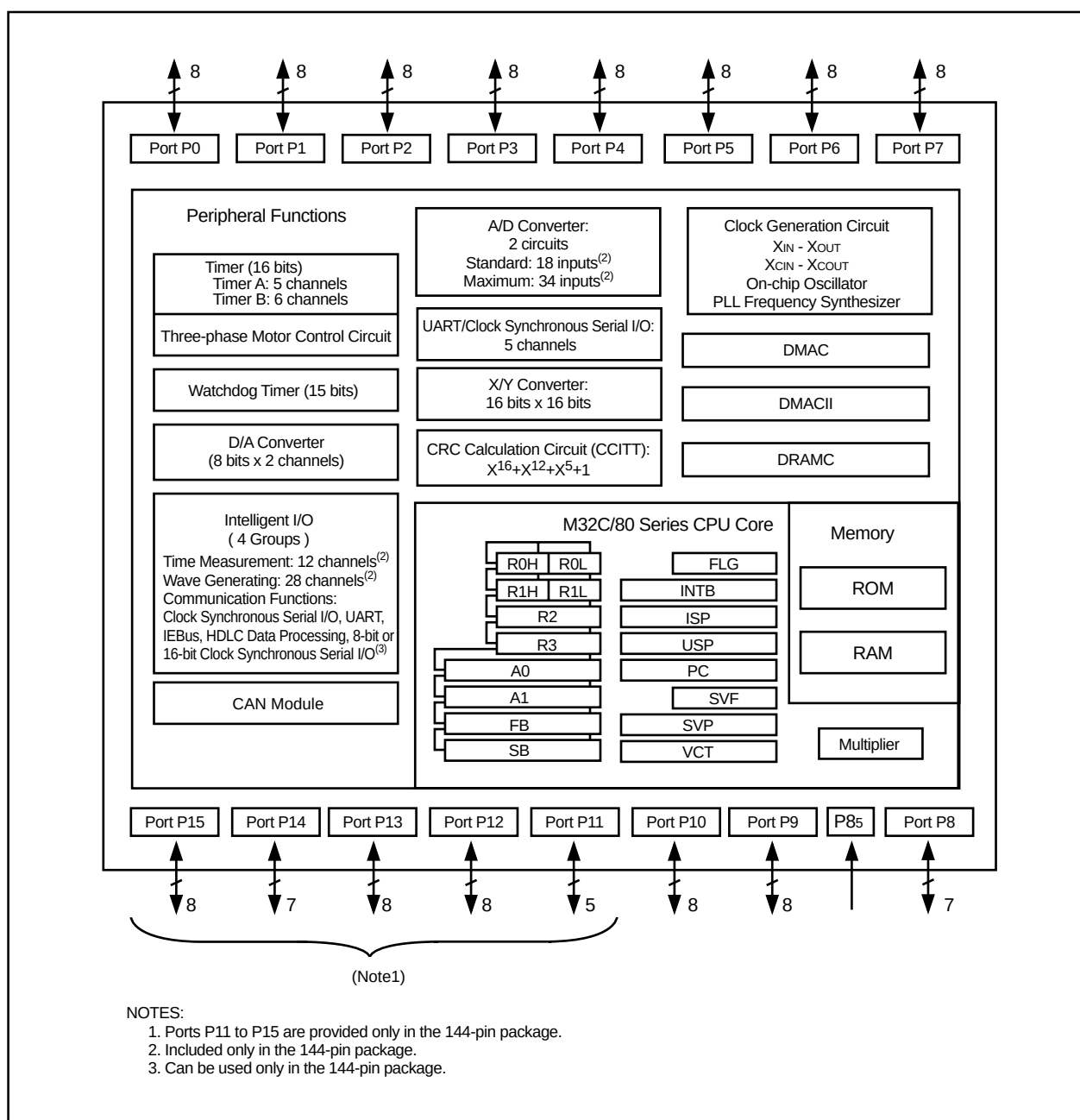


Figure 1.1 M32C/83 Group (M32C/83, M32C/83T) Block Diagram

1.4 Product Information

Table 1.3 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.3 M32C/83 Group (1) (M32C/83)

As of January, 2006

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30835FJGP	PLQP0144KA-A (144P6Q-A)	512K	31K	Flash Memory
M30833FJGP	PLQP0100KB-A (100P6Q-A)			
M30833FJFP	PRQP0100JB-A (100P6S-A)			

Table 1.3 M32C/83 Group (2) (T Version, M32C/83T)

As of January, 2006

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30833FJTGP	PLQP0100KB-A (100P6Q-A)	512K	31K	Flash Memory T Version (High-reliability 85°C Version)

Please contact our sales office for V version information.

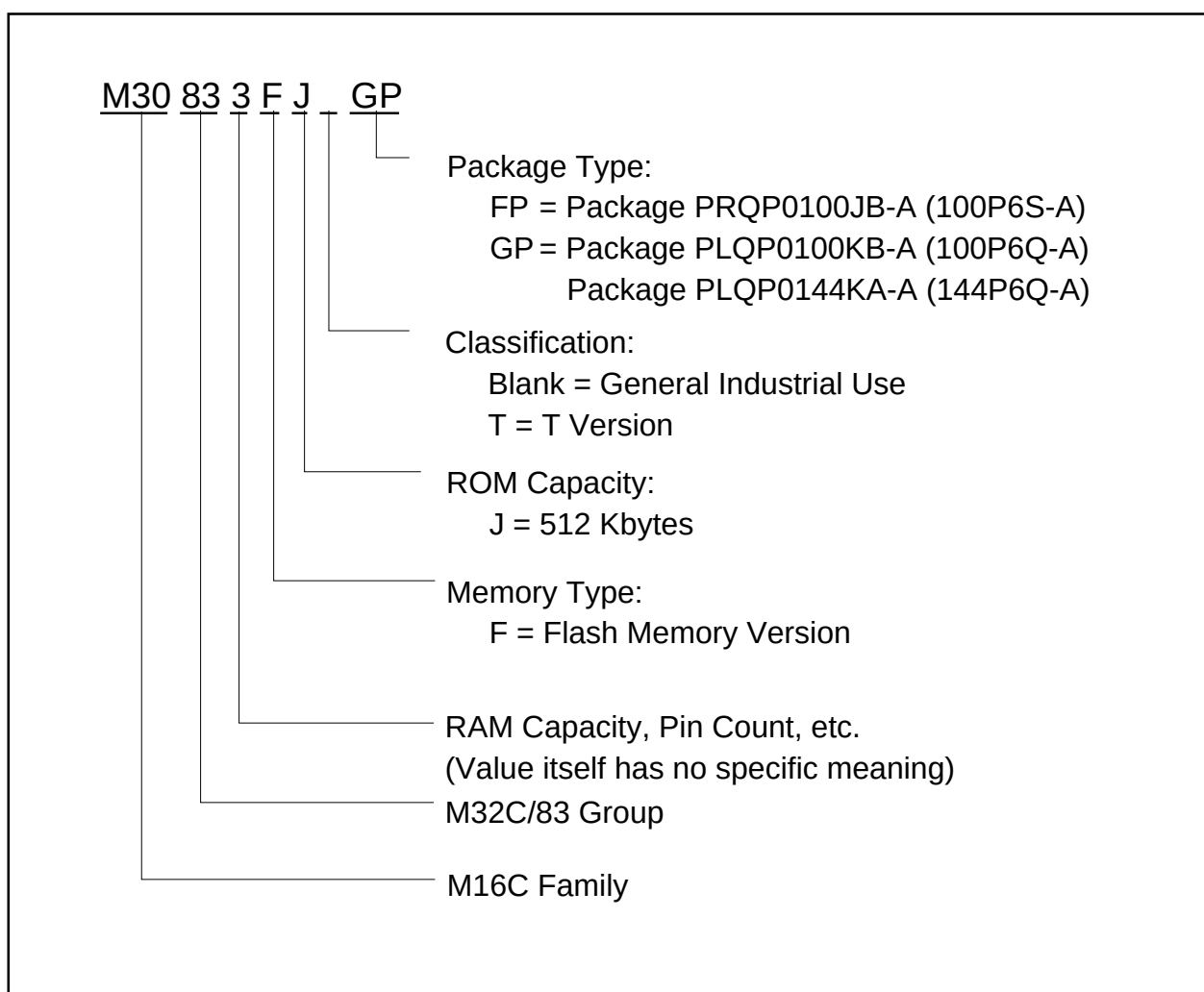


Figure 1.2 Product Numbering System

1.5 Pin Assignment

Figures 1.3 to 1.5 show pin assignments (top view).

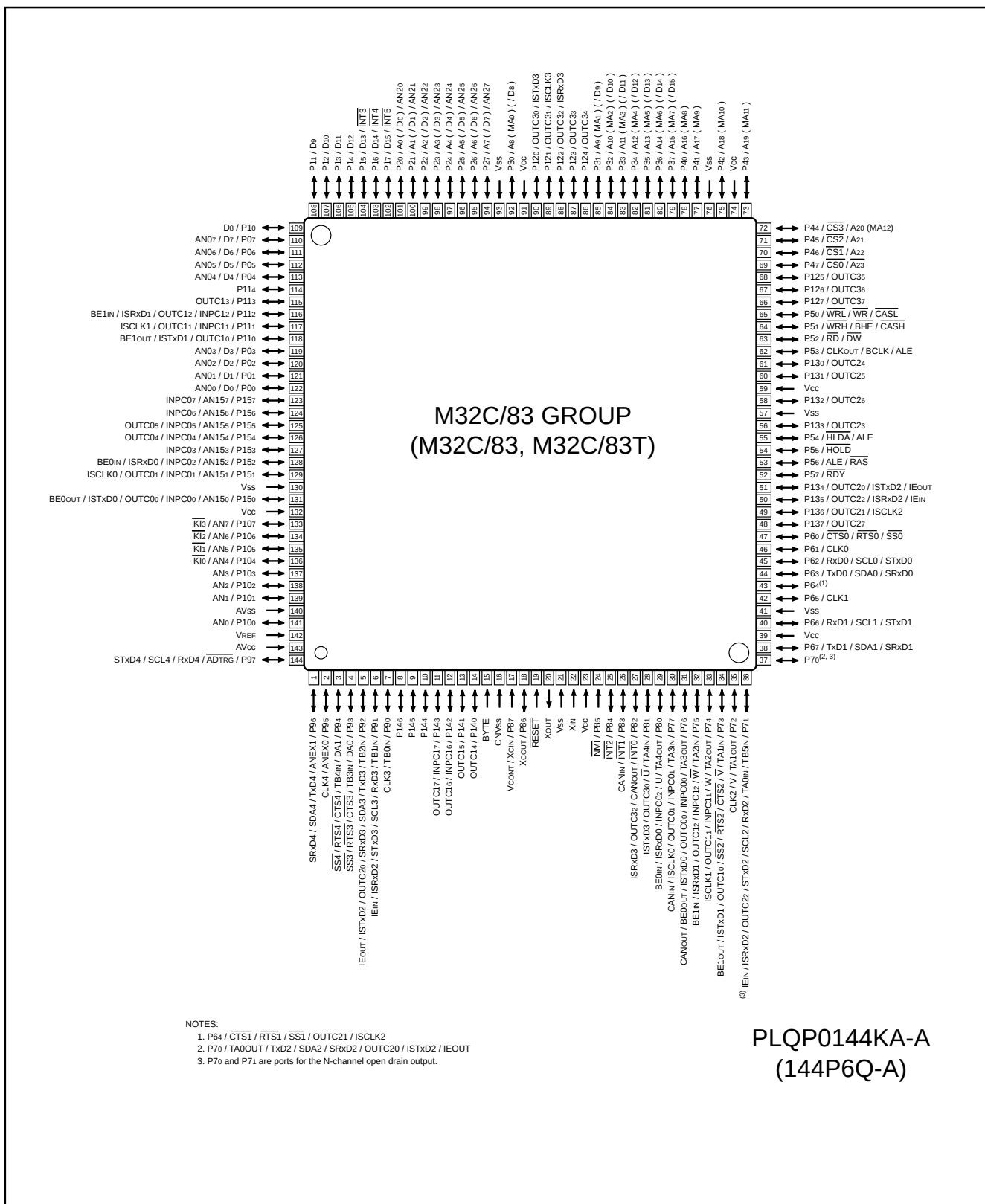


Figure 1.3 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
1		P96			TxD4/SDA4/SRx4D4		ANEX1	
2		P95			CLK4		ANEX0	
3		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5		P92		TB2IN	TxD3/SDA3/SRx3D3	OUTC20/IEOUT/ISTxD2		
6		P91		TB1IN	RxD3/SCL3/STxD3	IEIN/ISRxD2		
7		P90		TB0IN	CLK3			
8		P146						
9		P145						
10		P144						
11		P143				INPC17/OUTC17		
12		P142				INPC16/OUTC16		
13		P141				OUTC15		
14		P140				OUTC14		
15	BYTE							
16	CNVSS							
17	XCIN/VCONT	P87						
18	XCOUT	P86						
19	RESET							
20	XOUT							
21	VSS							
22	XIN							
23	VCC							
24		P85	NMI					
25		P84	INT2					
26		P83	INT1		CANIN			
27		P82	INT0		CANOUT	OUTC32/ISRxD3		
28		P81		TA4IN/U		OUTC30/ISTxD3		
29		P80		TA4OUT/U		INPC02/ISRxD0/BE0IN		
30		P77		TA3IN	CANIN	INPC01/OUTC01/ISCLK0		
31		P76		TA3OUT	CANOUT	INPC00/OUTC00/ISTxD0/BE0OUT		
32		P75		TA2IN/W		INPC12/OUTC12/ISRxD1/BE1IN		
33		P74		TA2OUT/W		INPC11/OUTC11/ISCLK1		
34		P73		TA1IN/V	CTS2/RTS2/SS2	OUTC10/ISTxD1/BE1OUT		
35		P72		TA1OUT/V	CLK2			
36		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2	OUTC22/ISRxD2/IEIN		
37		P70		TA0OUT	TxD2/SDA2/SRx2D2	OUTC20/ISTxD2/IEOUT		
38		P67			TxD1/SDA1/SRx1D1			
39	VCC							
40		P66			RxD1/SCL1/STxD1			
41	VSS							
42		P65			CLK1			
43		P64			CTS1/RTS1/SS1	OUTC21/ISCLK2		
44		P63			TxD0/SDA0/SRx0D0			
45		P62			RxD0/SCL0/STxD0			
46		P61			CLK0			
47		P60			CTS0/RTS0/SS0			
48		P137				OUTC27		

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
49		P136				OUTC21/ISCLK2		
50		P135				OUTC22/ISRxD2/IEiN		
51		P134				OUTC20/ISTxD2/IEoUT		
52		P57						RDY
53		P56						ALE/RAS
54		P55						HOLD
55		P54						HLDA/ALE
56		P133				OUTC23		
57	Vss							
58		P132				OUTC26		
59	Vcc							
60		P131				OUTC25		
61		P130				OUTC24		
62		P53						CLKOUT/BCLK/ALE
63		P52						RD/DW
64		P51						WRH/BHE/CASH
65		P50						WRL/WR/CASL
66		P127				OUTC37		
67		P126				OUTC36		
68		P125				OUTC35		
69		P47						CS0/A23
70		P46						CS1/A22
71		P45						CS2/A21
72		P44						CS3/A20(MA12)
73		P43						A19(MA11)
74	Vcc							
75		P42						A18(MA10)
76	Vss							
77		P41						A17(MA9)
78		P40						A16(MA8)
79		P37						A15(MA7)/(D15)
80		P36						A14(MA6)/(D14)
81		P35						A13(MA5)/(D13)
82		P34						A12(MA4)/(D12)
83		P33						A11(MA3)/(D11)
84		P32						A10(MA2)/(D10)
85		P31						A9(MA1)/(D9)
86		P124				OUTC34		
87		P123				OUTC33		
88		P122				OUTC32/ISRxD3		
89		P121				OUTC31/ISCLK3		
90		P120				OUTC30/ISTxD3		
91	Vcc							
92		P30						A8(MA0)/(D8)
93	Vss							
94		P27					AN27	A7/(D7)
95		P26					AN26	A6/(D6)
96		P25					AN25	A5/(D5)

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
97		P24					AN24	A4(/D4)
98		P23					AN23	A3(/D3)
99		P22					AN22	A2(/D2)
100		P21					AN21	A1(/D1)
101		P20					AN20	A0(/D0)
102		P17	INT5					D15
103		P16	INT4					D14
104		P15	INT3					D13
105		P14						D12
106		P13						D11
107		P12						D10
108		P11						D9
109		P10						D8
110		P07					AN07	D7
111		P06					AN06	D6
112		P05					AN05	D5
113		P04					AN04	D4
114		P114						
115		P113				OUTC13		
116		P112				INPC12/OUTC12/ISRxD1/BE1IN		
117		P111				INPC11/OUTC11/ISCLK1		
118		P110				OUTC10/ISTxD1/BE1OUT		
119		P03					AN03	D3
120		P02					AN02	D2
121		P01					AN01	D1
122		P00					AN00	D0
123		P157				INPC07	AN157	
124		P156				INPC06	AN156	
125		P155				INPC05/OUTC05	AN155	
126		P154				INPC04/OUTC04	AN154	
127		P153				INPC03	AN153	
128		P152				INPC02/ISRxD0/BE0IN	AN152	
129		P151				INPC01/OUTC01/ISCLK0	AN151	
130	VSS							
131		P150				INPC00/OUTC00/ISTxD0/BE0OUT	AN150	
132	VCC							
133		P107	KI3				AN7	
134		P106	KI2				AN6	
135		P105	KI1				AN5	
136		P104	KI0				AN4	
137		P103					AN3	
138		P102					AN2	
139		P101					AN1	
140	AVSS							
141		P100					AN0	
142	VREF							
143	AVCC							
144		P97			RxD4/SCL4/STxD4		ADTRG	

NOTES:

1. Bus control pins in M32C/83T cannot be used.

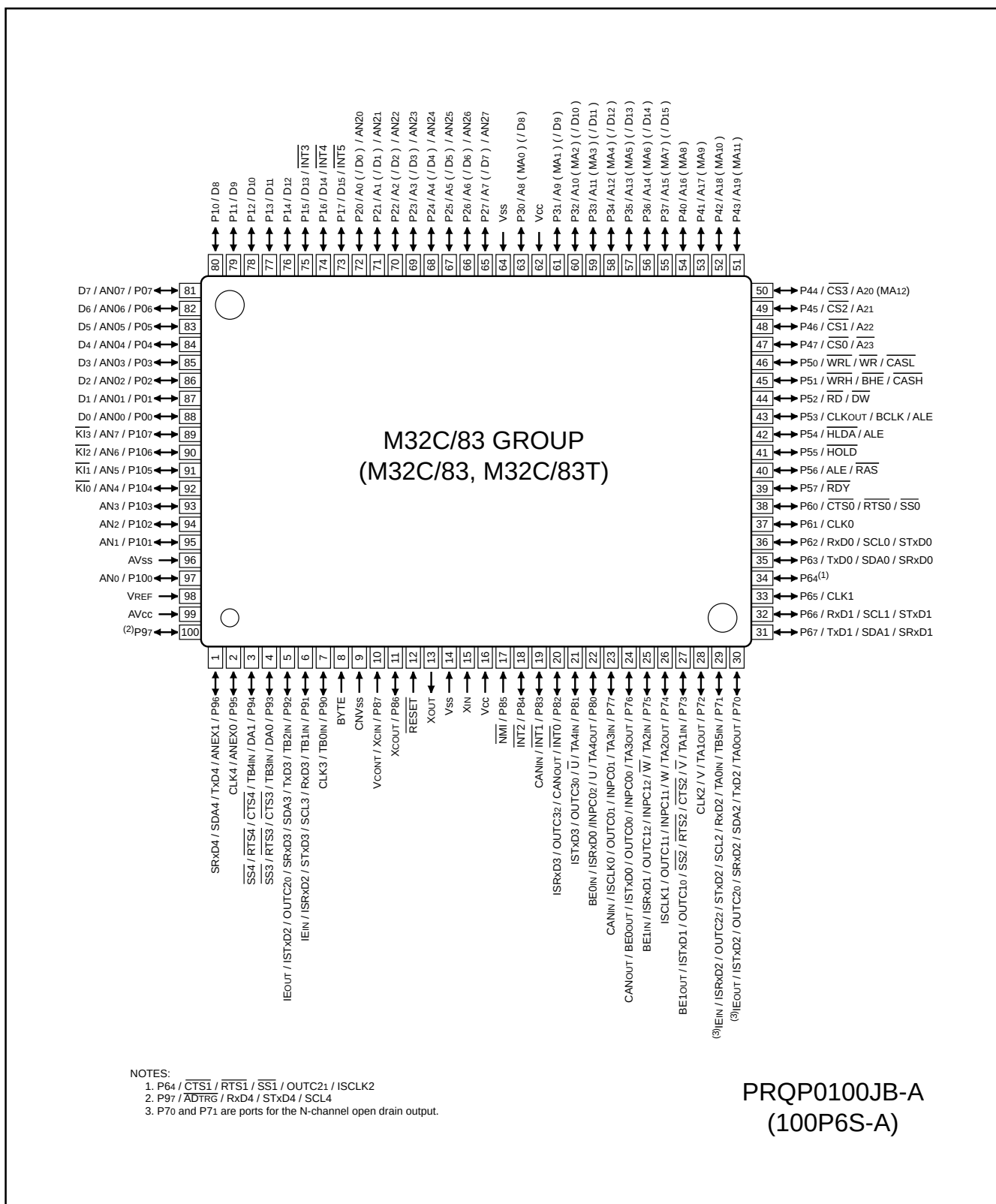


Figure 1.4 Pin Assignment for 100-Pin Package

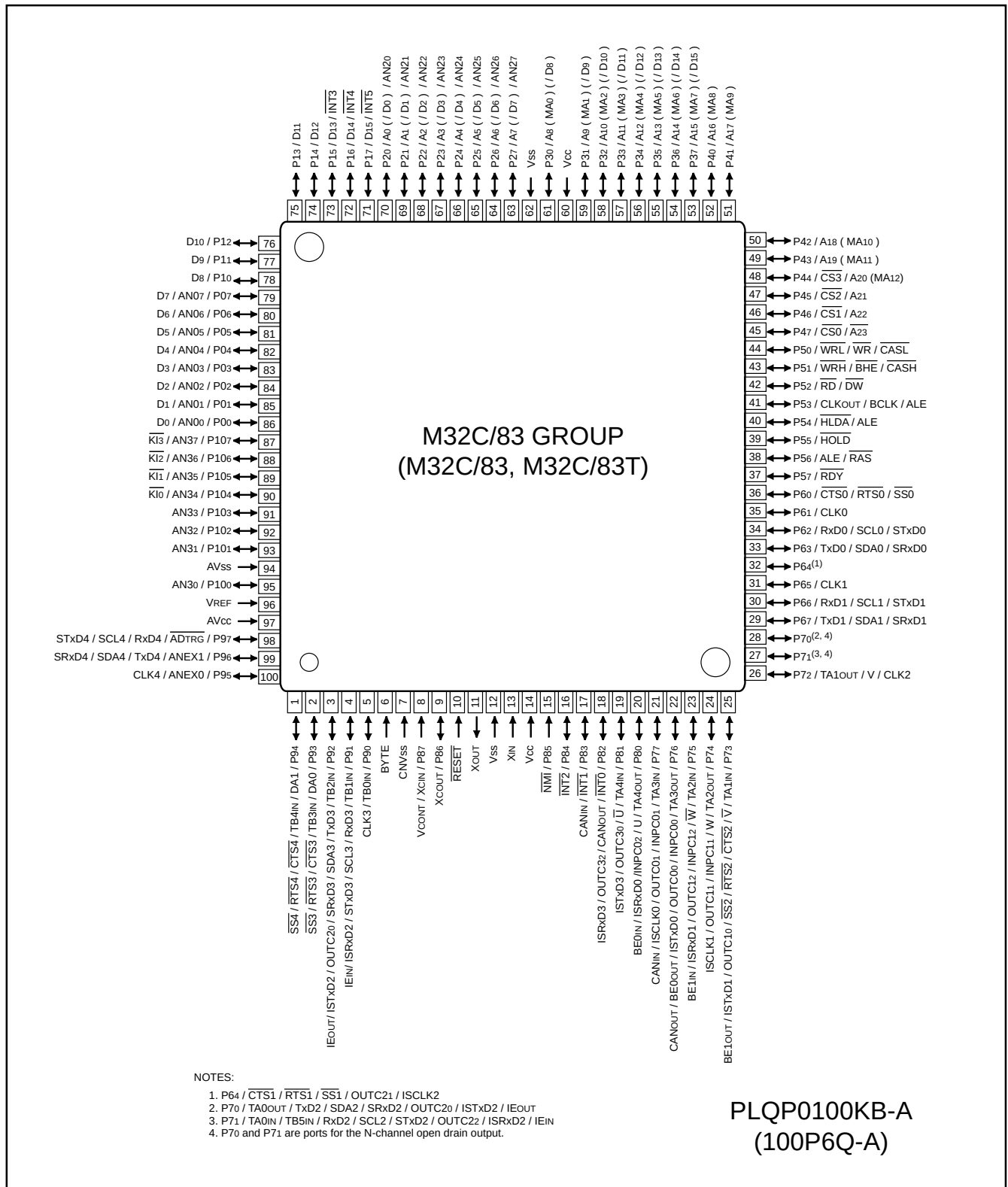


Figure 1.5 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
FP	GP								
1	99		P96			TxD4/SDA4/SRxD4		ANEX1	
2	100		P95			CLK4		ANEX0	
3	1		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P92		TB2IN	TxD3/SDA3/SRxD3	OUTC2 ₀ /IE _{OUT} /ISTxD2		
6	4		P91		TB1IN	RxD3/SCL3/STxD3	IE _{IN} /ISRxD2		
7	5		P90		TB0IN	CLK3			
8	6	BYTE							
9	7	CNV _{SS}							
10	8	X _{CIN} /V _{CONT}	P87						
11	9	X _{CO} UT	P86						
12	10	RESET							
13	11	X _{OUT}							
14	12	V _{SS}							
15	13	X _{IN}							
16	14	V _{CC}							
17	15		P85	NMI					
18	16		P84	INT2					
19	17		P83	INT1		CAN _{IN}			
20	18		P82	INT0		CAN _{OUT}	OUTC3 ₂ /ISRxD3		
21	19		P81		TA4 _{IN} /U		OUTC3 ₀ /ISTxD3		
22	20		P80		TA4 _{OUT} /U		INPC0 ₂ /ISRxD0/BE0 _{IN}		
23	21		P77		TA3 _{IN}	CAN _{IN}	INPC0 ₁ /OUTC0 ₁ /ISCLK0		
24	22		P76		TA3 _{OUT}	CAN _{OUT}	INPC0 ₀ /OUTC0 ₀ /ISTxD0/BE0 _{OUT}		
25	23		P75		TA2 _{IN} /W		INPC1 ₂ /OUTC1 ₂ /ISRxD1/BE1 _{IN}		
26	24		P74		TA2 _{OUT} /W		INPC1 ₁ /OUTC1 ₁ /ISCLK1		
27	25		P73		TA1 _{IN} /V	CTS2/RTS2/SS2	OUTC1 ₀ /ISTxD1/BE1 _{OUT}		
28	26		P72		TA1 _{OUT} /V	CLK2			
29	27		P71		TB5 _{IN} /TA0 _{IN}	RxD2/SCL2/STxD2	OUTC2 ₂ /ISRxD2/IE _{IN}		
30	28		P70		TA0 _{OUT}	TxD2/SDA2/SRxD2	OUTC2 ₀ /ISTxD2/IE _{OUT}		
31	29		P67			TxD1/SDA1/SRxD1			
32	30		P66			RxD1/SCL1/STxD1			
33	31		P65			CLK1			
34	32		P64			CTS1/RTS1/SS1	OUTC2 ₁ /ISCLK2		
35	33		P63			TxD0/SDA0/SRxD0			
36	34		P62			RxD0/SCL0/STxD0			
37	35		P61			CLK0			
38	36		P60			CTS0/RTS0/SS0			
39	37		P57						RDY
40	38		P56						ALE/RAS
41	39		P55						HOLD
42	40		P54						HLDA/ALE
43	41		P53						CLK _{OUT} /BCLK/ALE
44	42		P52						RD/DW
45	43		P51						WRH/BHE/CASH
46	44		P50						WRL/WR/CASL
47	45		P47						CS0/A ₂₃
48	46		P46						CS1/A ₂₂
49	47		P45						CS2/A ₂₁
50	48		P44						CS3/A ₂₀ (MA ₁₂)

NOTES:

1. Bus control pins in M32C/83T cannot be used.

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package Pin No		Control Pin	Port	Interrupt Pin	Timer Pin	UART/CAN Pin	Intelligent I/O Pin	Analog Pin	Bus Control Pin ⁽¹⁾
FP	GP								
51	49		P43						A19(MA11)
52	50		P42						A18(MA10)
53	51		P41						A17(MA9)
54	52		P40						A16(MA8)
55	53		P37						A15(MA7)/(D15)
56	54		P36						A14(MA6)/(D14)
57	55		P35						A13(MA5)/(D13)
58	56		P34						A12(MA4)/(D12)
59	57		P33						A11(MA3)/(D11)
60	58		P32						A10(MA2)/(D10)
61	59		P31						A9(MA1)/(D9)
62	60	VCC							
63	61		P30						A8(MA0)/(D8)
64	62	VSS							
65	63		P27					AN27	A7(/D7)
66	64		P26					AN26	A6(/D6)
67	65		P25					AN25	A5(/D5)
68	66		P24					AN24	A4(/D4)
69	67		P23					AN23	A3(/D3)
70	68		P22					AN22	A2(/D2)
71	69		P21					AN21	A1(/D1)
72	70		P20					AN20	A0(/D0)
73	71		P17	INT5					D15
74	72		P16	INT4					D14
75	73		P15	INT3					D13
76	74		P14						D12
77	75		P13						D11
78	76		P12						D10
79	77		P11						D9
80	78		P10						D8
81	79		P07					AN07	D7
82	80		P06					AN06	D6
83	81		P05					AN05	D5
84	82		P04					AN04	D4
85	83		P03					AN03	D3
86	84		P02					AN02	D2
87	85		P01					AN01	D1
88	86		P00					AN00	D0
89	87		P107	KI3				AN7	
90	88		P106	KI2				AN6	
91	89		P105	KI1				AN5	
92	90		P104	KI0				AN4	
93	91		P103					AN3	
94	92		P102					AN2	
95	93		P101					AN1	
96	94	AVSS							
97	95		P100					AN0	
98	96	VREF							
99	97	AVCC							
100	98		P97			RxD4/SCL4/STxD4		ADTRG	

NOTES:

1. Bus control pins in M32C/83T cannot be used.

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	Vcc Vss	I	Apply 3.0 to 5.5V to both Vcc pin. Apply 0V to the Vss pin. ⁽¹⁾
Analog Power Supply	AVcc AVss	I	Supplies power to the A/D converter. Connect the AVcc pin to Vcc and the AVss pin to Vss
Reset Input	RESET	I	The microcomputer is in a reset state when "L" is applied to the RESET pin
CNVss	CNVss	I	Switches processor mode. Connect the CNVss pin to Vss to start up in single-chip mode or to Vcc to start up in microprocessor mode
Input to Switch External Data Bus Width ⁽²⁾	BYTE	I	Switches data bus width in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when it is held "H". Set to either. Connect the BYTE pin to Vss to use the microcomputer in single-chip mode
Bus Control Pins ⁽²⁾	D0 to D7	I/O	Inputs and outputs data (D0 to D7) while accessing an external memory space with separate bus
	D8 to D15	I/O	Inputs and outputs data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A22	O	Outputs address bits A0 to A22
	A23	O	Outputs inversed address bit A23
	A0/D0 to A7/D7	I/O	Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing while accessing an external memory space with 16-bit multiplexed bus
	CS0 to CS3	O	Outputs CS0 to CS3 that are chip-select signals specifying an external space
	WRL / WR WRH / BHE RD	O	Outputs WRL, WRH, (WR, BHE) and RD signals. WRL and WRH can be switched with WR and BHE by program ■ WRL, WRH and RD selected: If external data bus is 16 bits wide, data is written to an even address in external memory space when WRL is held "L". Data is written to an odd address when WRH is held "L". Data is read when RD is held "L". ■ WR, BHE and RD selected: Data is written to external memory space when WR is held "L". Data in an external memory space is read when RD is held "L". An odd address is accessed when BHE is held "L". Select WR, BHE and RD for external 8-bit data bus.
	ALE	O	ALE is a signal latching the address
	HOLD	I	The microcomputer is placed in a hold state while the HOLD pin is held "L"
DRAM Bus Control Pin ⁽²⁾	HLDA	O	Outputs an "L" signal while the microcomputer is placed in a hold state
	RDY	I	Bus is placed in a wait state while the RDY pin is held "L"
	MA0 to MA12	O	When DRAM area is accessed, outputs column and row addresses by time-sharing.
	DW	O	The DW signal becomes "L" when data is written to the DRAM area. CASL and CASH are signals indicating the timing to latch column addresses. The CASL signal becomes "L" when an even address is accessed. The CASH signal becomes "L" when an odd address is accessed. RAS is a signal latching row addresses.
	CASL CASH RAS		

I : Input O : Output I/O : Input and output

NOTES:

1. Apply 4.2 to 5.5V to the Vcc pin when using M32C/83T.
2. Bus control pins in M32C/83T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classsification	Symbol	I/O Type	Function
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XOUT. To apply external clock, apply it to XCIN and leave XOUT open
Sub Clock Output	XOUT	O	
Low-Pass Filter Connect Pin for PLL Frequency Synthesizer Pin	VCONT		Connects the low-pass filter to the VCONT pin when using the PLL frequency synthesizer. Connect P86 to VSS to stabilize the PLL frequency.
BCLK Output ⁽¹⁾	BCLK	O	Outputs BCLK signal
Clock Output	CLKOUT	O	Outputs the clock having the same frequency as fc, f8 or f32
INT Interrupt Input	INT0 to INT5	I	Input pins for the INT interrupt
NMI Interrupt Input	NMI	I	Input pin for the NMI interrupt
Key Input Interrupt	KI0 to KI3	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	Input pins for the timer B0 to B5
Three-phase Motor Control Timer Output	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	Output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS4	I	Input pins for data transmission control
	RTS0 to RTS4	O	Output pins for data reception control
	CLK0 to CLK4	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	Inputs serial data
	TxD0 to TxD4	O	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I ² C Mode	SDA0 to SDA4	I/O	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4		Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)

I : Input O : Output I/O : Input and output

NOTE:

1. Bus control pins in M32C/83T cannot be used.

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Serial I/O Special Function	STxD0 to STxD4	O	Outputs serial data when slave mode is selected
	SRxD0 to SRxD4	I	Inputs serial data when slave mode is selected
	SS0 to SS4	I	Input pins to control serial I/O special function
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter and D/A converter
A/D Converter	AN0 to AN7 AN00 to AN07 AN20 to AN27 AN150 to AN157	I	Analog input pins for the A/D converter
	ADTRG	I	Input pin for an external A/D trigger
	ANEX0	I/O	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	Extended analog input pin for the A/D converter
	DA0, DA1	O	Output pin for the D/A converter
Intelligent I/O	INPC00 to INPC02	I	Input pins for the time measurement function
	INPC03 to INPC07 ⁽¹⁾		
	INPC11 to INPC12		
	INPC16 to INPC17 ⁽¹⁾		
	OUTC00 to OUTC02	O	Output pins for the waveform generating function (OUTC20 and OUTC22 assigned to P70 and P71 are pins for the N-channel open drain output.)
	OUTC04 to OUTC05 ⁽¹⁾		
	OUTC10 to OUTC12		
	OUTC13 to OUTC17 ⁽¹⁾		
	OUTC20 to OUTC22		
	OUTC23 to OUTC27 ⁽¹⁾		
	OUTC30 to OUTC32		
	OUTC31, OUTC33 to OUTC37 ⁽¹⁾		
	ISCLK0 to ISCLK2	I/O	Inputs and outputs the clock for the intelligent I/O communication function
	ISCLK3 ⁽¹⁾		
	ISRXD0 to ISRXD3	I	Inputs data for the intelligent I/O communication function
	ISTXD0 to ISTXD3	O	Outputs data for the intelligent I/O communication function
	BE0IN, BE1IN	I	Inputs data for the intelligent I/O communication function
	BE0OUT, BE1OUT	O	Outputs data for the intelligent I/O communication function
	IEIN	I	Inputs data for the intelligent I/O communication function
	IEOUT	O	Outputs data for the intelligent I/O communication function
CAN	CANIN	I	Input pin for the CAN communication function
	CANOUT	O	Output pin for the CAN communication function

I : Input O : Output I/O : Input and output

NOTE:

1. Available in the 144-pin package only.

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Classification	Symbol	I/O Type	Function
I/O Ports	P00 to P07 P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57 P60 to P67 P70 to P77 P90 to P97 P100 to P107	I/O	8-bit I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units (P70 and P71 are ports for the N-channel open drain output.)
	P110 to P114 P120 to P127 P130 to P137 P140 to P146 P150 to P157 (1)	I/O	I/O ports having equivalent functions to P0
	P80 to P84 P86, P87	I/O	I/O ports having equivalent functions to P0
Input Port	P85	I	Shares a pin with $\overline{\text{NMI}}$. $\overline{\text{NMI}}$ input state can be got by reading P85

I : Input O : Output I/O : Input and output

NOTE:

1. Available in the 144-pin package only.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.

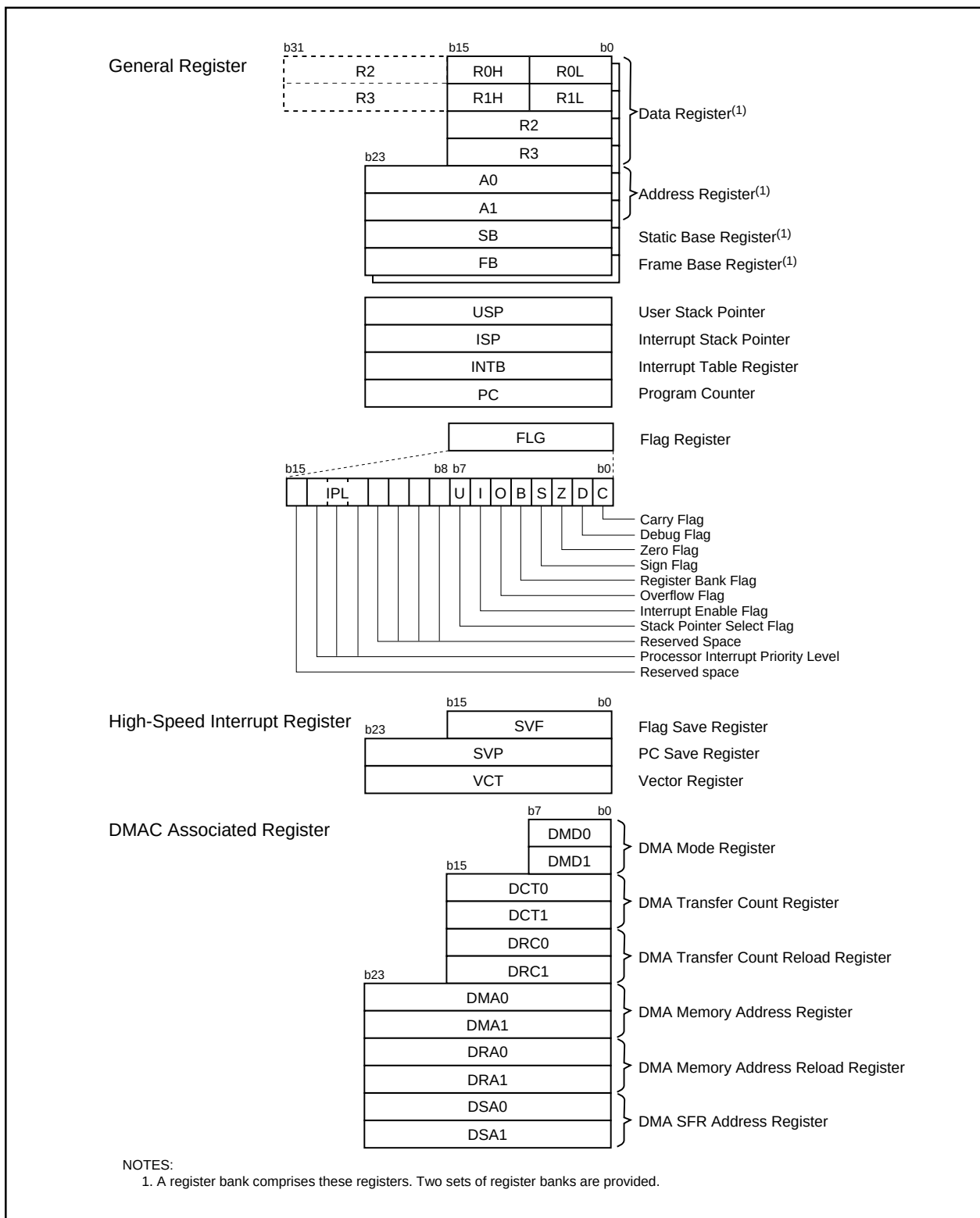


Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to "2.1.8 Flag Register (FLG)" for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows. Refer to **10.4 High-Speed Interrupt** for details.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows. Refer to **12. DMAC** for details.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/83 group (M32C/83, M32C/83T).

M32C/83 group (M32C/83, M32C/83T) provides 16-Mbyte address space from addresses 000000₁₆ to FFFFFFF₁₆.

The internal ROM is allocated lower addresses beginning with address FFFFFFF₁₆. For example, a 64-Kbyte internal ROM is allocated addresses FF0000₁₆ to FFFFFFF₁₆.

The fixed interrupt vectors are allocated addresses FFFFDC₁₆ to FFFFFFF₁₆. It stores the starting address of each interrupt routine. Refer to **10. Interrupts** for details.

The internal RAM is allocated higher addresses beginning with address 000400₁₆. For example, a 10-Kbyte internal RAM is allocated addresses 000400₁₆ to 002BFF₁₆. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, and timers, is allocated addresses 000000₁₆ to 0003FF₁₆. All addresses, which have nothing allocated within SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated addresses FFFE00₁₆ to FFFFDB₁₆. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.

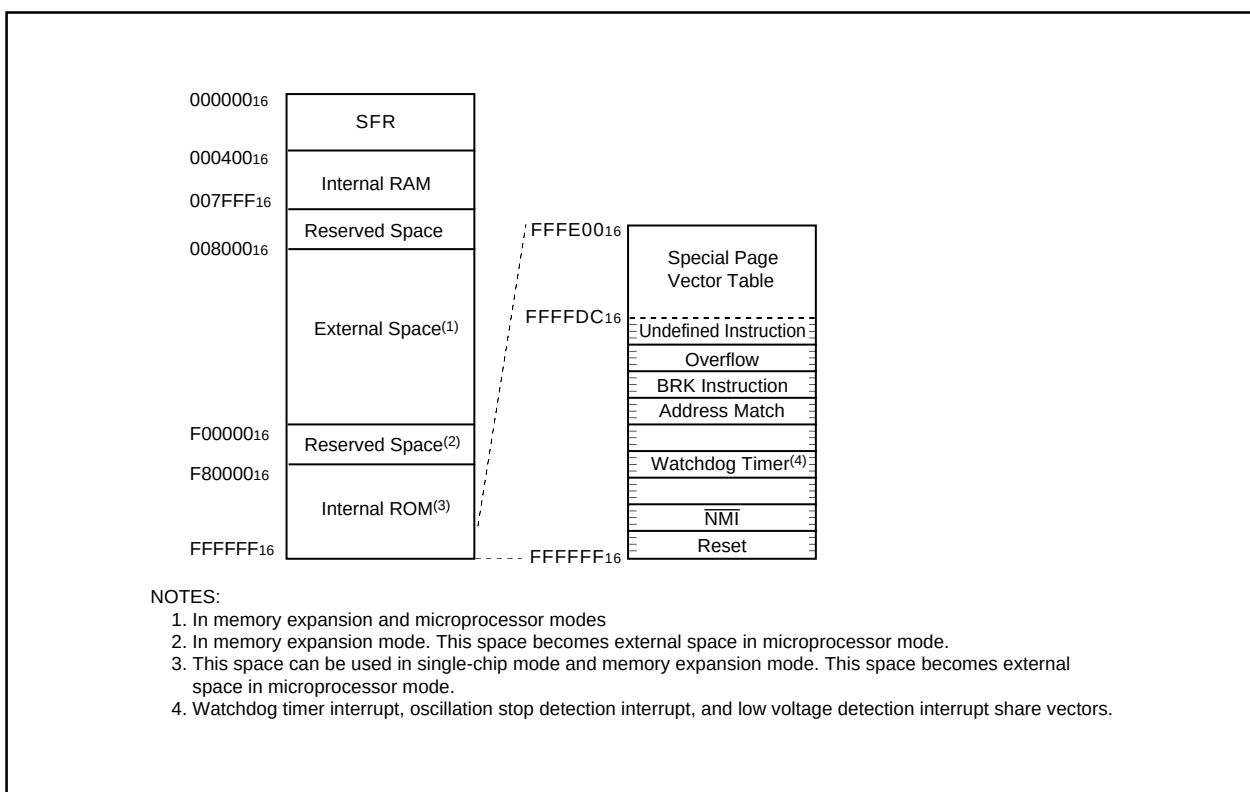


Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor Mode Register 0 ⁽¹⁾	PM0	1000 0000 ₂ (CNVss pin ="L") 0000 0011 ₂ (CNVss pin ="H")
0005 ₁₆	Processor Mode Register 1	PM1	0X00 0000 ₂
0006 ₁₆	System Clock Control Register 0	CM0	0000 X000 ₂
0007 ₁₆	System Clock Control Register 1	CM1	0010 0000 ₂
0008 ₁₆	Wait Control Register ⁽²⁾	WCR	1111 1111 ₂
0009 ₁₆	Address Match Interrupt Enable Register	AIER	XXXX 0000 ₂
000A ₁₆	Protect Register	PRCR	XXXX 0000 ₂
000B ₁₆	External Data Bus Width Control Register ⁽²⁾	DS	XXXX 1000 ₂ (BYTE pin ="L") XXXX 0000 ₂ (BYTE pin ="H")
000C ₁₆	Main Clock Division Register	MCD	XXX0 1000 ₂
000D ₁₆	Oscillation Stop Detection Register	CM2	00 ₁₆
000E ₁₆	Watchdog Timer Start Register	WDTS	XX ₁₆
000F ₁₆	Watchdog Timer Control Register	WDC	000X XXXX ₂
0010 ₁₆	Address Match Interrupt Register 0	RMAD0	00 00 00 ₁₆
0011 ₁₆			
0012 ₁₆			
0013 ₁₆			
0014 ₁₆	Address Match Interrupt Register 1	RMAD1	00 00 00 ₁₆
0015 ₁₆			
0016 ₁₆			
0017 ₁₆	VDC Control Register for PLL	PLV	XXXX XX01 ₂
0018 ₁₆	Address Match Interrupt Register 2	RMAD2	00 00 00 ₁₆
0019 ₁₆			
001A ₁₆			
001B ₁₆	VDC Control Register 0	VDC0	00 ₁₆
001C ₁₆	Address Match Interrupt Register 3	RMAD3	00 00 00 ₁₆
001D ₁₆			
001E ₁₆			
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The PM00 and PM01 bits in the PM1 register maintain values set before reset even if software reset or watchdog timer reset is performed.
2. These registers in M32C/83T cannot be used.

Address	Register	Symbol	Value after RESET
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			
0040 ₁₆	DRAM Control Register ⁽¹⁾	DRAMCONT	XX ₁₆
0041 ₁₆	DRAM Refresh Interval Set Register ⁽¹⁾	REFCNT	XX ₁₆
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆			
0049 ₁₆			
004A ₁₆			
004B ₁₆			
004C ₁₆			
004D ₁₆			
004E ₁₆			
004F ₁₆			
0050 ₁₆			
0051 ₁₆			
0052 ₁₆			
0053 ₁₆			
0054 ₁₆			
0055 ₁₆			
0056 ₁₆			
0057 ₁₆	Flash Memory Control Register 0	FMR0	XX00 0001 ₂
0058 ₁₆			
0059 ₁₆			
005A ₁₆			
005B ₁₆			
005C ₁₆			
005D ₁₆			
005E ₁₆			
005F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. These registers in M32C/83T cannot be used.

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
006916	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A16	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B16	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C16	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D16	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E16	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F16	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
007016	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
007116	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
007316	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
007416	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
007516	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X0002
007616	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
007716	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X0002
007816	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
007916	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A16	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B16	Intelligent I/O Interrupt Control Register 6	IIO6IC	XXXX X0002
007C16	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D16	Intelligent I/O Interrupt Control Register 8	IIO8IC	XXXX X0002
007E16	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F16	Intelligent I/O Interrupt Control Register 10/ CAN Interrupt 1 Control Register	IIO10IC CAN1IC	XXXX X0002
008016			
008116	Intelligent I/O Interrupt Control Register 11/ CAN Interrupt 2 Control Register	IIO11IC CAN2IC	XXXX X0002
008216			
008316			
008416			
008516			
008616	A/D1 Conversion Interrupt Control Register	AD1IC	XXXX X0002
008716			
008816	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
008916	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A16	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B16	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C16	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D16	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E16	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F16	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000 ₂
0092 ₁₆	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key Input Interrupt Control Register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 Interrupt Control Register	TB0IC	XXXX X000 ₂
0095 ₁₆	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000 ₂
0096 ₁₆	Timer B2 Interrupt Control Register	TB2IC	XXXX X000 ₂
0097 ₁₆	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000 ₂
0098 ₁₆	Timer B4 Interrupt Control Register	TB4IC	XXXX X000 ₂
0099 ₁₆	Intelligent I/O Interrupt Control Register 5	IIO5IC	XXXX X000 ₂
009A ₁₆	INT4 Interrupt Control Register	INT4IC	XX00 X000 ₂
009B ₁₆	Intelligent I/O Interrupt Control Register 7	IIO7IC	XXXX X000 ₂
009C ₁₆	INT2 Interrupt Control Register	INT2IC	XX00 X000 ₂
009D ₁₆	Intelligent I/O Interrupt Control Register 9/ CAN Interrupt 0 Control Register	IIO9IC CAN0IC	XXXX X000 ₂
009E ₁₆	INT0 Interrupt Control Register	INT0IC	XX00 X000 ₂
009F ₁₆	Exit Priority Control Register	RLVL	XXXX 0000 ₂
00A0 ₁₆	Interrupt Request Register 0	IIO0IR	0000 000X ₂
00A1 ₁₆	Interrupt Request Register 1	IIO1IR	0000 000X ₂
00A2 ₁₆	Interrupt Request Register 2	IIO2IR	0000 000X ₂
00A3 ₁₆	Interrupt Request Register 3	IIO3IR	0000 000X ₂
00A4 ₁₆	Interrupt Request Register 4	IIO4IR	0000 000X ₂
00A5 ₁₆	Interrupt Request Register 5	IIO5IR	0000 000X ₂
00A6 ₁₆	Interrupt Request Register 6	IIO6IR	0000 000X ₂
00A7 ₁₆	Interrupt Request Register 7	IIO7IR	0000 000X ₂
00A8 ₁₆	Interrupt Request Register 8	IIO8IR	0000 000X ₂
00A9 ₁₆	Interrupt Request Register 9	IIO9IR	0000 000X ₂
00AA ₁₆	Interrupt Request Register 10	IIO10IR	0000 000X ₂
00AB ₁₆	Interrupt Request Register 11	IIO11IR	0000 000X ₂
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt Enable Register 0	IIO0IE	00 ₁₆
00B1 ₁₆	Interrupt Enable Register 1	IIO1IE	00 ₁₆
00B2 ₁₆	Interrupt Enable Register 2	IIO2IE	00 ₁₆
00B3 ₁₆	Interrupt Enable Register 3	IIO3IE	00 ₁₆
00B4 ₁₆	Interrupt Enable Register 4	IIO4IE	00 ₁₆
00B5 ₁₆	Interrupt Enable Register 5	IIO5IE	00 ₁₆
00B6 ₁₆	Interrupt Enable Register 6	IIO6IE	00 ₁₆
00B7 ₁₆	Interrupt Enable Register 7	IIO7IE	00 ₁₆
00B8 ₁₆	Interrupt Enable Register 8	IIO8IE	00 ₁₆
00B9 ₁₆	Interrupt Enable Register 9	IIO9IE	00 ₁₆
00BA ₁₆	Interrupt Enable Register 10	IIO10IE	00 ₁₆
00BB ₁₆	Interrupt Enable Register 11	IIO11IE	00 ₁₆
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 ₁₆ 00C1 ₁₆	Group 0 Time Measurement/Waveform Generating Register 0	G0TM0/G0PO0	XX ₁₆ XX ₁₆
00C2 ₁₆ 00C3 ₁₆	Group 0 Time Measurement/Waveform Generating Register 1	G0TM1/G0PO1	XX ₁₆ XX ₁₆
00C4 ₁₆ 00C5 ₁₆	Group 0 Time Measurement/Waveform Generating Register 2	G0TM2/G0PO2	XX ₁₆ XX ₁₆
00C6 ₁₆ 00C7 ₁₆	Group 0 Time Measurement/Waveform Generating Register 3	G0TM3/G0PO3	XX ₁₆ XX ₁₆
00C8 ₁₆ 00C9 ₁₆	Group 0 Time Measurement/Waveform Generating Register 4	G0TM4/G0PO4	XX ₁₆ XX ₁₆
00CA ₁₆ 00CB ₁₆	Group 0 Time Measurement/Waveform Generating Register 5	G0TM5/G0PO5	XX ₁₆ XX ₁₆
00CC ₁₆ 00CD ₁₆	Group 0 Time Measurement/Waveform Generating Register 6	G0TM6/G0PO6	XX ₁₆ XX ₁₆
00CE ₁₆ 00CF ₁₆	Group 0 Time Measurement/Waveform Generating Register 7	G0TM7/G0PO7	XX ₁₆ XX ₁₆
00D0 ₁₆	Group 0 Waveform Generating Control Register 0	G0POCR0	0X00 X000 ₂
00D1 ₁₆	Group 0 Waveform Generating Control Register 1	G0POCR1	0X00 X000 ₂
00D2 ₁₆	Group 0 Waveform Generating Control Register 2	G0POCR2	0X00 X000 ₂
00D3 ₁₆	Group 0 Waveform Generating Control Register 3	G0POCR3	0X00 X000 ₂
00D4 ₁₆	Group 0 Waveform Generating Control Register 4	G0POCR4	0X00 X000 ₂
00D5 ₁₆	Group 0 Waveform Generating Control Register 5	G0POCR5	0X00 X000 ₂
00D6 ₁₆	Group 0 Waveform Generating Control Register 6	G0POCR6	0X00 X000 ₂
00D7 ₁₆	Group 0 Waveform Generating Control Register 7	G0POCR7	0X00 X000 ₂
00D8 ₁₆	Group 0 Time Measurement Control Register 0	G0TMCR0	00 ₁₆
00D9 ₁₆	Group 0 Time Measurement Control Register 1	G0TMCR1	00 ₁₆
00DA ₁₆	Group 0 Time Measurement Control Register 2	G0TMCR2	00 ₁₆
00DB ₁₆	Group 0 Time Measurement Control Register 3	G0TMCR3	00 ₁₆
00DC ₁₆	Group 0 Time Measurement Control Register 4	G0TMCR4	00 ₁₆
00DD ₁₆	Group 0 Time Measurement Control Register 5	G0TMCR5	00 ₁₆
00DE ₁₆	Group 0 Time Measurement Control Register 6	G0TMCR6	00 ₁₆
00DF ₁₆	Group 0 Time Measurement Control Register 7	G0TMCR7	00 ₁₆
00E0 ₁₆ 00E1 ₁₆	Group 0 Base Timer Register	G0BT	XX ₁₆ XX ₁₆
00E2 ₁₆	Group 0 Base Timer Control Register 0	G0BCR0	00 ₁₆
00E3 ₁₆	Group 0 Base Timer Control Register 1	G0BCR1	00 ₁₆
00E4 ₁₆	Group 0 Time Measurement Prescaler Register 6	G0TPR6	00 ₁₆
00E5 ₁₆	Group 0 Time Measurement Prescaler Register 7	G0TPR7	00 ₁₆
00E6 ₁₆	Group 0 Function Enable Register	G0FE	00 ₁₆
00E7 ₁₆	Group 0 Function Select Register	G0FS	00 ₁₆
00E8 ₁₆ 00E9 ₁₆	Group 0 SI/O Receive Buffer Register	G0RB	XXXX XXXX ₂ XX00 XXXX ₂
00EA ₁₆ 00EB ₁₆	Group 0 Transmit Buffer/Receive Data Register	G0TB/G0DR	XX ₁₆
00EC ₁₆	Group 0 Receive Input Register	G0RI	XX ₁₆
00ED ₁₆	Group 0 SI/O Communication Mode Register	G0MR	00 ₁₆
00EE ₁₆	Group 0 Transmit Output Register	G0TO	XX ₁₆
00EF ₁₆	Group 0 SI/O Communication Control Register	G0CR	0000 X000 ₂

X: Indeterminate

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Address	Register	Symbol	Value after RESET
00F0 ₁₆	Group 0 Data Compare Register 0	G0CMP0	XX ₁₆
00F1 ₁₆	Group 0 Data Compare Register 1	G0CMP1	XX ₁₆
00F2 ₁₆	Group 0 Data Compare Register 2	G0CMP2	XX ₁₆
00F3 ₁₆	Group 0 Data Compare Register 3	G0CMP3	XX ₁₆
00F4 ₁₆	Group 0 Data Mask Register 0	G0MSK0	XX ₁₆
00F5 ₁₆	Group 0 Data Mask Register 1	G0MSK1	XX ₁₆
00F6 ₁₆			
00F7 ₁₆			
00F8 ₁₆	Group 0 Receive CRC Code Register	G0RCRC	XX ₁₆
00F9 ₁₆			XX ₁₆
00FA ₁₆	Group 0 Transmit CRC Code Register	G0TCRC	00 ₁₆
00FB ₁₆			00 ₁₆
00FC ₁₆	Group 0 SI/O Extended Mode Register	G0EMR	00 ₁₆
00FD ₁₆	Group 0 SI/O Extended Receive Control Register	G0ERC	00 ₁₆
00FE ₁₆	Group 0 SI/O Special Communication Interrupt Detect Register	G0IRF	0000 00XX ₂
00FF ₁₆	Group 0 SI/O Extended Transmit Control Register	G0ETC	0000 0XXX ₂
0100 ₁₆	Group 1 Time Measurement/Waveform Generating Register 0	G1TM0/G1PO0	XX ₁₆
0101 ₁₆			XX ₁₆
0102 ₁₆	Group 1 Time Measurement/Waveform Generating Register 1	G1TM1/G1PO1	XX ₁₆
0103 ₁₆			XX ₁₆
0104 ₁₆	Group 1 Time Measurement/Waveform Generating Register 2	G1TM2/G1PO2	XX ₁₆
0105 ₁₆			XX ₁₆
0106 ₁₆	Group 1 Time Measurement/Waveform Generating Register 3	G1TM3/G1PO3	XX ₁₆
0107 ₁₆			XX ₁₆
0108 ₁₆	Group 1 Time Measurement/Waveform Generating Register 4	G1TM4/G1PO4	XX ₁₆
0109 ₁₆			XX ₁₆
010A ₁₆	Group 1 Time Measurement/Waveform Generating Register 5	G1TM5/G1PO5	XX ₁₆
010B ₁₆			XX ₁₆
010C ₁₆	Group 1 Time Measurement/Waveform Generating Register 6	G1TM6/G1PO6	XX ₁₆
010D ₁₆			XX ₁₆
010E ₁₆	Group 1 Time Measurement/Waveform Generating Register 7	G1TM7/G1PO7	XX ₁₆
010F ₁₆			XX ₁₆
0110 ₁₆	Group 1 Waveform Generating Control Register 0	G1POCR0	0X00 X000 ₂
0111 ₁₆	Group 1 Waveform Generating Control Register 1	G1POCR1	0X00 X000 ₂
0112 ₁₆	Group 1 Waveform Generating Control Register 2	G1POCR2	0X00 X000 ₂
0113 ₁₆	Group 1 Waveform Generating Control Register 3	G1POCR3	0X00 X000 ₂
0114 ₁₆	Group 1 Waveform Generating Control Register 4	G1POCR4	0X00 X000 ₂
0115 ₁₆	Group 1 Waveform Generating Control Register 5	G1POCR5	0X00 X000 ₂
0116 ₁₆	Group 1 Waveform Generating Control Register 6	G1POCR6	0X00 X000 ₂
0117 ₁₆	Group 1 Waveform Generating Control Register 7	G1POCR7	0X00 X000 ₂
0118 ₁₆	Group 1 Time Measurement Control Register 0	G1TMCR0	00 ₁₆
0119 ₁₆	Group 1 Time Measurement Control Register 1	G1TMCR1	00 ₁₆
011A ₁₆	Group 1 Time Measurement Control Register 2	G1TMCR2	00 ₁₆
011B ₁₆	Group 1 Time Measurement Control Register 3	G1TMCR3	00 ₁₆
011C ₁₆	Group 1 Time Measurement Control Register 4	G1TMCR4	00 ₁₆
011D ₁₆	Group 1 Time Measurement Control Register 5	G1TMCR5	00 ₁₆
011E ₁₆	Group 1 Time Measurement Control Register 6	G1TMCR6	00 ₁₆
011F ₁₆	Group 1 Time Measurement Control Register 7	G1TMCR7	00 ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0120 ₁₆	Group 1 Base Timer Register	G1BT	XX ₁₆
0121 ₁₆			XX ₁₆
0122 ₁₆	Group 1 Base Timer Control Register 0	G1BCR0	00 ₁₆
0123 ₁₆	Group 1 Base Timer Control Register 1	G1BCR1	00 ₁₆
0124 ₁₆	Group 1 Time Measurement Prescaler Register 6	G1TPR6	00 ₁₆
0125 ₁₆	Group 1 Time Measurement Prescaler Register 7	G1TPR7	00 ₁₆
0126 ₁₆	Group 1 Function Enable Register	G1FE	00 ₁₆
0127 ₁₆	Group 1 Function Select Register	G1FS	00 ₁₆
0128 ₁₆	Group 1 SI/O Receive Buffer Register	G1RB	XXXX XXXX ₂
0129 ₁₆			XX00 XXXX ₂
012A ₁₆	Group 1 Transmit Buffer/Receive Data Register	G1TB/G1DR	XX ₁₆
012B ₁₆			
012C ₁₆	Group 1 Receive Input Register	G1RI	XX ₁₆
012D ₁₆	Group 1 SI/O Communication Mode Register	G1MR	00 ₁₆
012E ₁₆	Group 1 Transmit Output Register	G1TO	XX ₁₆
012F ₁₆	Group 1 SI/O Communication Control Register	G1CR	0000 X000 ₂
0130 ₁₆	Group 1 Data Compare Register 0	G1CMP0	XX ₁₆
0131 ₁₆	Group 1 Data Compare Register 1	G1CMP1	XX ₁₆
0132 ₁₆	Group 1 Data Compare Register 2	G1CMP2	XX ₁₆
0133 ₁₆	Group 1 Data Compare Register 3	G1CMP3	XX ₁₆
0134 ₁₆	Group 1 Data Mask Register 0	G1MSK0	XX ₁₆
0135 ₁₆	Group 1 Data Mask Register 1	G1MSK1	XX ₁₆
0136 ₁₆			
0137 ₁₆			
0138 ₁₆	Group 1 Receive CRC Code Register	G1RCRC	XX ₁₆
0139 ₁₆			XX ₁₆
013A ₁₆	Group 1 Transmit CRC Code Register	G1TCRC	00 ₁₆
013B ₁₆			00 ₁₆
013C ₁₆	Group 1 SI/O Extended Mode Register	G1EMR	00 ₁₆
013D ₁₆	Group 1 SI/O Extended Receive Control Register	G1ERC	00 ₁₆
013E ₁₆	Group 1 SI/O Special Communication Interrupt Detect Register	G1IRF	0000 00XX ₂
013F ₁₆	Group 1 SI/O Extended Transmit Control Register	G1ETC	0000 0XXX ₂
0140 ₁₆	Group 2 Waveform Generating Register 0	G2PO0	XX ₁₆
0141 ₁₆			XX ₁₆
0142 ₁₆	Group 2 Waveform Generating Register 1	G2PO1	XX ₁₆
0143 ₁₆			XX ₁₆
0144 ₁₆	Group 2 Waveform Generating Register 2	G2PO2	XX ₁₆
0145 ₁₆			XX ₁₆
0146 ₁₆	Group 2 Waveform Generating Register 3	G2PO3	XX ₁₆
0147 ₁₆			XX ₁₆
0148 ₁₆	Group 2 Waveform Generating Register 4	G2PO4	XX ₁₆
0149 ₁₆			XX ₁₆
014A ₁₆	Group 2 Waveform Generating Register 5	G2PO5	XX ₁₆
014B ₁₆			XX ₁₆
014C ₁₆	Group 2 Waveform Generating Register 6	G2PO6	XX ₁₆
014D ₁₆			XX ₁₆
014E ₁₆	Group 2 Waveform Generating Register 7	G2PO7	XX ₁₆
014F ₁₆			XX ₁₆

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Address	Register	Symbol	Value after RESET
0150 ₁₆	Group 2 Waveform Generating Control Register 0	G2POCR0	00 ₁₆
0151 ₁₆	Group 2 Waveform Generating Control Register 1	G2POCR1	00 ₁₆
0152 ₁₆	Group 2 Waveform Generating Control Register 2	G2POCR2	00 ₁₆
0153 ₁₆	Group 2 Waveform Generating Control Register 3	G2POCR3	00 ₁₆
0154 ₁₆	Group 2 Waveform Generating Control Register 4	G2POCR4	00 ₁₆
0155 ₁₆	Group 2 Waveform Generating Control Register 5	G2POCR5	00 ₁₆
0156 ₁₆	Group 2 Waveform Generating Control Register 6	G2POCR6	00 ₁₆
0157 ₁₆	Group 2 Waveform Generating Control Register 7	G2POCR7	00 ₁₆
0158 ₁₆			
0159 ₁₆			
015A ₁₆			
015B ₁₆			
015C ₁₆			
015D ₁₆			
015E ₁₆			
015F ₁₆			
0160 ₁₆	Group 2 Base Timer Register	G2BT	XX ₁₆
0161 ₁₆			XX ₁₆
0162 ₁₆	Group 2 Base Timer Control Register 0	G2BCR0	00 ₁₆
0163 ₁₆	Group 2 Base Timer Control Register 1	G2BCR1	00 ₁₆
0164 ₁₆	Base Timer Start Register	BTSR	XXXX 0000 ₂
0165 ₁₆			
0166 ₁₆	Group 2 Function Enable Register	G2FE	00 ₁₆
0167 ₁₆	Group 2 RTP Output Buffer Register	G2RTP	00 ₁₆
0168 ₁₆			
0169 ₁₆			
016A ₁₆	Group 2 SI/O Communication Mode Register	G2MR	00XX X000 ₂
016B ₁₆	Group 2 SI/O Communication Control Register	G2CR	0000 X000 ₂
016C ₁₆	Group 2 SI/O Transmit Buffer Register	G2TB	XX ₁₆
016D ₁₆			XX ₁₆
016E ₁₆	Group 2 SI/O Receive Buffer Register	G2RB	XX ₁₆
016F ₁₆			XX ₁₆
0170 ₁₆	Group 2 IEBus Address Register	IEAR	XX ₁₆
0171 ₁₆			XX ₁₆
0172 ₁₆	Group 2 IEBus Control Register	IECR	00XX X000 ₂
0173 ₁₆	Group 2 IEBus Transmit Interrupt Cause Detect Register	IETIF	XXX0 0000 ₂
0174 ₁₆	Group 2 IEBus Receive Interrupt Cause Detect Register	IERIF	XXX0 0000 ₂
0175 ₁₆			
0176 ₁₆			
0177 ₁₆			
0178 ₁₆	Input Function Select Register	IPS	00 ₁₆
0179 ₁₆			
017A ₁₆	Group 3 SI/O Communication Mode Register	G3MR	00XX 0000 ₂
017B ₁₆	Group 3 SI/O Communication Control Register	G3CR	0000 X000 ₂
017C ₁₆	Group 3 SI/O Transmit Buffer Register	G3TB	XX ₁₆
017D ₁₆			XX ₁₆
017E ₁₆	Group 3 SI/O Receive Buffer Register	G3RB	XX ₁₆
017F ₁₆			XX ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0180 ₁₆ 0181 ₁₆	Group 3 Waveform Generating Register 0	G3PO0	XX ₁₆ XX ₁₆
0182 ₁₆ 0183 ₁₆	Group 3 Waveform Generating Register 1	G3PO1	XX ₁₆ XX ₁₆
0184 ₁₆ 0185 ₁₆	Group 3 Waveform Generating Register 2	G3PO2	XX ₁₆ XX ₁₆
0186 ₁₆ 0187 ₁₆	Group 3 Waveform Generating Register 3	G3PO3	XX ₁₆ XX ₁₆
0188 ₁₆ 0189 ₁₆	Group 3 Waveform Generating Register 4	G3PO4	XX ₁₆ XX ₁₆
018A ₁₆ 018B ₁₆	Group 3 Waveform Generating Register 5	G3PO5	XX ₁₆ XX ₁₆
018C ₁₆ 018D ₁₆	Group 3 Waveform Generating Register 6	G3PO6	XX ₁₆ XX ₁₆
018E ₁₆ 018F ₁₆	Group 3 Waveform Generating Register 7	G3PO7	XX ₁₆ XX ₁₆
0190 ₁₆	Group 3 Waveform Generating Control Register 0	G3POCR0	00 ₁₆
0191 ₁₆	Group 3 Waveform Generating Control Register 1	G3POCR1	00 ₁₆
0192 ₁₆	Group 3 Waveform Generating Control Register 2	G3POCR2	00 ₁₆
0193 ₁₆	Group 3 Waveform Generating Control Register 3	G3POCR3	00 ₁₆
0194 ₁₆	Group 3 Waveform Generating Control Register 4	G3POCR4	00 ₁₆
0195 ₁₆	Group 3 Waveform Generating Control Register 5	G3POCR5	00 ₁₆
0196 ₁₆	Group 3 Waveform Generating Control Register 6	G3POCR6	00 ₁₆
0197 ₁₆	Group 3 Waveform Generating Control Register 7	G3POCR7	00 ₁₆
0198 ₁₆ 0199 ₁₆	Group 3 Waveform Generating Mask Register 4	G3MK4	XX ₁₆ XX ₁₆
019A ₁₆ 019B ₁₆	Group 3 Waveform Generating Mask Register 5	G3MK5	XX ₁₆ XX ₁₆
019C ₁₆ 019D ₁₆	Group 3 Waveform Generating Mask Register 6	G3MK6	XX ₁₆ XX ₁₆
019E ₁₆ 019F ₁₆	Group 3 Waveform Generating Mask Register 7	G3MK7	XX ₁₆ XX ₁₆
01A0 ₁₆ 01A1 ₁₆	Group 3 Base Timer Register	G3BT	XX ₁₆ XX ₁₆
01A2 ₁₆	Group 3 Base Timer Control Register 0	G3BCR0	00 ₁₆
01A3 ₁₆	Group 3 Base Timer Control Register 1	G3BCR1	00 ₁₆
01A4 ₁₆			
01A5 ₁₆			
01A6 ₁₆	Group 3 Function Enable Register	G3FE	00 ₁₆
01A7 ₁₆	Group 3 RTP Output Buffer Register	G3RTP	00 ₁₆
01A8 ₁₆			
01A9 ₁₆			
01AA ₁₆			
01AB ₁₆			
01AC ₁₆			
01AD ₁₆	Group 3 SI/O Communication Flag Register	G3FLG	XXXX XXX0 ₂
01AE ₁₆			
01AF ₁₆			

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Address	Register	Symbol	Value after RESET
01B0 ₁₆			
01B1 ₁₆			
01B2 ₁₆			
01B3 ₁₆			
01B4 ₁₆			
01B5 ₁₆			
01B6 ₁₆			
01B7 ₁₆			
01B8 ₁₆			
01B9 ₁₆			
01BA ₁₆			
01BB ₁₆			
01BC ₁₆			
01BD ₁₆			
01BE ₁₆			
01BF ₁₆			
01C0 ₁₆ 01C1 ₁₆	A/D1 Register 0	AD10	XX ₁₆ XX ₁₆
01C2 ₁₆ 01C3 ₁₆	A/D1 Register 1	AD11	XX ₁₆ XX ₁₆
01C4 ₁₆ 01C5 ₁₆	A/D1 Register 2	AD12	XX ₁₆ XX ₁₆
01C6 ₁₆ 01C7 ₁₆	A/D1 Register 3	AD13	XX ₁₆ XX ₁₆
01C8 ₁₆ 01C9 ₁₆	A/D1 Register 4	AD14	XX ₁₆ XX ₁₆
01CA ₁₆ 01CB ₁₆	A/D1 Register 5	AD15	XX ₁₆ XX ₁₆
01CC ₁₆ 01CD ₁₆	A/D1 Register 6	AD16	XX ₁₆ XX ₁₆
01CE ₁₆ 01CF ₁₆	A/D1 Register 7	AD17	XX ₁₆ XX ₁₆
01D0 ₁₆			
01D1 ₁₆			
01D2 ₁₆			
01D3 ₁₆			
01D4 ₁₆ 01D5 ₁₆	A/D1 Control Register 2	AD1CON2	X00X X000 ₂
01D6 ₁₆ 01D7 ₁₆	A/D1 Control Register 0	AD1CON0	00 ₁₆
01D8 ₁₆ 01D9 ₁₆	A/D1 Control Register 1	AD1CON1	XX00 0000 ₂
01DA ₁₆			
01DB ₁₆			
01DC ₁₆			
01DD ₁₆			
01DE ₁₆			
01DF ₁₆			

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Address	Register	Symbol	Value after RESET
01E0 ₁₆	CAN0 Message Slot Buffer 0 Standard ID0	C0SLOT0_0	XX ₁₆
01E1 ₁₆	CAN0 Message Slot Buffer 0 Standard ID1	C0SLOT0_1	XX ₁₆
01E2 ₁₆	CAN0 Message Slot Buffer 0 Extended ID0	C0SLOT0_2	XX ₁₆
01E3 ₁₆	CAN0 Message Slot Buffer 0 Extended ID1	C0SLOT0_3	XX ₁₆
01E4 ₁₆	CAN0 Message Slot Buffer 0 Extended ID2	C0SLOT0_4	XX ₁₆
01E5 ₁₆	CAN0 Message Slot Buffer 0 Data Length Code	C0SLOT0_5	XX ₁₆
01E6 ₁₆	CAN0 Message Slot Buffer 0 Data 0	C0SLOT0_6	XX ₁₆
01E7 ₁₆	CAN0 Message Slot Buffer 0 Data 1	C0SLOT0_7	XX ₁₆
01E8 ₁₆	CAN0 Message Slot Buffer 0 Data 2	C0SLOT0_8	XX ₁₆
01E9 ₁₆	CAN0 Message Slot Buffer 0 Data 3	C0SLOT0_9	XX ₁₆
01EA ₁₆	CAN0 Message Slot Buffer 0 Data 4	C0SLOT0_10	XX ₁₆
01EB ₁₆	CAN0 Message Slot Buffer 0 Data 5	C0SLOT0_11	XX ₁₆
01EC ₁₆	CAN0 Message Slot Buffer 0 Data 6	C0SLOT0_12	XX ₁₆
01ED ₁₆	CAN0 Message Slot Buffer 0 Data 7	C0SLOT0_13	XX ₁₆
01EE ₁₆	CAN0 Message Slot Buffer 0 Time Stamp High-Order	C0SLOT0_14	XX ₁₆
01EF ₁₆	CAN0 Message Slot Buffer 0 Time Stamp Low-Order	C0SLOT0_15	XX ₁₆
01F0 ₁₆	CAN0 Message Slot Buffer 1 Standard ID0	C0SLOT1_0	XX ₁₆
01F1 ₁₆	CAN0 Message Slot Buffer 1 Standard ID1	C0SLOT1_1	XX ₁₆
01F2 ₁₆	CAN0 Message Slot Buffer 1 Extended ID0	C0SLOT1_2	XX ₁₆
01F3 ₁₆	CAN0 Message Slot Buffer 1 Extended ID1	C0SLOT1_3	XX ₁₆
01F4 ₁₆	CAN0 Message Slot Buffer 1 Extended ID2	C0SLOT1_4	XX ₁₆
01F5 ₁₆	CAN0 Message Slot Buffer 1 Data Length Code	C0SLOT1_5	XX ₁₆
01F6 ₁₆	CAN0 Message Slot Buffer 1 Data 0	C0SLOT1_6	XX ₁₆
01F7 ₁₆	CAN0 Message Slot Buffer 1 Data 1	C0SLOT1_7	XX ₁₆
01F8 ₁₆	CAN0 Message Slot Buffer 1 Data 2	C0SLOT1_8	XX ₁₆
01F9 ₁₆	CAN0 Message Slot Buffer 1 Data 3	C0SLOT1_9	XX ₁₆
01FA ₁₆	CAN0 Message Slot Buffer 1 Data 4	C0SLOT1_10	XX ₁₆
01FB ₁₆	CAN0 Message Slot Buffer 1 Data 5	C0SLOT1_11	XX ₁₆
01FC ₁₆	CAN0 Message Slot Buffer 1 Data 6	C0SLOT1_12	XX ₁₆
01FD ₁₆	CAN0 Message Slot Buffer 1 Data 7	C0SLOT1_13	XX ₁₆
01FE ₁₆	CAN0 Message Slot Buffer 1 Time Stamp High-Order	C0SLOT1_14	XX ₁₆
01FF ₁₆	CAN0 Message Slot Buffer 1 Time Stamp Low-Order	C0SLOT1_15	XX ₁₆
0200 ₁₆ 0201 ₁₆	CAN0 Control Register 0	C0CTLR0	XX01 0X01 ₂ ⁽¹⁾ XXXX 0000 ₂ ⁽¹⁾
0202 ₁₆ 0203 ₁₆	CAN0 Status Register	C0STR	0000 0000 ₂ ⁽¹⁾ X000 0X01 ₂ ⁽¹⁾
0204 ₁₆ 0205 ₁₆	CAN0 Extended ID Register	C0IDR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
0206 ₁₆ 0207 ₁₆	CAN0 Configuration Register	C0CONR	0000 XXXX ₂ ⁽¹⁾ 0000 0000 ₂ ⁽¹⁾
0208 ₁₆ 0209 ₁₆	CAN0 Time Stamp Register	C0TSR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
020A ₁₆	CAN0 Transmit Error Count Register	C0TEC	00 ₁₆ ⁽¹⁾
020B ₁₆	CAN0 Receive Error Count Register	C0REC	00 ₁₆ ⁽¹⁾
020C ₁₆ 020D ₁₆	CAN0 Slot Interrupt Status Register	C0SISTR	00 ₁₆ ⁽¹⁾ 00 ₁₆ ⁽¹⁾
020E ₁₆			
020F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
0210 ₁₆	CAN0 Slot Interrupt Mask Register	C0SIMKR	00 ₁₆ ⁽²⁾
0211 ₁₆			00 ₁₆ ⁽²⁾
0212 ₁₆			
0213 ₁₆			
0214 ₁₆	CAN0 Error Interrupt Mask Register	C0EIMKR	XXXX X000 ₂ ⁽²⁾
0215 ₁₆	CAN0 Error Interrupt Status Register	C0EISTR	XXXX X000 ₂ ⁽²⁾
0216 ₁₆			
0217 ₁₆	CAN0 Baud Rate Prescaler	C0BRP	0000 0001 ₂ ⁽²⁾
0218 ₁₆			
0219 ₁₆			
021A ₁₆			
021B ₁₆			
021C ₁₆			
021D ₁₆			
021E ₁₆			
021F ₁₆			
0220 ₁₆			
0221 ₁₆			
0222 ₁₆			
0223 ₁₆			
0224 ₁₆			
0225 ₁₆			
0226 ₁₆			
0227 ₁₆			
0228 ₁₆	CAN0 Global Mask Register Standard ID0	C0GMR0	XXX0 0000 ₂ ⁽²⁾
0229 ₁₆	CAN0 Global Mask Register Standard ID1	C0GMR1	XX00 0000 ₂ ⁽²⁾
022A ₁₆	CAN0 Global Mask Register Extended ID0	C0GMR2	XXXX 0000 ₂ ⁽²⁾
022B ₁₆	CAN0 Global Mask Register Extended ID1	C0GMR3	00 ₁₆ ⁽²⁾
022C ₁₆	CAN0 Global Mask Register Extended ID2	C0GMR4	XX00 0000 ₂ ⁽²⁾
022D ₁₆			
022E ₁₆			
022F ₁₆			
0230 ₁₆	CAN0 Message Slot 0 Control Register /	C0MCTL0/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register A Standard ID0	C0LMAR0	XXX0 0000 ₂ ⁽²⁾
0231 ₁₆	CAN0 Message Slot 1 Control Register /	C0MCTL1/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register A Standard ID1	C0LMAR1	XX00 0000 ₂ ⁽²⁾
0232 ₁₆	CAN0 Message Slot 2 Control Register /	C0MCTL2/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register A Extended ID0	C0LMAR2	XXXX 0000 ₂ ⁽²⁾
0233 ₁₆	CAN0 Message Slot 3 Control Register /	C0MCTL3/	00 ₁₆ ⁽²⁾
	CAN0 Local Mask Register A Extended ID1	C0LMAR3	00 ₁₆ ⁽²⁾
0234 ₁₆	CAN0 Message Slot 4 Control Register /	C0MCTL4/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register A Extended ID2	C0LMAR4	XX00 0000 ₂ ⁽²⁾
0235 ₁₆	CAN0 Message Slot 5 Control Register	C0MCTL5	00 ₁₆ ⁽²⁾
0236 ₁₆	CAN0 Message Slot 6 Control Register	C0MCTL6	00 ₁₆ ⁽²⁾
0237 ₁₆	CAN0 Message Slot 7 Control Register	C0MCTL7	00 ₁₆ ⁽²⁾
0238 ₁₆	CAN0 Message Slot 8 Control Register /	C0MCTL8/	0000 0000 ₂ ⁽²⁾
	CAN0 Local Mask Register B Standard ID0	C0LMBR0	XXX0 0000 ₂ ⁽²⁾

(Note 1)

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET	
0239 ₁₆	CAN0 Message Slot 9 Control Register / CAN0 Local Mask Register B Standard ID1	C0MCTL9/ C0LMBR1	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾	↑ (Note 1) ↓
023A ₁₆	CAN0 Message Slot 10 Control Register / CAN0 Local Mask Register B Extended ID0	C0MCTL10/ C0LMBR2	0000 0000 ₂ ⁽²⁾ XXXX 0000 ₂ ⁽²⁾	
023B ₁₆	CAN0 Message Slot 11 Control Register / CAN0 Local Mask Register B Extended ID1	C0MCTL11/ C0LMBR3	00 ₁₆ ⁽²⁾ 00 ₁₆ ⁽²⁾	
023C ₁₆	CAN0 Message Slot 12 Control Register / CAN0 Local Mask Register B Extended ID2	C0MCTL12/ C0LMBR4	0000 0000 ₂ ⁽²⁾ XX00 0000 ₂ ⁽²⁾	
023D ₁₆	CAN0 Message Slot 13 Control Register	C0MCTL13	00 ₁₆ ⁽²⁾	
023E ₁₆	CAN0 Message Slot 14 Control Register	C0MCTL14	00 ₁₆ ⁽²⁾	
023F ₁₆	CAN0 Message Slot 15 Control Register	C0MCTL15	00 ₁₆ ⁽²⁾	
0240 ₁₆	CAN0 Slot Buffer Select Register	C0SBS	00 ₁₆ ⁽²⁾	
0241 ₁₆	CAN0 Control Register 1	C0CTLR1	XX00 00XX ₂ ⁽²⁾	
0242 ₁₆	CAN0 Sleep Control Register	C0SLPR	XXXX XXX0 ₂	
0243 ₁₆				
0244 ₁₆ 0245 ₁₆	CAN0 Acceptance Filter Support Register	C0AFS	00 ₁₆ ⁽²⁾ 01 ₁₆ ⁽²⁾	
0246 ₁₆				
0247 ₁₆				
0248 ₁₆				
0249 ₁₆				
024A ₁₆				
024B ₁₆				
024C ₁₆				
024D ₁₆				
024E ₁₆				
024F ₁₆				
0250 ₁₆				
0251 ₁₆				
0252 ₁₆				
0253 ₁₆				
0254 ₁₆				
0255 ₁₆				
0256 ₁₆				
0257 ₁₆				
0258 ₁₆				
0259 ₁₆				
025A ₁₆				
025B ₁₆				
025C ₁₆				
025D ₁₆				
025E ₁₆				
025F ₁₆				
0260 ₁₆				
0261 ₁₆ to 02BF ₁₆				

X: Indeterminate

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NOTES:

1. The BANKSEL bit in the C0CTLR1 register switches functions for addresses 0220₁₆ to 023F₁₆.
2. Values are obtained by setting the SLEEP bit in the C0SLPR register to "1" (sleep mode exited) and supplying a clock to the CAN module after reset.

Address	Register	Symbol	Value after RESET
02C0 ₁₆ 02C1 ₁₆	X0 Register Y0 Register	X0R,Y0R	XX ₁₆ XX ₁₆
02C2 ₁₆ 02C3 ₁₆	X1 Register Y1 Register	X1R,Y1R	XX ₁₆ XX ₁₆
02C4 ₁₆ 02C5 ₁₆	X2 Register Y2 Register	X2R,Y2R	XX ₁₆ XX ₁₆
02C6 ₁₆ 02C7 ₁₆	X3 Register Y3 Register	X3R,Y3R	XX ₁₆ XX ₁₆
02C8 ₁₆ 02C9 ₁₆	X4 Register Y4 Register	X4R,Y4R	XX ₁₆ XX ₁₆
02CA ₁₆ 02CB ₁₆	X5 Register Y5 Register	X5R,Y5R	XX ₁₆ XX ₁₆
02CC ₁₆ 02CD ₁₆	X6 Register Y6 Register	X6R,Y6R	XX ₁₆ XX ₁₆
02CE ₁₆ 02CF ₁₆	X7 Register Y7 Register	X7R,Y7R	XX ₁₆ XX ₁₆
02D0 ₁₆ 02D1 ₁₆	X8 Register Y8 Register	X8R,Y8R	XX ₁₆ XX ₁₆
02D2 ₁₆ 02D3 ₁₆	X9 Register Y9 Register	X9R,Y9R	XX ₁₆ XX ₁₆
02D4 ₁₆ 02D5 ₁₆	X10 Register Y10 Register	X10R,Y10R	XX ₁₆ XX ₁₆
02D6 ₁₆ 02D7 ₁₆	X11 Register Y11 Register	X11R,Y11R	XX ₁₆ XX ₁₆
02D8 ₁₆ 02D9 ₁₆	X12 Register Y12 Register	X12R,Y12R	XX ₁₆ XX ₁₆
02DA ₁₆ 02DB ₁₆	X13 Register Y13 Register	X13R,Y13R	XX ₁₆ XX ₁₆
02DC ₁₆ 02DD ₁₆	X14 Register Y14 Register	X14R,Y14R	XX ₁₆ XX ₁₆
02DE ₁₆ 02DF ₁₆	X15 Register Y15 Register	X15R,Y15R	XX ₁₆ XX ₁₆
02E0 ₁₆	XY Control Register	XYC	XXXX XX00 ₂
02E1 ₁₆			
02E2 ₁₆			
02E3 ₁₆			
02E4 ₁₆	UART1 Special Mode Register 4	U1SMR4	00 ₁₆
02E5 ₁₆	UART1 Special Mode Register 3	U1SMR3	00 ₁₆
02E6 ₁₆	UART1 Special Mode Register 2	U1SMR2	00 ₁₆
02E7 ₁₆	UART1 Special Mode Register	U1SMR	00 ₁₆
02E8 ₁₆	UART1 Transmit/Receive Mode Register	U1MR	00 ₁₆
02E9 ₁₆	UART1 Baud Rate Register	U1BRG	XX ₁₆
02EA ₁₆ 02EB ₁₆	UART1 Transmit Buffer Register	U1TB	XX ₁₆ XX ₁₆
02EC ₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000 ₂
02ED ₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010 ₂
02EE ₁₆ 02EF ₁₆	UART1 Receive Buffer Register	U1RB	XX ₁₆ XX ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 Special Mode Register 4	U4SMR4	00 ₁₆
02F5 ₁₆	UART4 Special Mode Register 3	U4SMR3	00 ₁₆
02F6 ₁₆	UART4 Special Mode Register 2	U4SMR2	00 ₁₆
02F7 ₁₆	UART4 Special Mode Register	U4SMR	00 ₁₆
02F8 ₁₆	UART4 Transmit/Receive Mode Register	U4MR	00 ₁₆
02F9 ₁₆	UART4 Baud Rate Register	U4BRG	XX ₁₆
02FA ₁₆	UART4 Transmit Buffer Register	U4TB	XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 Receive Buffer Register	U4RB	XX ₁₆
02FF ₁₆			XX ₁₆
0300 ₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 Register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 Register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 Register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-Phase PWM Control Register 0	INVC0	00 ₁₆
0309 ₁₆	Three-Phase PWM Control Register 1	INVC1	00 ₁₆
030A ₁₆	Three-Phase output Buffer Register 0	IDB0	XX11 1111 ₂
030B ₁₆	Three-Phase output Buffer Register 1	IDB1	XX11 1111 ₂
030C ₁₆	Dead Time Timer	DTT	XX ₁₆
030D ₁₆	Timer B2 Interrupt Generating Frequency Set Counter	ICTB2	XX ₁₆
030E ₁₆			
030F ₁₆			
0310 ₁₆	Timer B3 Register	TB3	XX ₁₆
0311 ₁₆			XX ₁₆
0312 ₁₆	Timer B4 Register	TB4	XX ₁₆
0313 ₁₆			XX ₁₆
0314 ₁₆	Timer B5 Register	TB5	XX ₁₆
0315 ₁₆			XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 Mode Register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 Mode Register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 Mode Register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External Interrupt Cause Select Register	IFSR	00 ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 Special Mode Register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 Special Mode Register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 Special Mode Register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 Special Mode Register	U3SMR	00 ₁₆
0328 ₁₆	UART3 Transmit/Receive Mode Register	U3MR	00 ₁₆
0329 ₁₆	UART3 Baud Rate Register	U3BRG	XX ₁₆
032A ₁₆	UART3 Transmit Buffer Register	U3TB	XX ₁₆
032B ₁₆			XX ₁₆
032C ₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010 ₂
032E ₁₆	UART3 Receive Buffer Register	U3RB	XX ₁₆
032F ₁₆			XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 Special Mode Register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 Special Mode Register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 Special Mode Register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 Special Mode Register	U2SMR	00 ₁₆
0338 ₁₆	UART2 Transmit/Receive Mode Register	U2MR	00 ₁₆
0339 ₁₆	UART2 Baud Rate Register	U2BRG	XX ₁₆
033A ₁₆	UART2 Transmit Buffer Register	U2TB	XX ₁₆
033B ₁₆			XX ₁₆
033C ₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010 ₂
033E ₁₆	UART2 Receive Buffer Register	U2RB	XX ₁₆
033F ₁₆			XX ₁₆
0340 ₁₆	Count Start Flag	TABSR	00 ₁₆
0341 ₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-Shot Start Flag	ONSF	00 ₁₆
0343 ₁₆	Trigger Select Register	TRGSR	00 ₁₆
0344 ₁₆	Up-Down Flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆	Timer A0 Register	TA0	XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆	Timer A1 Register	TA1	XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆	Timer A2 Register	TA2	XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆	Timer A3 Register	TA3	XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	Timer A4 Register	TA4	XX ₁₆
034F ₁₆			XX ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0350 ₁₆ 0351 ₁₆	Timer B0 Register	TB0	XX ₁₆ XX ₁₆
0352 ₁₆ 0353 ₁₆	Timer B1 Register	TB1	XX ₁₆ XX ₁₆
0354 ₁₆ 0355 ₁₆	Timer B2 Register	TB2	XX ₁₆ XX ₁₆
0356 ₁₆	Timer A0 Mode Register	TA0MR	0000 0X00 ₂
0357 ₁₆	Timer A1 Mode Register	TA1MR	0000 0X00 ₂
0358 ₁₆	Timer A2 Mode Register	TA2MR	0000 0X00 ₂
0359 ₁₆	Timer A3 Mode Register	TA3MR	0000 0X00 ₂
035A ₁₆	Timer A4 Mode Register	TA4MR	0000 0X00 ₂
035B ₁₆	Timer B0 Mode Register	TB0MR	00XX 0000 ₂
035C ₁₆	Timer B1 Mode register	TB1MR	00XX 0000 ₂
035D ₁₆	Timer B2 Mode Register	TB2MR	00XX 0000 ₂
035E ₁₆	Timer B2 Special Mode Register	TB2SC	XXXX XXX0 ₂
035F ₁₆	Count Source Prescaler Register ⁽¹⁾	TCSPR	0XXX 0000 ₂
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆	UART0 Special Mode Register 4	U0SMR4	00 ₁₆
0365 ₁₆	UART0 Special Mode Register 3	U0SMR3	00 ₁₆
0366 ₁₆	UART0 Special Mode Register 2	U0SMR2	00 ₁₆
0367 ₁₆	UART0 Special Mode Register	U0SMR	00 ₁₆
0368 ₁₆	UART0 Transmit/Receive Mode Register	U0MR	00 ₁₆
0369 ₁₆	UART0 Baud Rate Register	U0BRG	XX ₁₆
036A ₁₆ 036B ₁₆	UART0 Transmit Buffer Register	U0TB	XX ₁₆ XX ₁₆
036C ₁₆	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000 ₂
036D ₁₆	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010 ₂
036E ₁₆ 036F ₁₆	UART0 Receive Buffer Register	U0RB	XX ₁₆ XX ₁₆
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆	PLL Control Register 0	PLC0	0011 X100 ₂
0377 ₁₆	PLL Control Register 1	PLC1	XXXX 0000 ₂
0378 ₁₆	DMA0 Cause Select Register	DM0SL	0X00 0000 ₂
0379 ₁₆	DMA1 Cause Select Register	DM1SL	0X00 0000 ₂
037A ₁₆	DMA2 Cause Select Register	DM2SL	0X00 0000 ₂
037B ₁₆	DMA3 Cause Select Register	DM3SL	0X00 0000 ₂
037C ₁₆ 037D ₁₆	CRC Data Register	CRCD	XX ₁₆ XX ₁₆
037E ₁₆ 037F ₁₆	CRC Input Register	CRCIN	XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1. The TCSPR register maintains the values set before reset even if software reset or watchdog timer reset is performed.

Address	Register	Symbol	Value after RESET
0380 ₁₆ 0381 ₁₆	A/D0 Register 0	AD00	XX ₁₆ XX ₁₆
0382 ₁₆ 0383 ₁₆	A/D0 Register 1	AD01	XX ₁₆ XX ₁₆
0384 ₁₆ 0385 ₁₆	A/D0 Register 2	AD02	XX ₁₆ XX ₁₆
0386 ₁₆ 0387 ₁₆	A/D0 Register 3	AD03	XX ₁₆ XX ₁₆
0388 ₁₆ 0389 ₁₆	A/D0 Register 4	AD04	XX ₁₆ XX ₁₆
038A ₁₆ 038B ₁₆	A/D0 Register 5	AD05	XX ₁₆ XX ₁₆
038C ₁₆ 038D ₁₆	A/D0 Register 6	AD06	XX ₁₆ XX ₁₆
038E ₁₆ 038F ₁₆	A/D0 Register 7	AD07	XX ₁₆ XX ₁₆
0390 ₁₆			
0391 ₁₆			
0392 ₁₆			
0393 ₁₆			
0394 ₁₆ 0395 ₁₆	A/D0 Control Register 2	AD0CON2	X000 0000 ₂
0396 ₁₆	A/D0 Control Register 0	AD0CON0	00 ₁₆
0397 ₁₆	A/D0 Control Register 1	AD0CON1	00 ₁₆
0398 ₁₆ 0399 ₁₆	D/A Register 0	DA0	XX ₁₆
039A ₁₆ 039B ₁₆	D/A Register 1	DA1	XX ₁₆
039C ₁₆ 039D ₁₆	D/A Control Register	DACON	XXXX XX00 ₂
039E ₁₆			
039F ₁₆			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
03A0 ₁₆	Function Select Register A8	PS8	X000 0000 ₂
03A1 ₁₆	Function Select Register A9	PS9	00 ₁₆
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆			
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆			
03AD ₁₆			
03AE ₁₆			
03AF ₁₆	Function Select Register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function Select Register A0	PS0	00 ₁₆
03B1 ₁₆	Function Select Register A1	PS1	00 ₁₆
03B2 ₁₆	Function Select Register B0	PSL0	00 ₁₆
03B3 ₁₆	Function Select Register B1	PSL1	00 ₁₆
03B4 ₁₆	Function Select Register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function Select Register A3	PS3	00 ₁₆
03B6 ₁₆	Function Select Register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function Select Register B3	PSL3	00 ₁₆
03B8 ₁₆			
03B9 ₁₆	Function Select Register A5	PS5	XXX0 0000 ₂
03BA ₁₆			
03BB ₁₆			
03BC ₁₆	Function Select Register A6	PS6	00 ₁₆
03BD ₁₆	Function Select Register A7	PS7	00 ₁₆
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 Register	P6	XX ₁₆
03C1 ₁₆	Port P7 Register	P7	XX ₁₆
03C2 ₁₆	Port P6 Direction Register	PD6	00 ₁₆
03C3 ₁₆	Port P7 Direction Register	PD7	00 ₁₆
03C4 ₁₆	Port P8 Register	P8	XX ₁₆
03C5 ₁₆	Port P9 Register	P9	XX ₁₆
03C6 ₁₆	Port P8 Direction Register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 Direction Register	PD9	00 ₁₆
03C8 ₁₆	Port P10 Register	P10	XX ₁₆
03C9 ₁₆	Port P11 Register	P11	XX ₁₆
03CA ₁₆	Port P10 Direction Register	PD10	00 ₁₆
03CB ₁₆	Port P11 Direction Register	PD11	XXX0 0000 ₂
03CC ₁₆	Port P12 Register	P12	XX ₁₆
03CD ₁₆	Port P13 Register	P13	XX ₁₆
03CE ₁₆	Port P12 Direction Register	PD12	00 ₁₆
03CF ₁₆	Port P13 Direction Register	PD13	00 ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03D0 ₁₆	Port P14 Register	P14	XX ₁₆
03D1 ₁₆	Port P15 Register	P15	XX ₁₆
03D2 ₁₆	Port P14 Direction Register	PD14	X000 0000 ₂
03D3 ₁₆	Port P15 Direction Register	PD15	00 ₁₆
03D4 ₁₆			
03D5 ₁₆			
03D6 ₁₆			
03D7 ₁₆			
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆	Pull-Up Control Register 2	PUR2	00 ₁₆
03DB ₁₆	Pull-Up Control Register 3	PUR3	00 ₁₆
03DC ₁₆	Pull-Up Control Register 4	PUR4	XXXX 0000 ₂
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 Register	P0	XX ₁₆
03E1 ₁₆	Port P1 Register	P1	XX ₁₆
03E2 ₁₆	Port P0 Direction Register	PD0	00 ₁₆
03E3 ₁₆	Port P1 Direction Register	PD1	00 ₁₆
03E4 ₁₆	Port P2 Register	P2	XX ₁₆
03E5 ₁₆	Port P3 Register	P3	XX ₁₆
03E6 ₁₆	Port P2 Direction Register	PD2	00 ₁₆
03E7 ₁₆	Port P3 Direction Register	PD3	00 ₁₆
03E8 ₁₆	Port P4 Register	P4	XX ₁₆
03E9 ₁₆	Port P5 Register	P5	XX ₁₆
03EA ₁₆	Port P4 Direction Register	PD4	00 ₁₆
03EB ₁₆	Port P5 Direction Register	PD5	00 ₁₆
03EC ₁₆			
03ED ₁₆			
03EE ₁₆			
03EF ₁₆			
03F0 ₁₆	Pull-Up Control Register 0	PUR0	00 ₁₆
03F1 ₁₆	Pull-Up Control Register 1	PUR1	XXXX 0000 ₂
03F2 ₁₆			
03F3 ₁₆			
03F4 ₁₆			
03F5 ₁₆			
03F6 ₁₆			
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆	Port Control Register	PCR	XXXX XXX0 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<100-pin package>

Address	Register	Symbol	Value after RESET	
03A0 ₁₆				(Note 2)
03A1 ₁₆				
03A2 ₁₆				
03A3 ₁₆				
03A4 ₁₆				
03A5 ₁₆				
03A6 ₁₆				
03A7 ₁₆				
03A8 ₁₆				
03A9 ₁₆				
03AA ₁₆				
03AB ₁₆				
03AC ₁₆				
03AD ₁₆				
03AE ₁₆				
03AF ₁₆	Function Select Register C	PSC	0X00 0000 ₂	(Note 2)
03B0 ₁₆	Function Select Register A0	PS0	00 ₁₆	
03B1 ₁₆	Function Select Register A1	PS1	00 ₁₆	
03B2 ₁₆	Function Select Register B0	PSL0	00 ₁₆	
03B3 ₁₆	Function Select Register B1	PSL1	00 ₁₆	
03B4 ₁₆	Function Select Register A2	PS2	00X0 0000 ₂	
03B5 ₁₆	Function Select Register A3	PS3	00 ₁₆	
03B6 ₁₆	Function Select Register B2	PSL2	00X0 0000 ₂	
03B7 ₁₆	Function Select Register B3	PSL3	00 ₁₆	
03B8 ₁₆				
03B9 ₁₆				
03BA ₁₆				
03BB ₁₆				
03BC ₁₆				
03BD ₁₆				
03BE ₁₆				(Note 2)
03BF ₁₆				
03C0 ₁₆	Port P6 Register	P6	XX ₁₆	
03C1 ₁₆	Port P7 Register	P7	XX ₁₆	
03C2 ₁₆	Port P6 Direction Register	PD6	00 ₁₆	
03C3 ₁₆	Port P7 Direction Register	PD7	00 ₁₆	
03C4 ₁₆	Port P8 Register	P8	XX ₁₆	
03C5 ₁₆	Port P9 Register	P9	XX ₁₆	
03C6 ₁₆	Port P8 Direction Register	PD8	00X0 0000 ₂	
03C7 ₁₆	Port P9 Direction Register	PD9	00 ₁₆	
03C8 ₁₆	Port P10 Register	P10	XX ₁₆	
03C9 ₁₆				
03CA ₁₆	Port P10 Direction Register	PD10	00 ₁₆	
03CB ₁₆				
03CC ₁₆				
03CD ₁₆				
03CE ₁₆				
03CF ₁₆				

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1.  Set address spaces 03CB₁₆, 03CE₁₆ and 03CF₁₆ to "FF₁₆" in the 100-pin package.
2.  Address spaces 03A0₁₆, 03A1₁₆, 03B9₁₆, 03BC₁₆, 03BD₁₆, 03C9₁₆, 03CC₁₆ and 03CD₁₆ are not provided in the 100-pin package.

<100-pin package>

Address	Register	Symbol	Value after RESET	
03D0 ₁₆				(Note 3)
03D1 ₁₆				
03D2 ₁₆				(Note 1)
03D3 ₁₆				
03D4 ₁₆				
03D5 ₁₆				
03D6 ₁₆				
03D7 ₁₆				
03D8 ₁₆				
03D9 ₁₆				
03DA ₁₆	Pull-up Control Register 2	PUR2	00 ₁₆	
03DB ₁₆	Pull-up Control Register 3	PUR3	00 ₁₆	
03DC ₁₆				(Note 2)
03DD ₁₆				
03DE ₁₆				
03DF ₁₆				
03E0 ₁₆	Port P0 Register	P0	XX ₁₆	
03E1 ₁₆	Port P1 Register	P1	XX ₁₆	
03E2 ₁₆	Port P0 Direction Register	PD0	00 ₁₆	
03E3 ₁₆	Port P1 Direction Register	PD1	00 ₁₆	
03E4 ₁₆	Port P2 Register	P2	XX ₁₆	
03E5 ₁₆	Port P3 Register	P3	XX ₁₆	
03E6 ₁₆	Port P2 Direction Register	PD2	00 ₁₆	
03E7 ₁₆	Port P3 Direction Register	PD3	00 ₁₆	
03E8 ₁₆	Port P4 Register	P4	XX ₁₆	
03E9 ₁₆	Port P5 Register	P5	XX ₁₆	
03EA ₁₆	Port P4 Direction Register	PD4	00 ₁₆	
03EB ₁₆	Port P5 Direction Register	PD5	00 ₁₆	
03EC ₁₆				
03ED ₁₆				
03EE ₁₆				
03EF ₁₆				
03F0 ₁₆	Pull-Up Control Register 0	PUR0	00 ₁₆	
03F1 ₁₆	Pull-Up Control Register 1	PUR1	XXXX 0000 ₂	
03F2 ₁₆				
03F3 ₁₆				
03F4 ₁₆				
03F5 ₁₆				
03F6 ₁₆				
03F7 ₁₆				
03F8 ₁₆				
03F9 ₁₆				
03FA ₁₆				
03FB ₁₆				
03FC ₁₆				
03FD ₁₆				
03FE ₁₆				
03FF ₁₆	Port Control Register	PCR	XXXX XXX0 ₂	

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1.  Set address spaces 03D2₁₆ and 03D3₁₆ to "FF₁₆" in the 100-pin package.
2.  Set address spaces 03DC₁₆ to "00₁₆" in the 100-pin package.
3.  Address spaces 03D0₁₆ and 03D1₁₆ are not provided in the 100-pin package.

5. Electrical Characteristics

5.1 Electrical Characteristics (M32C/83)

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Value	Unit
V _{CC}	Supply Voltage	V _{CC} =AV _{CC}	-0.3 to 6.0	V
AV _{CC}	Analog Supply Voltage	V _{CC} =AV _{CC}	-0.3 to 6.0	V
V _I	Input Voltage	RESET, CNV _{SS} , BYTE, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , V _{REF} , X _{IN}	-0.3 to V _{CC} +0.3	V
		P7 ₀ , P7 ₁	-0.3 to 6.0	V
V _O	Output Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{OUT}	-0.3 to V _{CC} +0.3	V
P _d	Power Dissipation	T _{opr} =25° C	500	mW
T _{opr}	Operating Ambient Temperature		-20 to 85	° C
T _{stg}	Storage Temperature		-65 to 150	° C

NOTES:

1. P11 to P15 are provided in the 144-pin package.

Table 5.2 Recommended Operating Conditions ($V_{CC} = 3.0V$ to $5.5V$ at $T_{opr} = -20$ to $85^{\circ}C$)

Symbol	Parameter		Standard			Unit
			Min	Typ	Max	
V_{CC}	Supply Voltage (Through VDC)		3.0	5.0	5.5	V
	Supply Voltage (Not through VDC)		3.0	3.3	3.6	V
AV_{CC}	Analog Supply Voltage			V_{CC}		V
V_{SS}	Supply Voltage			0		V
AV_{SS}	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾ , X_{IN} , $\overline{RESET}$, CNV_{SS} , BYTE	0.8 V_{CC}		V_{CC}	V
		P70, P71	0.8 V_{CC}		6.0	
		P00-P07, P10-P17 (in single-chip mode)	0.8 V_{CC}		V_{CC}	V
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0.5 V_{CC}		V_{CC}	V
V_{IL}	Input Low ("L") Voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾ , X_{IN} , $\overline{RESET}$, CNV_{SS} , BYTE	0		0.2 V_{CC}	V
		P00-P07, P10-P17 (in single-chip mode)	0		0.2 V_{CC}	V
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0		0.16 V_{CC}	V
$I_{OH(peak)}$	Peak Output High ("H") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			5.0	mA
$f(X_{IN})$	Main Clock Input Frequency	Through VDC	$V_{CC}=4.2$ to $5.5V$	0	32	MHz
			$V_{CC}=3.0$ to $4.3V$	0	20	MHz
		Not through VDC	$V_{CC}=3.0$ to 3.6	0	20	MHz
$f(X_{CIN})$	Sub Clock Oscillation Frequency			32.768	50	kHz

NOTES:

- Typical values when average output current is 100ms.
- Total $I_{OL(peak)}$ for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80mA or less.
Total $I_{OH(peak)}$ for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be -80mA or less.
Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80mA or less.
Total $I_{OH(peak)}$ for P3, P4, P5, P6, P72 to P77, P80 to P84, P12 and P13 must be -80mA or less.
- V_{IH} and V_{IL} reference for P87 applies when P87 is used as a programmable input port.
It does not apply to P87 used as X_{CIN} .
- P11 to P15 are provided in the 144-pin package only.

**Table 5.3 Electrical Characteristics (V_{CC}=4.2 to 5.5V, V_{SS}=0V
at T_{opr}= -20 to 85°C, f(X_{IN})=32MHz unless otherwise specified)**

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-5mA	V _{CC} - 2.0			V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-200μA	V _{CC} - 0.3			
		X _{OUT}	I _{OH} =-1mA	3.0			V
		X _{COU}	No load applied		3.3		V
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =5mA			2.0	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =200μA			0.45	V
		X _{OUT}	I _{OL} =1mA			2.0	V
		X _{COU}	No load applied		0		V
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =5V			5.0	μA
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	30	50	167	kΩ
R _{FXIN}	Feedback Resistance	X _{IN}			1.5		MΩ
R _{FXCIN}	Feedback Resistance	X _{CIN}			10		MΩ
V _{RAM}	RAM Standby Voltage	Through VDC		2.5			V
I _{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(X _{IN})=32 MHz, square wave, no division		40	54	mA
			f(X _{CIN})=32 kHz, with a wait state, T _{opr} =25° C		470		μA
			T _{opr} =25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

**Table 5.4 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5V, V_{SS} = AV_{SS} = 0V
at Topr = -20 to 85°C, f(X_{IN}) = 32MHz unless otherwise specified)**

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution	V _{REF} =V _{CC}			10	Bits
INL	Integral Nonlinearity Error	V _{REF} =V _{CC} =5V			±3	LSB
						LSB
					±7	LSB
						LSB
DNL	Differential Nonlinearity Error				±1	LSB
-	Offset Error				±3	LSB
-	Gain Error				±3	LSB
R _{LADDER}	Resistor Ladder	V _{REF} =V _{CC}	8		40	kΩ
t _{CONV}	10-bit Conversion Time		2.1			μs
t _{CONV}	8-bit Conversion Time		1.8			μs
t _{SAMP}	Sample Time		0.2			μs
V _{REF}	Reference Voltage		2		V _{CC}	V
V _{IA}	Analog Input Voltage		0		V _{REF}	V

NOTES:

1. Divide f(X_{IN}), if exceeding 16 MHz, to keep φ_{AD} frequency at 16 MHz or less.

**Table 5.5 D/A Conversion Characteristics (V_{CC} = V_{REF} = 4.2 to 5.5V, V_{SS} = AV_{SS} = 0V
at Topr = -20 to 85°C, f(X_{IN}) = 32MHz unless otherwise specified)**

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	kΩ
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:

1. Measurement results when using one D/A converter. The DAI register (i=0, 1) of the D/A converter not being used is set to "0016". The resistor ladder in the A/D converter is excluded. I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 5.6 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:

1. V_{CC}= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at Topr= 0 to 60° C, unless otherwise specified

Timing Requirements (V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at T_{opr} = -20 to 85°C unless otherwise specified)**Table 5.7 External Clock Input**

Symbol	Parameter	Standard		Unit
		Min	Max	
t _c	External Clock Input Cycle Time	33		ns
t _{w(H)}	External Clock Input High ("H") Pulse Width	13		ns
t _{w(L)}	External Clock Input Low ("L") Pulse Width	13		ns
t _r	External Clock Rise Time		5	ns
t _f	External Clock Fall Time		5	ns

Table 5.8 Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{ac1(RD-DB)}	Data Input Access Time (RD standard, with no wait state)		(Note 1)	ns
t _{ac1(AD-DB)}	Data Input Access Time (AD standard, CS standard, with no wait state)		(Note 1)	ns
t _{ac2(RD-DB)}	Data Input Access Time (RD standard, with a wait state)		(Note 1)	ns
t _{ac2(AD-DB)}	Data Input Access Time (AD standard, CS standard, with a wait state)		(Note 1)	ns
t _{ac3(RD-DB)}	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t _{ac3(AD-DB)}	Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t _{ac4(RAS-DB)}	Data Input Access Time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
t _{ac4(CAS-DB)}	Data Input Access Time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
t _{ac4(CAD-DB)}	Data Input Access Time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
t _{SU(DB-BCLK)}	Data Input Setup Time	26		ns
t _{SU(RDY-BCLK)}	RDY Input Setup Time	26		ns
t _{SU(HOLD-BCLK)}	HOLD Input Setup Time	30		ns
t _{h(RD-DB)}	Data Input Hold Time	0		ns
t _{h(CAS-DB)}	Data Input Hold Time	0		ns
t _{h(BCLK-RDY)}	RDY Input Hold Time	0		ns
t _{h(BCLK-HOLD)}	HOLD Input Hold Time	0		ns
t _{d(BCLK-HLDA)}	HLDA Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency. Insert a wait state or lower the operation frequency, f_(BCLK), if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f_{(BCLK)}} - 35 \quad [\text{ns}]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ with 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

Timing Requirements(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.9 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA _{IN} Input Cycle Time	100		ns
tw(TAH)	TA _{IN} Input High ("H") Pulse Width	40		ns
tw(TAL)	TA _{IN} Input Low ("L") Pulse Width	40		ns

Table 5.10 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA _{IN} Input Cycle Time	400		ns
tw(TAH)	TA _{IN} Input High ("H") Pulse Width	200		ns
tw(TAL)	TA _{IN} Input Low ("L") Pulse Width	200		ns

Table 5.11 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA _{IN} Input Cycle Time	200		ns
tw(TAH)	TA _{IN} Input High ("H") Pulse Width	100		ns
tw(TAL)	TA _{IN} Input Low ("L") Pulse Width	100		ns

Table 5.12 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TA _{IN} Input High ("H") Pulse Width	100		ns
tw(TAL)	TA _{IN} Input Low ("L") Pulse Width	100		ns

Table 5.13 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TA _{IOU} Input Cycle Time	2000		ns
tw(UPH)	TA _{IOU} Input High ("H") Pulse Width	1000		ns
tw(UPL)	TA _{IOU} Input Low ("L") Pulse Width	1000		ns
tsu(UP-TIN)	TA _{IOU} Input Setup Time	400		ns
th(TIN-UP)	TA _{IOU} Input Hold Time	400		ns

Timing Requirements(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at T_{opr} = -20 to 85°C unless otherwise specified)**Table 5.14 Timer B Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{c(TB)}	TB _{IN} Input Cycle Time (counted on one edge)	100		ns
t _{w(TBH)}	TB _{IN} Input High ("H") Pulse Width (counted on one edge)	40		ns
t _{w(TBL)}	TB _{IN} Input Low ("L") Pulse Width (counted on one edge)	40		ns
t _{c(TB)}	TB _{IN} Input Cycle Time (counted on both edges)	200		ns
t _{w(TBH)}	TB _{IN} Input High ("H") Pulse Width (counted on both edges)	80		ns
t _{w(TBL)}	TB _{IN} Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 5.15 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{c(TB)}	TB _{IN} Input Cycle Time	400		ns
t _{w(TBH)}	TB _{IN} Input High ("H") Pulse Width	200		ns
t _{w(TBL)}	TB _{IN} Input Low ("L") Pulse Width	200		ns

Table 5.16 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{c(TB)}	TB _{IN} Input Cycle Time	400		ns
t _{w(TBH)}	TB _{IN} Input High ("H") Pulse Width	200		ns
t _{w(TBL)}	TB _{IN} Input Low ("L") Pulse Width	200		ns

Table 5.17 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{c(AD)}	AD _{TRG} Input Cycle Time (required for re-trigger)	1000		ns
t _{w(ADL)}	AD _{TRG} Input Low ("L") Pulse Width	125		ns

Table 5.18 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{c(CLK)}	CLK _i Input Cycle Time	200		ns
t _{w(CLKH)}	CLK _i Input High ("H") Pulse Width	100		ns
t _{w(CLKL)}	CLK _i Input Low ("L") Pulse Width	100		ns
t _{d(CQ)}	TxD _i Output Delay Time		80	ns
t _{h(CQ)}	TxD _i Hold Time	0		ns
t _{su(DQ)}	RxD _i Input Set Up Time	30		ns
t _{h(CQ)}	RxD _i Input Hold Time	90		ns

Table 5.19 External Interrupt INT_i Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{w(INH)}	INT _i Input High ("H") Pulse Width	250		ns
t _{w(INL)}	INT _i Input Low ("L") Pulse Width	250		ns

Switching Characteristics(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.20 Memory Expansion Mode and Microprocessor Mode (with No Wait State)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard)		0		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		0		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		-2		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-3		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
tw(WR)	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$td(DB - WR) = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$th(WR - DB) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$

Switching Characteristics(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.21 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard)		0		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		0		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		-2		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-3		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
tw(WR)	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$td(DB - WR) = \frac{10^9 \times n}{f(BCLK)} - 20 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states and } n=3 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=5 \text{ with 3 wait states})$$

Switching Characteristics(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at T_{opr} = –20 to 85°C unless otherwise specified)**Table 5.22 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		-3		ns
th(RD-AD)	Address Output Hold Time (RD standard)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-AD)	RD Signal Output Hold Time		-5		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		-3		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
tdz(RD-AD)	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB - WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD - ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

Switching Characteristics(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.23 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting the DRAM Space)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-RAD)	Row Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-RAD)	Row Address Output Hold Time (BCLK standard)		-3		ns
td(BCLK-CAD)	Column Address Output Delay Time			18	ns
th(BCLK-CAD)	Column Address Output Hold Time (BCLK standard)		-3		ns
th(RAS-RAD)	Row Address Output Hold Time after RAS Output		(Note 1)		ns
td(BCLK-RAS)	RAS Output Delay Time (BCLK standard)			18	ns
th(BCLK-RAS)	RAS Output Hold Time (BCLK standard)		-3		ns
t _{RP}	RAS High ("H") Hold Time		(Note 1)		ns
td(BCLK-CAS)	CAS Output Delay Time (BCLK standard)			18	ns
th(BCLK-CAS)	CAS Output Hold Time (BCLK standard)		-3		ns
td(BCLK-DW)	DW Output Delay Time (BCLK standard)			18	ns
th(BCLK-DW)	DW Output Hold Time (BCLK standard)		-5		ns
tsu(DB-CAS)	CAS Output Setup Time after DB Output		(Note 1)		ns
th(BCLK-DB)	DB Signal Output Hold Time (BCLK standard)		-7		ns
tsu(CAS-RAS)	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

- Values can be obtained from the following equation, according to BCLK frequency.

$$th(RAS - RAD) = \frac{10^9}{f(BCLK) \times 2} - 13 \quad [ns]$$

$$t_{RP} = \frac{10^9 \times 3}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$tsu(DB - CAS) = \frac{10^9}{f(BCLK)} - 20 \quad [ns]$$

$$tsu(CAS - RAS) = \frac{10^9}{f(BCLK) \times 2} - 13 \quad [ns]$$

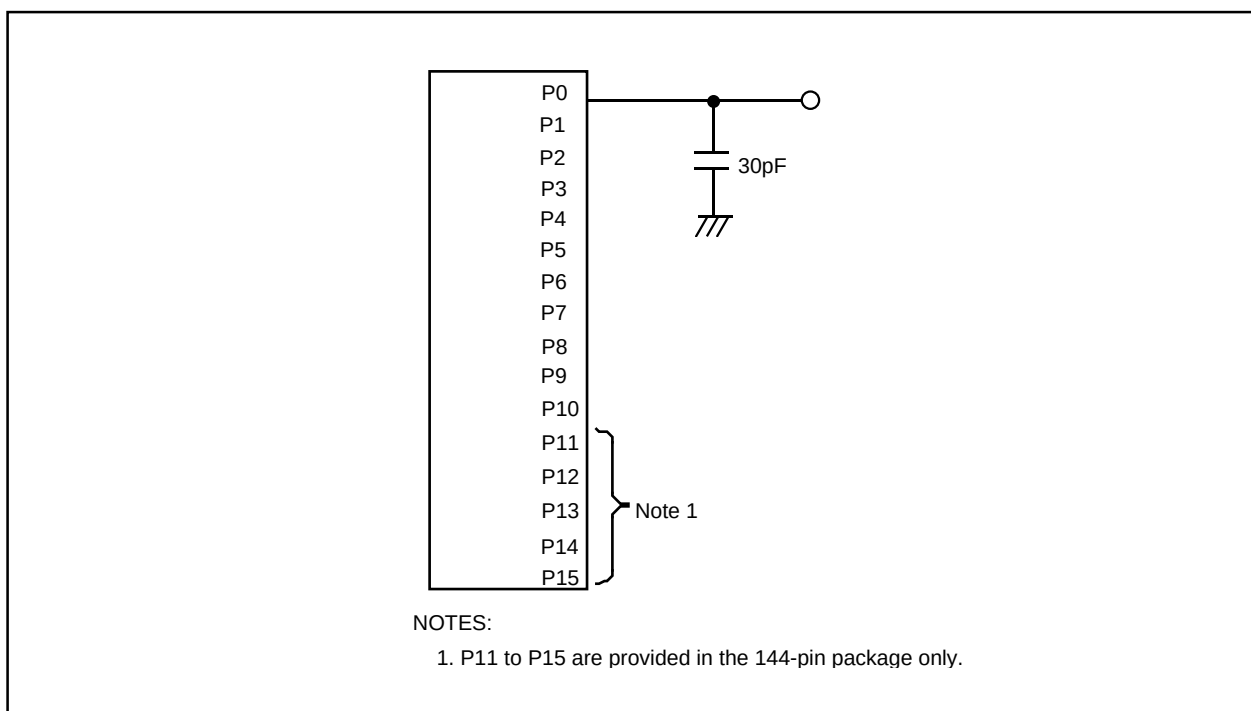
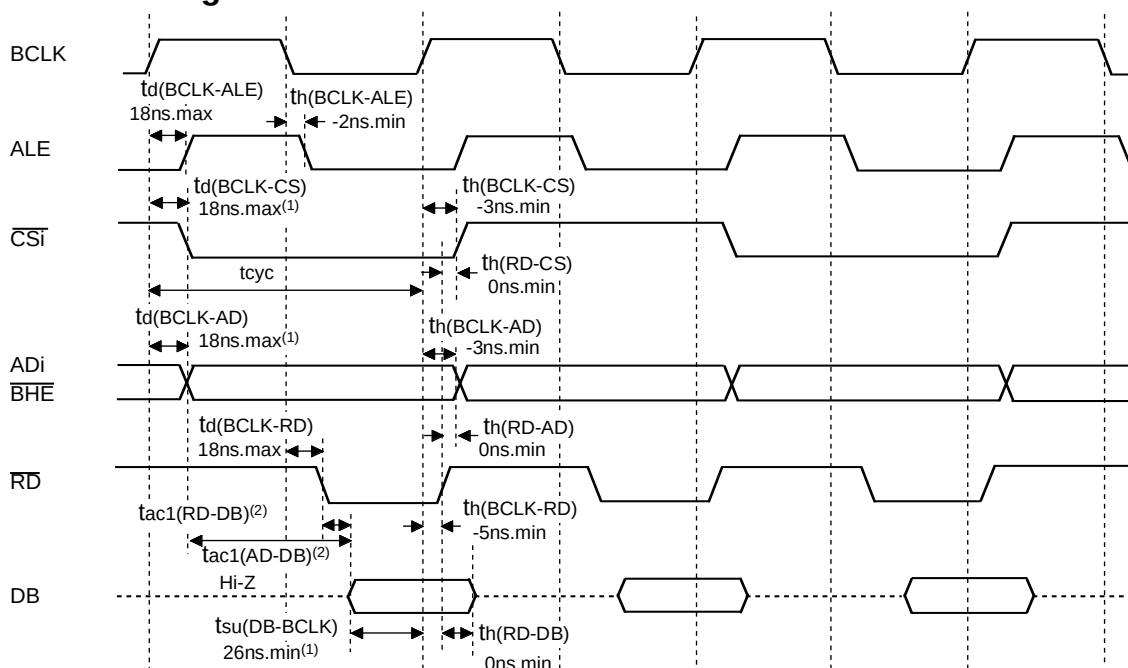


Figure 5.1 P0 to P15 Measurement Circuit

V_{CC}=5V

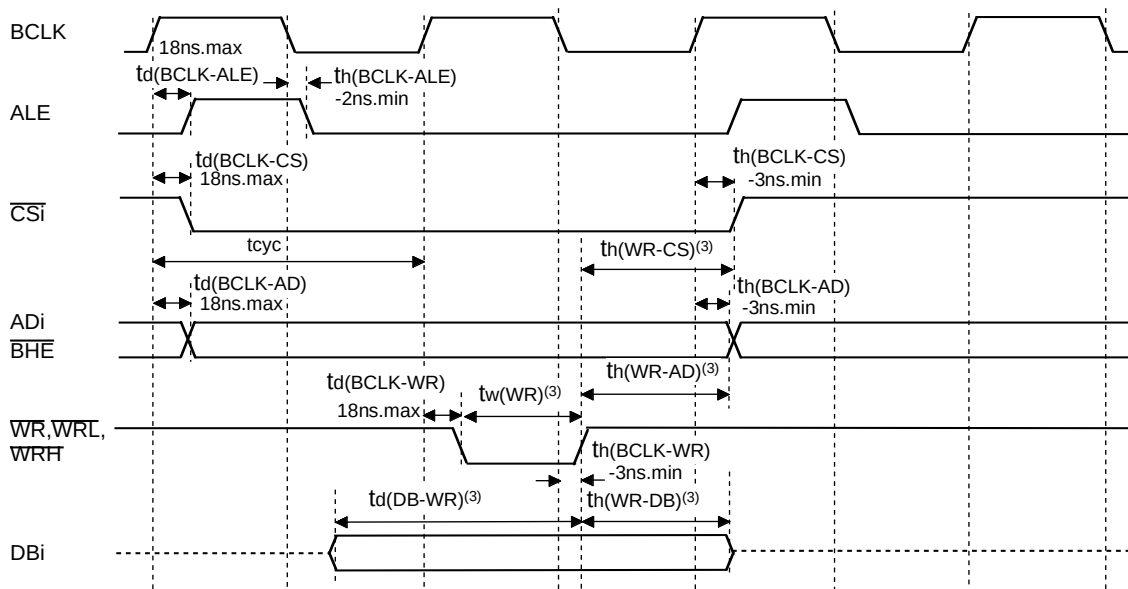
Memory Expansion Mode and Microprocessor Mode (with no wait state) Read Timing



NOTES:

- Values guaranteed only when the microcomputer is used independently.
A maximum of 35ns is guaranteed for $t_d(\text{BCLK-AD}) + t_{su}(\text{DB-BCLK})$.
- Varies with operation frequency:
 $t_{ac1}(\text{RD-DB}) = (t_{cyc}/2 - 35)\text{ns.max}$
 $t_{ac1}(\text{AD-DB}) = (t_{cyc} - 35)\text{ns.max}$

Write Timing (written in 2 cycles with no wait state)



NOTES:

- Varies with operation frequency:
 $t_d(\text{DB-WR}) = (t_{cyc} - 20)\text{ns.min}$
 $t_h(\text{WR-DB}) = (t_{cyc}/2 - 10)\text{ns.min}$
 $t_h(\text{WR-AD}) = (t_{cyc}/2 - 10)\text{ns.min}$
 $t_h(\text{WR-CS}) = (t_{cyc}/2 - 10)\text{ns.min}$
 $t_w(\text{WR}) = (t_{cyc}/2 - 15)\text{ns.min}$

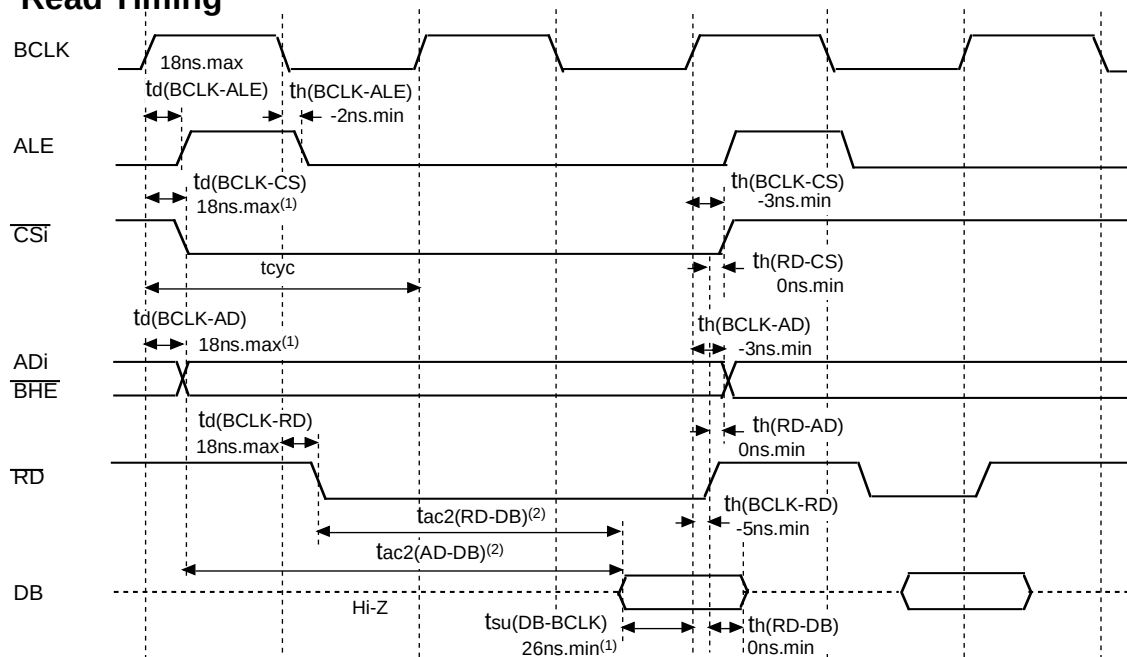
Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

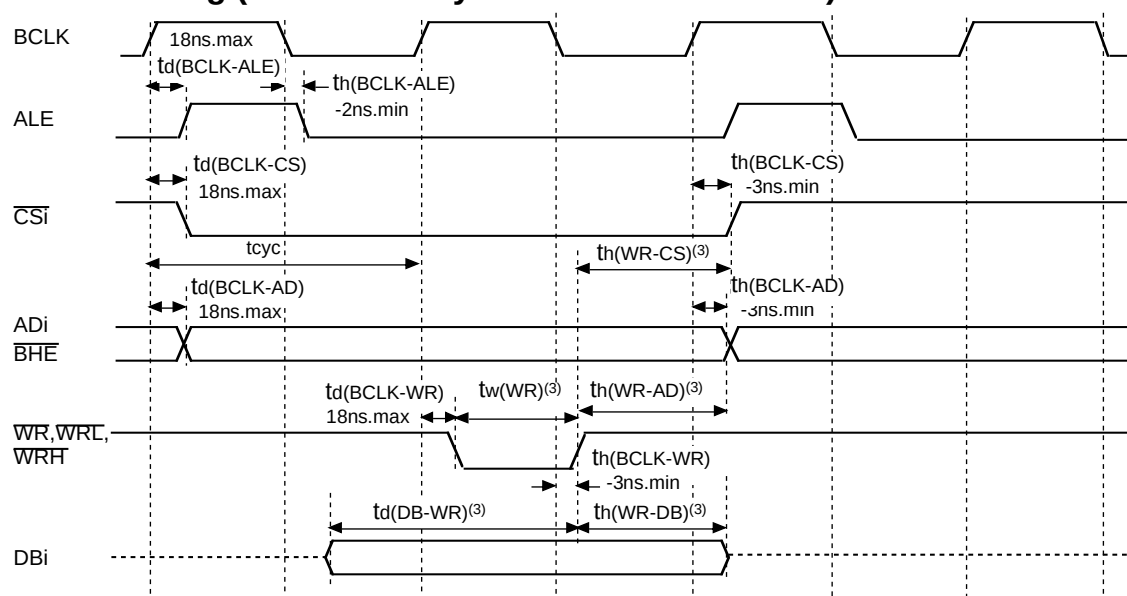
Figure 5.2 V_{CC}=5V Timing Diagram (1)

V_{CC}=5V

Memory Expansion Mode and Microprocessor Mode (with a wait state) Read Timing



Write Timing (written in 2 cycles with no wait state)



Measurement conditions

- V_{CC}=4.2 to 5.5V
- Input high and low voltage:
V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage:
V_{OH}=2.0V, V_{OL}=0.8V

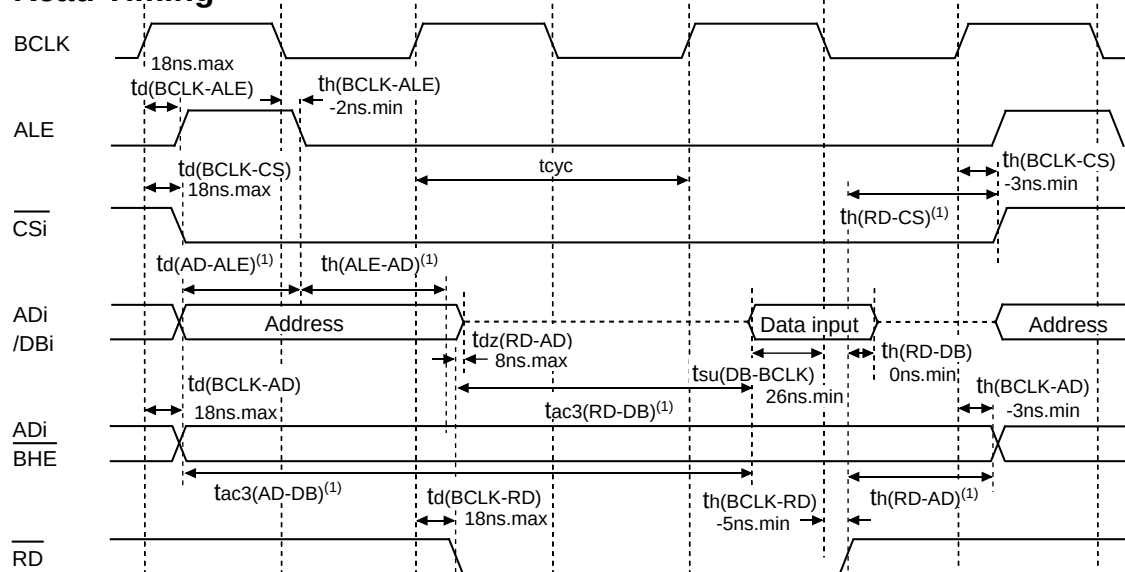
Figure 5.3 V_{CC}=5V Timing Diagram (2)

V_{CC}=5V

Memory Expansion Mode and Microprocessor Mode

(with a wait state, when accessing an external memory and using the multiplexed bus)

Read Timing



NOTES:

1. Varies with operation frequency:

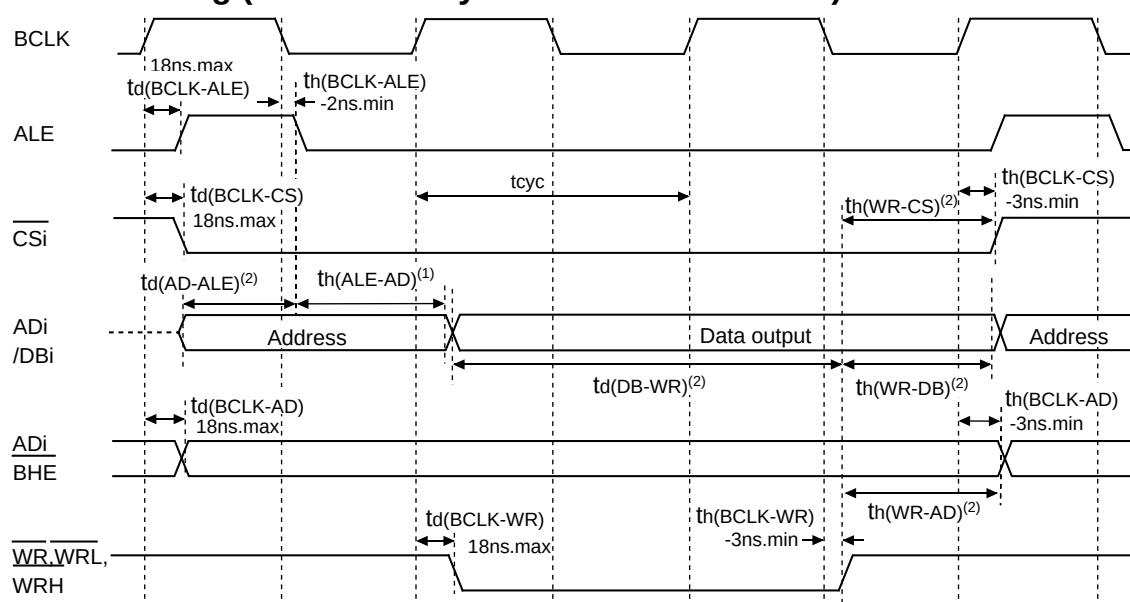
$$t_d(\text{AD-ALE}) = (\text{tcyc}/2 - 20)\text{ns.min}$$

$$t_h(\text{ALE-AD}) = (\text{tcyc}/2 - 10)\text{ns.min}, t_h(\text{RD-AD}) = (\text{tcyc}/2 - 10)\text{ns.min}, t_h(\text{RD-CS}) = (\text{tcyc}/2 - 10)\text{ns.min}$$

$$t_{ac3}(\text{RD-DB}) = (\text{tcyc}/2 \times m - 35)\text{ns.max} \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3}(\text{AD-DB}) = (\text{tcyc}/2 \times n - 35)\text{ns.max} \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

Write Timing (written in 2 cycles with no wait state)



NOTES:

2. Varies with operation frequency:

$$t_d(\text{AD-ALE}) = (\text{tcyc}/2 - 20)\text{ns.min}$$

$$t_h(\text{ALE-AD}) = (\text{tcyc}/2 - 10)\text{ns.min}, t_h(\text{WR-AD}) = (\text{tcyc}/2 - 10)\text{ns.min}$$

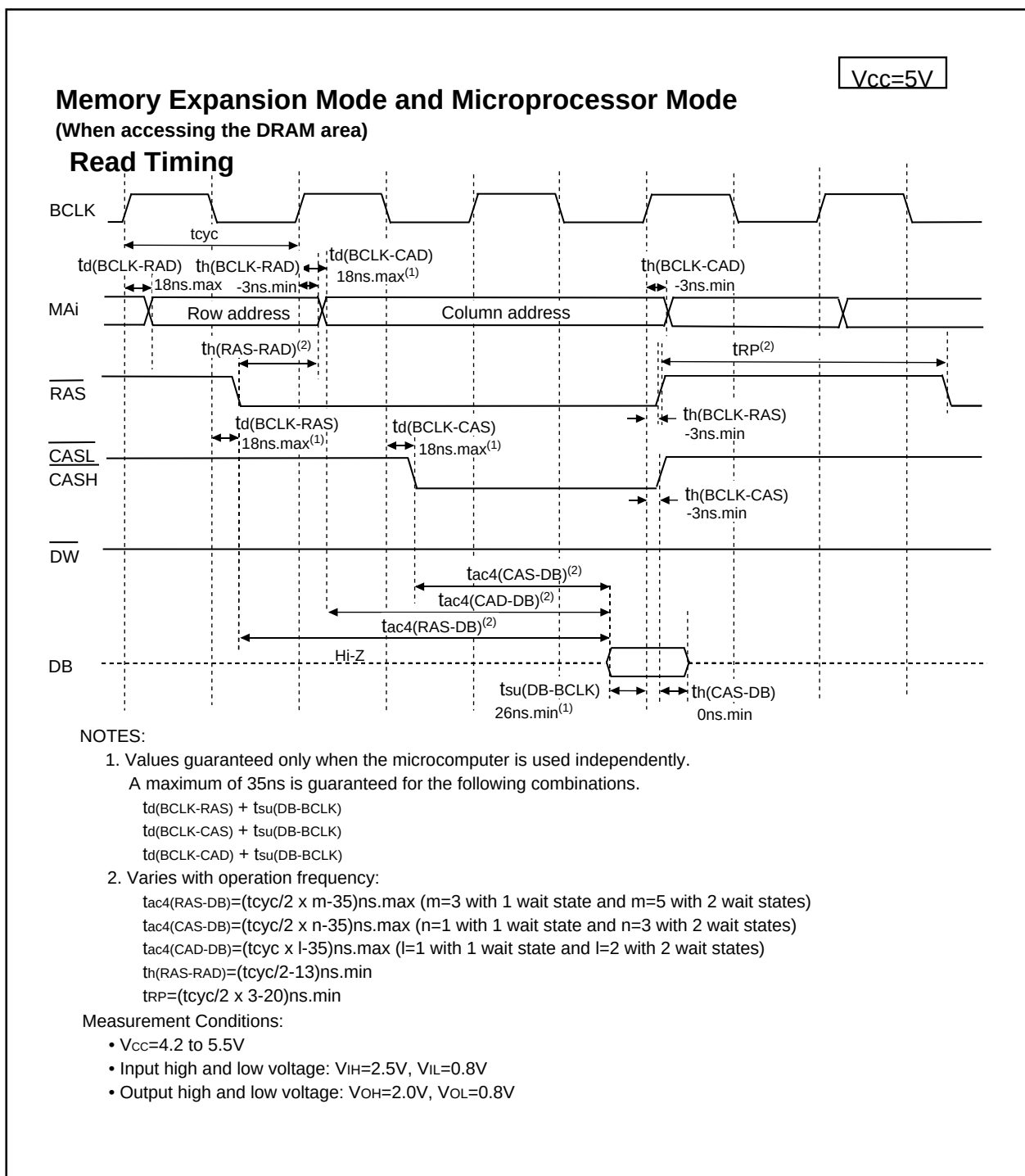
$$t_h(\text{WR-CS}) = (\text{tcyc}/2 - 10)\text{ns.min}, t_h(\text{WR-DB}) = (\text{tcyc}/2 - 10)\text{ns.min}$$

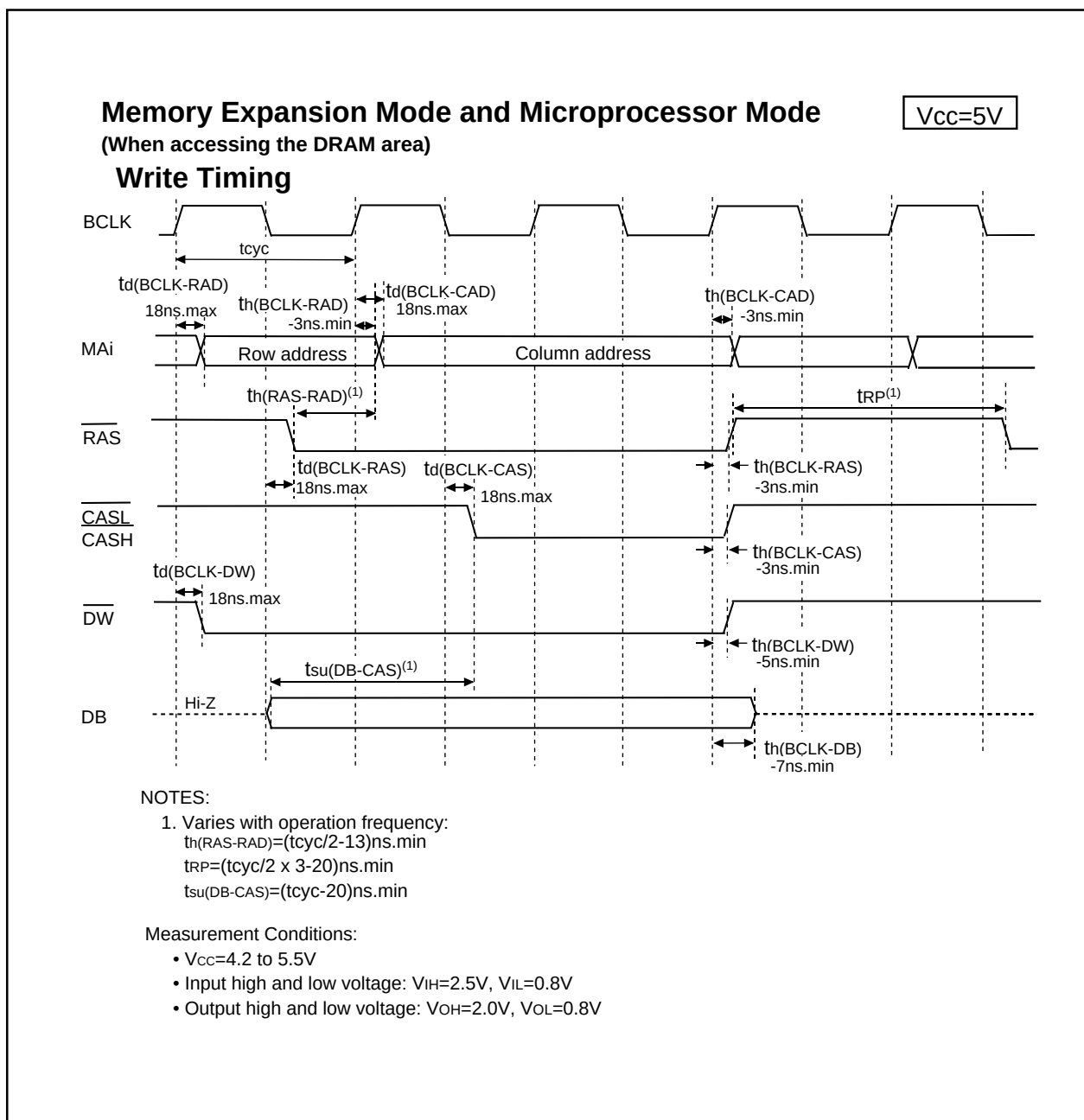
$$t_d(\text{DB-WR}) = (\text{tcyc}/2 \times m - 25)\text{ns.min}$$

Measurement Conditions:

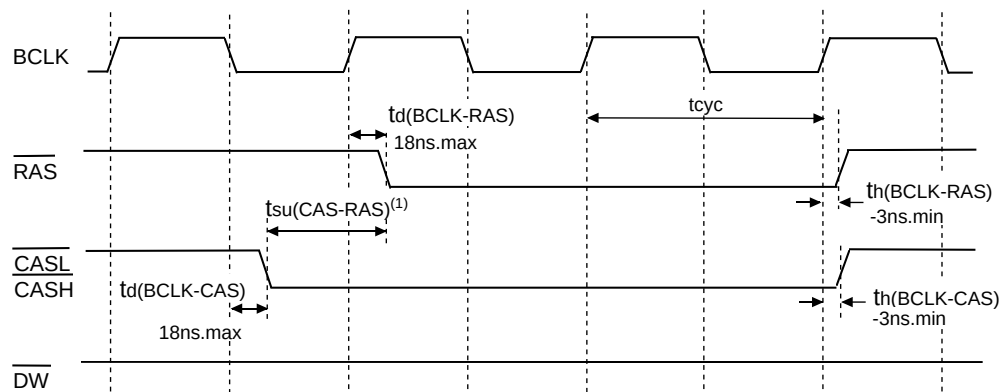
- V_{CC}=4.2 to 5.5V
- Input high and low voltage:
V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage:
V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.4 V_{CC}=5V Timing Diagram (3)

Figure 5.5 V_{CC}=5V Timing Diagram (4)

Figure 5.6 V_{CC}=5V Timing Diagram (5)

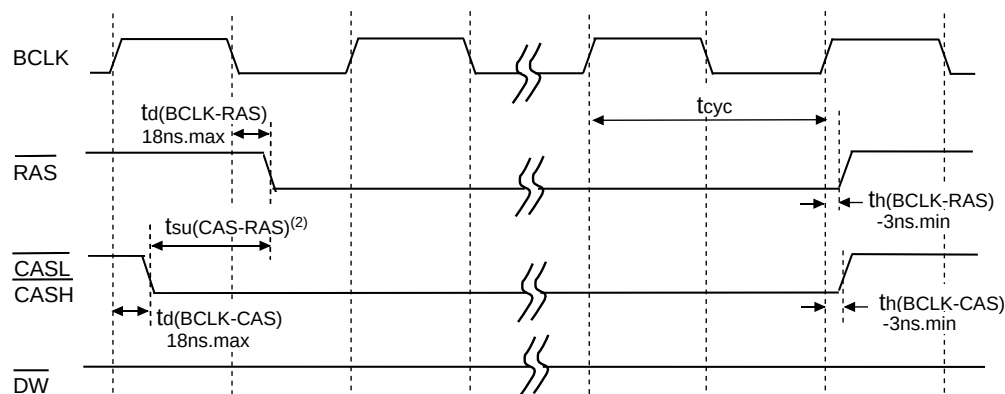
Memory Expansion Mode and Microprocessor Mode Refresh Timing (CAS-before-RAS refresh)

V_{CC}=5V

NOTES :

1. Varies with operation frequency:
 $t_{su}(CAS-RAS) = (t_{cy}/2 - 13)ns.min$

Refresh Timing (Self-refresh)



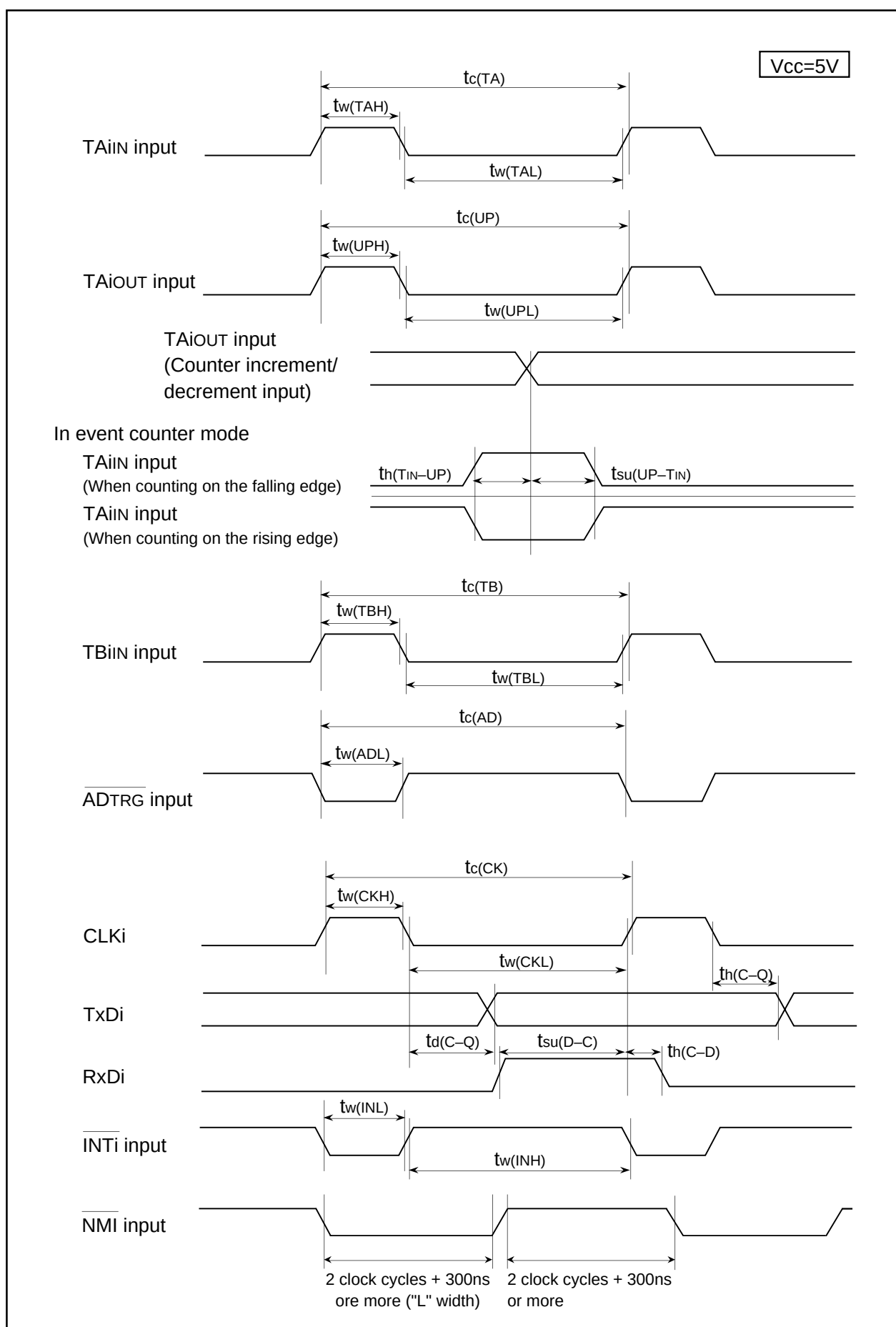
NOTES:

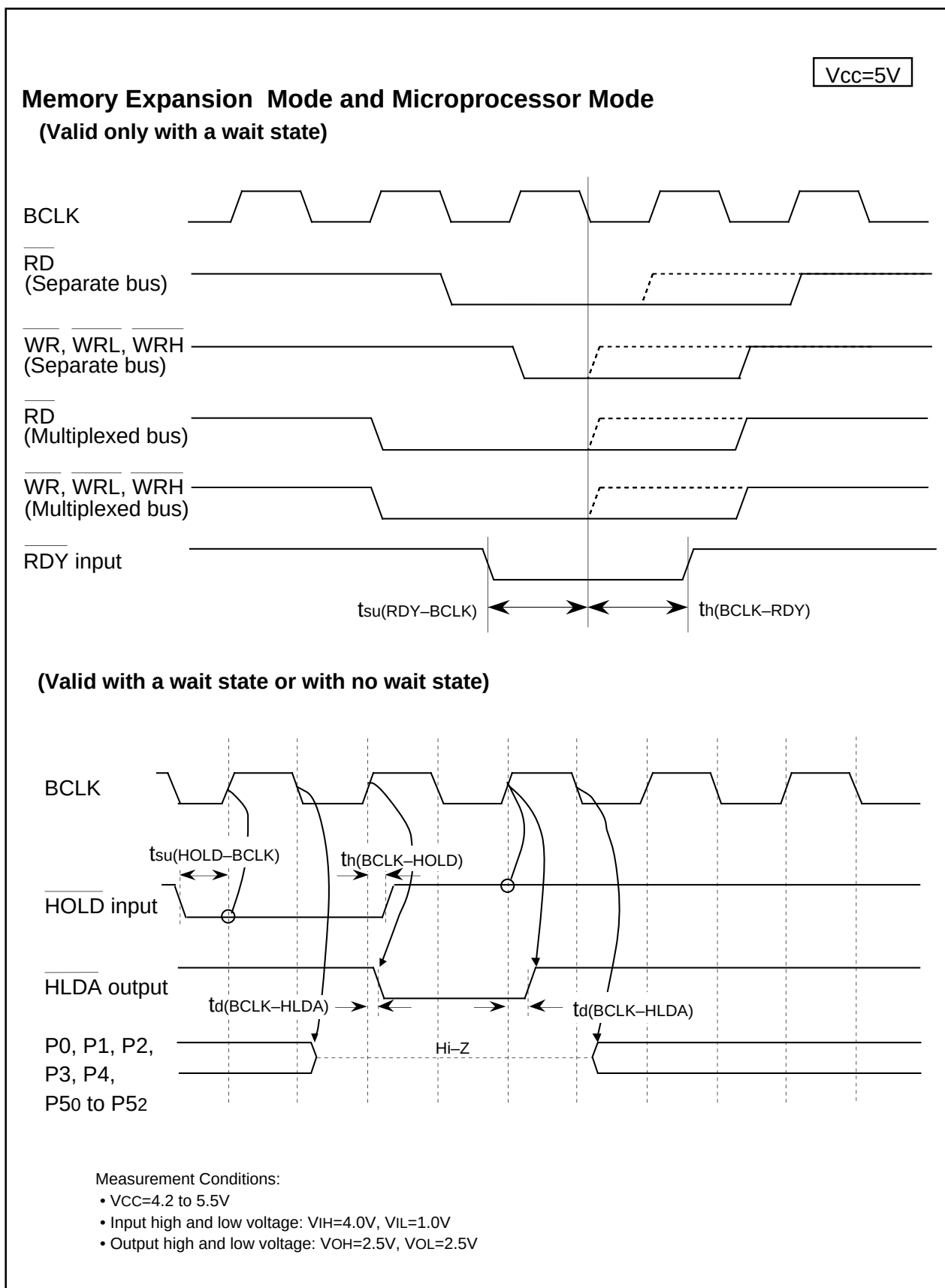
2. Varies with operation frequency:
 $t_{su}(CAS-RAS) = (t_{cy}/2 - 13)ns.min$

Measurement Conditions:

- V_{CC}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

Figure 5.7 V_{CC}=5V Timing Diagram (6)

Figure 5.8 $V_{CC}=5V$ Timing Diagram (7)

Figure 5.9 $V_{CC}=5V$ Timing Diagram (8)

**Table 5.24 Electrical Characteristics (V_{CC}=3.0 to 3.6V, V_{SS}=0V at T_{opr} = –20 to 85°C,
f(X_{IN})=20MHz unless otherwise specified)**

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-1mA	V _{CC} -0.6			V
		X _{OUT}	I _{OH} =-0.1mA	2.7			V
		X _{COUT}	No load applied		3.3		V
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =1mA			0.5	V
		X _{OUT}	I _{OL} =0.1mA			0.5	V
		X _{COUT}	No load applied		0		V
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0 _{IN} -TA4 _{IN} , TB0 _{IN} -TB5 _{IN} , INT0-INT5, AD _{TRG} , CTS0-CTS4, CLK0-CLK4, TA0 _{OUT} -TA4 _{OUT} , NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =3V			4.0	μA
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-4.0	μA
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	66	120	500	kΩ
R _{fXIN}	Feedback Resistance	X _{IN}			3.0		MΩ
R _{fXCIN}	Feedback Resistance	X _{CIN}			20.0		MΩ
V _{RAM}	RAM Standby Voltage	Through VDC		2.5			V
		Not through VDC		2.0			V
I _{CC}	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(X _{IN})=20 MHz, square wave, no division		26	38	mA
			f(X _{CIN})=32 kHz, with a wait state, not through VDC, T _{opr} =25° C		5.0		μA
			f(X _{CIN})=32 kHz, with a wait state, through VDC, T _{opr} =25° C		340		μA
			T _{opr} =25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

**Table 5.25 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V
at T_{opr} = -20 to 85°C, f(X_{IN}) = 20MHz unless otherwise specified)**

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		V _{REF} =V _{CC}			10	Bits
INL	Integral Nonlinearity Error	No S&H function (8-bit)	V _{CC} =V _{REF} =3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H function (8-bit)				±1	LSB
-	Offset Error	No S&H function (8-bit)				±2	LSB
-	Gain Error	No S&H function (8-bit)				±2	LSB
R _{LADDER}	Resistor Ladder		V _{REF} =V _{CC}	8		40	kΩ
t _{CONV}	8-bit Conversion Time			4.9			μs
V _{REF}	Reference Voltage			3.0		V _{CC}	V
V _{IA}	Analog Input Voltage			0		V _{REF}	V

S&H: Sample and hold

NOTES:

1. Divide f(X_{IN}), if exceeding 10 MHz, to keep φ_{AD} frequency at 10 MHz or less.

**Table 5.26 D/A Conversion Characteristics (V_{CC} = V_{REF} = 3.0 to 3.6V, V_{SS} = AV_{SS} = 0V
at T_{opr} = -20 to 85°C, f(X_{IN}) = 20MHz unless otherwise specified)**

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{su}	Setup Time				3	μs
R _o	Output Resistance		4	10	20	kΩ
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTES:

1. Measurement results when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter not being used is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 5.27 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:

1. V_{CC}= 4.2 to 5.5V (through VDC), 3.0 to 3.6V (not through VDC) at T_{opr}= 0 to 60° C, unless otherwise specified

Timing Requirements (V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.28 External Clock Input**

Symbol	Parameter	Standard		Unit
		Min	Max	
t _c	External Clock Input Cycle Time	50		ns
t _{w(H)}	External Clock Input High ("H") Pulse Width	22		ns
t _{w(L)}	External Clock Input Low ("L") Pulse Width	22		ns
t _r	External Clock Rise Time		5	ns
t _f	External Clock Fall Time		5	ns

Table 5.29 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{ac1(RD-DB)}	Data Input Access Time (RD standard, with no wait state)		(Note 1)	ns
t _{ac1(AD-DB)}	Data Input Access Time (AD standard, CS standard, with no wait state)		(Note 1)	ns
t _{ac2(RD-DB)}	Data Input Access Time (RD standard, with a wait state)		(Note 1)	ns
t _{ac2(AD-DB)}	Data Input Access Time (AD standard, CS standard, with a wait state)		(Note 1)	ns
t _{ac3(RD-DB)}	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t _{ac3(AD-DB)}	Data Input Access Time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
t _{ac4(RAS-DB)}	Data Input Access Time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
t _{ac4(CAS-DB)}	Data Input Access Time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
t _{ac4(CAD-DB)}	Data Input Access Time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
t _{su(DB-BCLK)}	Data Input Setup Time	30		ns
t _{su(RDY-BCLK)}	RDY Input Setup Time	40		ns
t _{su(HOLD-BCLK)}	HOLD Input Setup Time	60		ns
t _{h(RD-DB)}	Data Input Hold Time	0		ns
t _{h(CAS-DB)}	Data Input Hold Time	0		ns
t _{h(BCLK-RDY)}	RDY Input Hold Time	0		ns
t _{h(BCLK-HOLD)}	HOLD Input Hold Time	0		ns
t _{d(BCLK-HLDA)}	HLDA Output Delay Time		25	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency. Insert a wait state or lower operation frequency, f_(BCLK), if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}]$$

$$t_{ac1(AD-DB)} = \frac{10^9}{f_{(BCLK)}} - 35 \quad [\text{ns}]$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$t_{ac3(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$t_{ac4(RAS-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$t_{ac4(CAS-DB)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ with 2 wait states})$$

$$t_{ac4(CAD-DB)} = \frac{10^9 \times l}{f_{(BCLK)}} - 35 \quad [\text{ns}] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

Timing Requirements**(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)****Table 5.30 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA _{IN} Input Cycle Time	100		ns
tw(TAH)	TA _{IN} Input High ("H") Pulse Width	40		ns
tw(TAL)	TA _{IN} Input Low ("L") Pulse Width	40		ns

Table 5.31 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA _{IN} Input Cycle Time	400		ns
tw(TAH)	TA _{IN} Input High ("H") Pulse Width	200		ns
tw(TAL)	TA _{IN} Input Low ("L") Pulse Width	200		ns

Table 5.32 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TA _{IN} Input Cycle Time	200		ns
tw(TAH)	TA _{IN} Input High ("H") Pulse Width	100		ns
tw(TAL)	TA _{IN} Input Low ("L") Pulse Width	100		ns

Table 5.33 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TA _{IN} Input High ("H") Pulse Width	100		ns
tw(TAL)	TA _{IN} Input Low ("L") Pulse Width	100		ns

Table 5.34 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TA _{IOUT} Input Cycle Time	2000		ns
tw(UPH)	TA _{IOUT} Input High ("H") Pulse Width	1000		ns
tw(UPL)	TA _{IOUT} Input Low ("L") Pulse Width	1000		ns
tsu(UP-TIN)	TA _{IOUT} Input Setup Time	400		ns
th(TIN-UP)	TA _{IOUT} Input Hold Time	400		ns

Timing Requirements(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.35 Timer B input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TB _{IN} Input Cycle Time (counted on one edge)	100		ns
t _{W(TBH)}	TB _{IN} Input High ("H") Pulse Width (counted on one edge)	40		ns
t _{W(TBL)}	TB _{IN} Input Low ("L") Pulse Width (counted on one edge)	40		ns
t _{C(TB)}	TB _{IN} Input Cycle Time (counted on both edges)	200		ns
t _{W(TBH)}	TB _{IN} Input High ("H") Pulse Width (counted on both edges)	80		ns
t _{W(TBL)}	TB _{IN} Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 5.36 Timer B input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TB _{IN} Input Cycle Time	400		ns
t _{W(TBH)}	TB _{IN} Input High ("H") Pulse Width	200		ns
t _{W(TBL)}	TB _{IN} Input Low ("L") Pulse Width	200		ns

Table 5.37 Timer B input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(TB)}	TB _{IN} Input Cycle Time	400		ns
t _{W(TBH)}	TB _{IN} Input High ("H") Pulse Width	200		ns
t _{W(TBL)}	TB _{IN} Input Low ("L") Pulse Width	200		ns

Table 5.38 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(AD)}	AD _{TRG} Input High ("H") Pulse Width (required for re-trigger)	1000		ns
t _{W(ADL)}	AD _{TRG} Input Low ("L") Pulse Width	125		ns

Table 5.39 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{C(CLK)}	CLK _i Input Cycle Time	200		ns
t _{W(CLKH)}	CLK _i Input High ("H") Pulse Width	100		ns
t _{W(CLKL)}	CLK _i Input Low ("L") Pulse Width	100		ns
t _{d(C-Q)}	TxD _i Output Delay Time		80	ns
t _{h(C-Q)}	TxD _i Hold Time	0		ns
t _{su(D-Q)}	RxD _i Input Set Up Time	30		ns
t _{h(C-Q)}	RxD _i Input Hold Time	90		ns

Table 5.40 External Interrupt INT_i input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _{W(INH)}	INT _i Input High ("H") Pulse Width	250		ns
t _{W(INL)}	INT _i Input Low ("L") Pulse Width	250		ns

Switching Characteristics(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C, unless otherwise specified)**Table 5.41 Memory Expansion Mode and Microprocessor Mode (with No Wait State)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		0		ns
th(RD-AD)	Address Output Hold Time (RD standard)		0		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		0		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		-2		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-3		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
tw(WR)	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations according to the BCLK frequency.

$$td(DB - WR) = \frac{10^9}{f_{(BCLK)}} - 20 \quad [ns]$$

$$th(WR - DB) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$

Switching Characteristics(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.42 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		0		ns
th(RD-AD)	Address Output Hold Time (RD standard)		0		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		0		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time		-2		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-3		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
tw(WR)	WR Output Width		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$td(DB - WR) = \frac{10^9 \times n}{f_{(BCLK)}} - 20 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states and } n=3 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=5 \text{ with 3 wait states})$$

Switching Characteristics(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.43 Memory Expansion Mode and Microprocessor Mode****(With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		0		ns
th(RD-AD)	Address Output Hold Time (RD standard)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-select Signal Output Hold Time (BCLK standard)		0		ns
th(RD-CS)	Chip-select Signal Output Hold Time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-AD)	RD Signal Output Hold Time		-3		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(DB-WR)	Data Output Delay Time (WR standard)		(Note 1)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 1)		ns
tdz(RD-AD)	Address Output High-Impedance Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$td(DB - WR) = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$td(AD - ALE) = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$th(ALE - AD) = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

Switching Characteristics(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)**Table 5.44 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting the DRAM Area)**

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min	Max	
td(BCLK-RAD)	Row Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-RAD)	Row Address Output Hold Time (BCLK standard)		0		ns
td(BCLK-CAD)	Column Address Output Delay Time			18	ns
th(BCLK-CAD)	Column Address Output Hold Time (BCLK standard)		0		ns
th(RAS-RAD)	Row Address Output Hold Time after RAS Output		(Note 1)		ns
td(BCLK-RAS)	RAS Output Delay Time (BCLK standard)			18	ns
th(BCLK-RAS)	RAS Output Hold Time (BCLK standard)		0		ns
trp	RAS High ("H") Hold Time		(Note 1)		ns
td(BCLK-CAS)	CAS Output Delay Time (BCLK standard)			18	ns
th(BCLK-CAS)	CAS Output Hold Time (BCLK standard)		0		ns
td(BCLK-DW)	DW Output Delay Time (BCLK standard)			18	ns
th(BCLK-DW)	DW Output Hold Time (BCLK standard)		-3		ns
tsu(DB-CAS)	CAS Output Setup Time after DB output		(Note 1)		ns
th(BCLK-DB)	DB Signal Output Hold Time (BCLK standard)		-7		ns
tsu(CAS-RAS)	CAS Output Setup Time before RAS Output (refresh)		(Note 1)		ns

NOTES:

1. Values can be obtained from the following equations, according to the BCLK frequency.

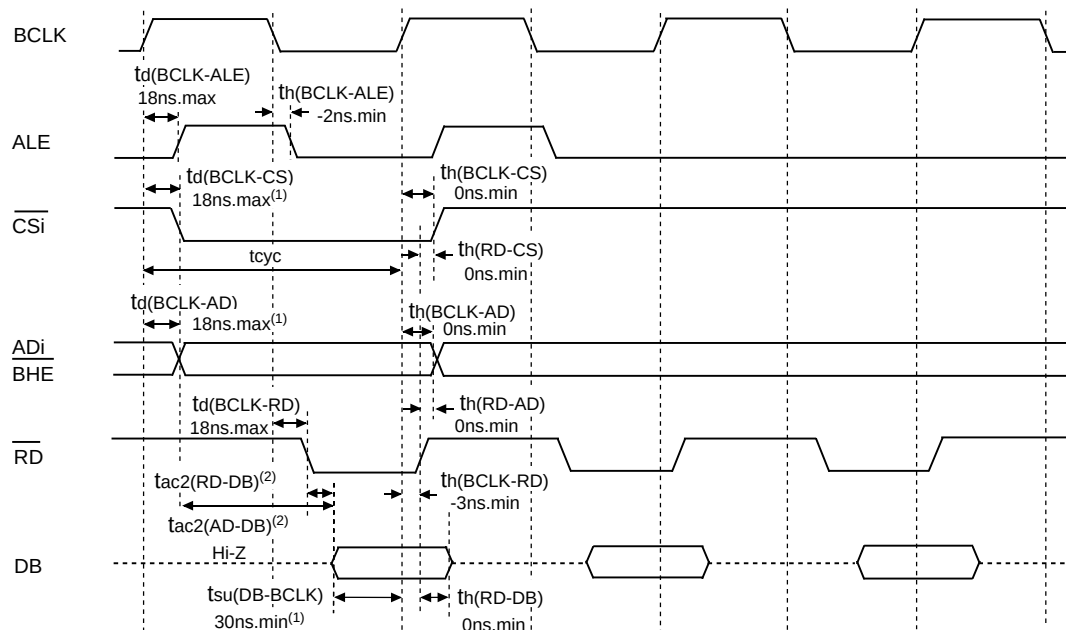
$$th(RAS - RAD) = \frac{10^9}{f(BCLK) \times 2} - 13 \quad [ns]$$

$$trp = \frac{10^9 \times 3}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$tsu(DB - CAS) = \frac{10^9}{f(BCLK)} - 20 \quad [ns]$$

$$tsu(CAS - RAS) = \frac{10^9}{f(BCLK) \times 2} - 13 \quad [ns]$$

Memory Expansion Mode and Microprocessor Mode (with no wait state) Read Timing



NOTES:

- Values guaranteed only when the microcomputer is used independently.

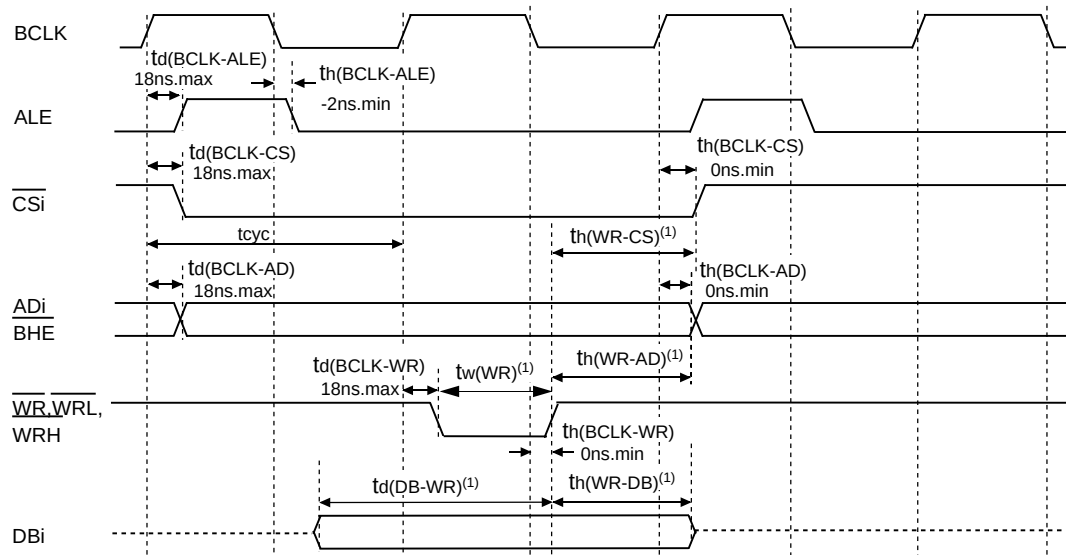
A maximum of 35ns is guaranteed for $t_d(\text{BCLK-AD}) + t_{su}(\text{DB-BCLK})$.

- Varies with operation frequency:

$$t_{ac2}(\text{RD-DB}) = (t_{cyc}/2 - 35)\text{ns.max}$$

$$t_{ac2}(\text{AD-DB}) = (t_{cyc} - 35)\text{ns.max}$$

Write Timing



NOTES:

- Varies with operation frequency.

$$t_d(\text{DB-WR}) = (t_{cyc} - 20)\text{ns.min}$$

$$t_h(\text{WR-DB}) = (t_{cyc}/2 - 10)\text{ns.min}$$

$$t_h(\text{WR-AD}) = (t_{cyc}/2 - 10)\text{ns.min}$$

$$t_h(\text{WR-CS}) = (t_{cyc}/2 - 10)\text{ns.min}$$

$$t_w(\text{WR}) = (t_{cyc}/2 - 15)\text{ns.min}$$

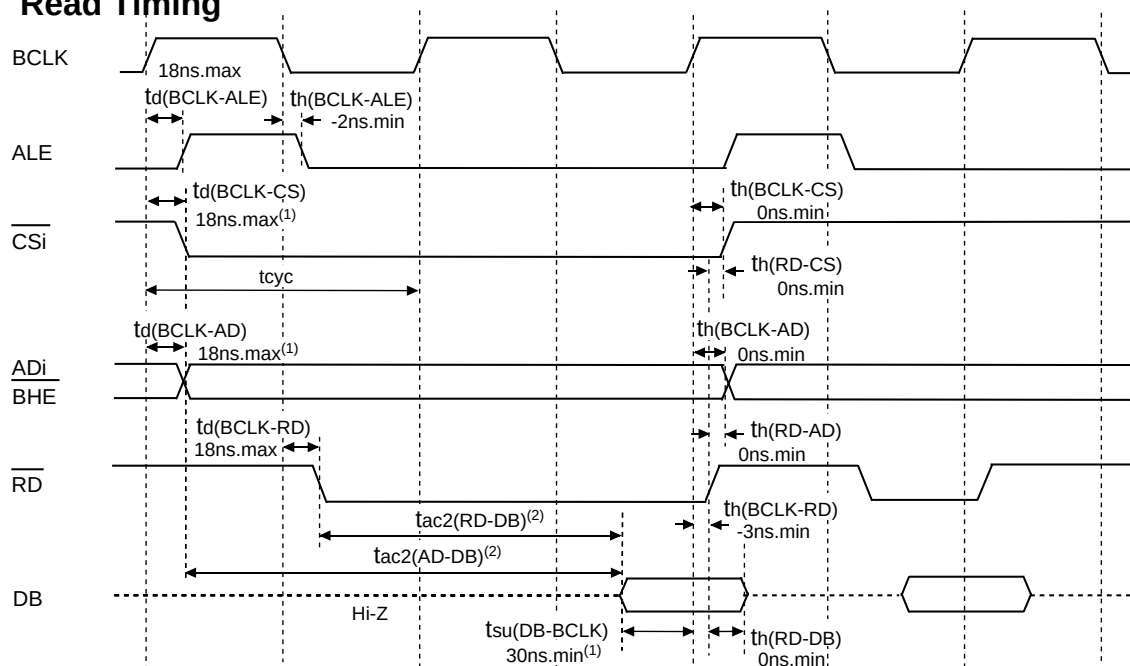
Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.10 V_{CC}=3.3V Timing Diagram (1)

V_{CC}=3.3V

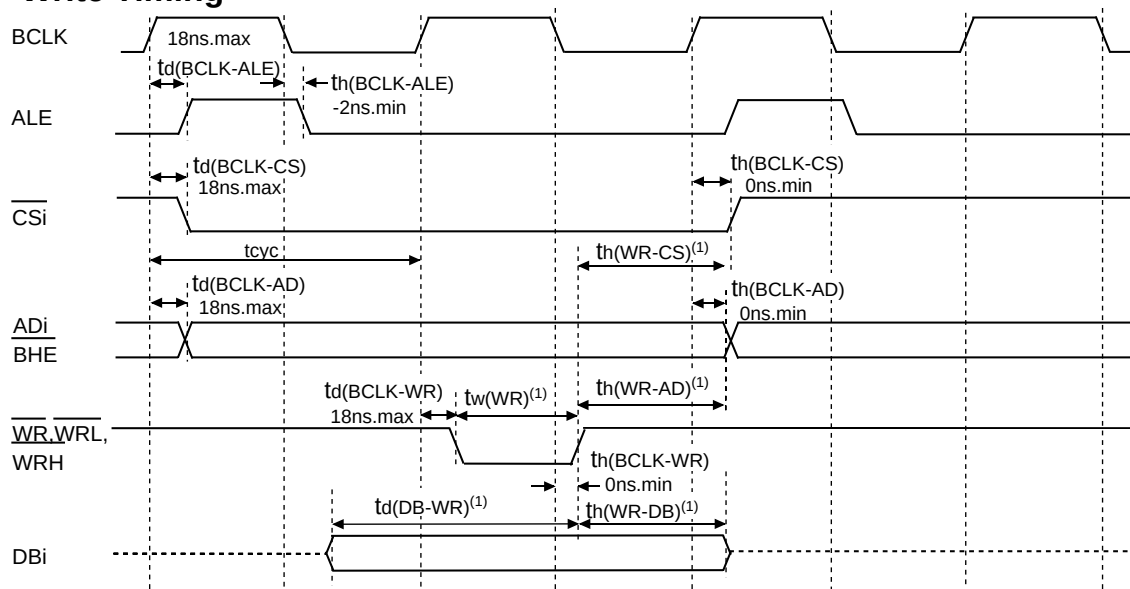
Memory Expansion Mode and Microprocessor Mode (with a wait state) Read Timing



NOTES:

- Values guaranteed only when the microcomputer is used independently. A maximum of 35ns is guaranteed for $t_d(\text{BCLK-AD}) + t_{su}(\text{DB-BCLK})$.
- Varies with operation frequency.
 $t_{ac2}(\text{RD-DB}) = (t_{cyc}/2 \times m - 35)\text{ns.max}$ ($m=3$ with 1 wait state, $m=5$ with 2 wait states and $m=7$ with 3 wait states)
 $t_{ac2}(\text{AD-DB}) = (t_{cyc} \times n - 35)\text{ns.max}$ ($n=2$ with 1 wait state, $n=3$ with 2 wait states and $n=4$ with 3 wait states)

Write Timing



NOTES:

- Varies with operation frequency.
 $t_d(\text{DB-WR}) = (t_{cyc} \times n - 20)\text{ns.min}$ ($n=1$ with 1 wait state, $n=2$ with 2 wait states and $n=3$ with 3 wait states)
 $t_h(\text{WR-DB}) = (t_{cyc}/2 - 10)\text{ns.min}$
 $t_h(\text{WR-AD}) = (t_{cyc}/2 - 10)\text{ns.min}$
 $t_h(\text{WR-CS}) = (t_{cyc}/2 - 10)\text{ns.min}$
 $t_w(\text{WR}) = (t_{cyc}/2 \times n - 15)\text{ns.min}$ ($n=1$ with 1 wait state, $n=3$ with 2 wait states and $n=5$ with 3 wait states)

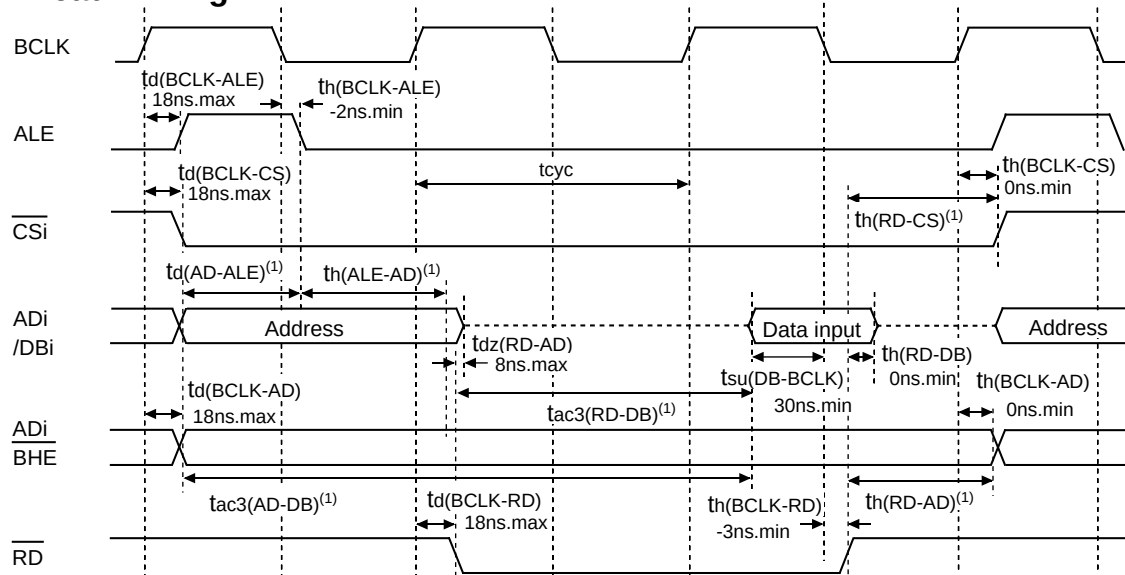
Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.11 V_{CC}=3.3V Timing Diagram (2)

V_{CC}=3.3V**Memory Expansion Mode and Microprocessor Mode**

(with a wait state, when accessing an external memory and using the multiplexed bus)

Read Timing**NOTES:**

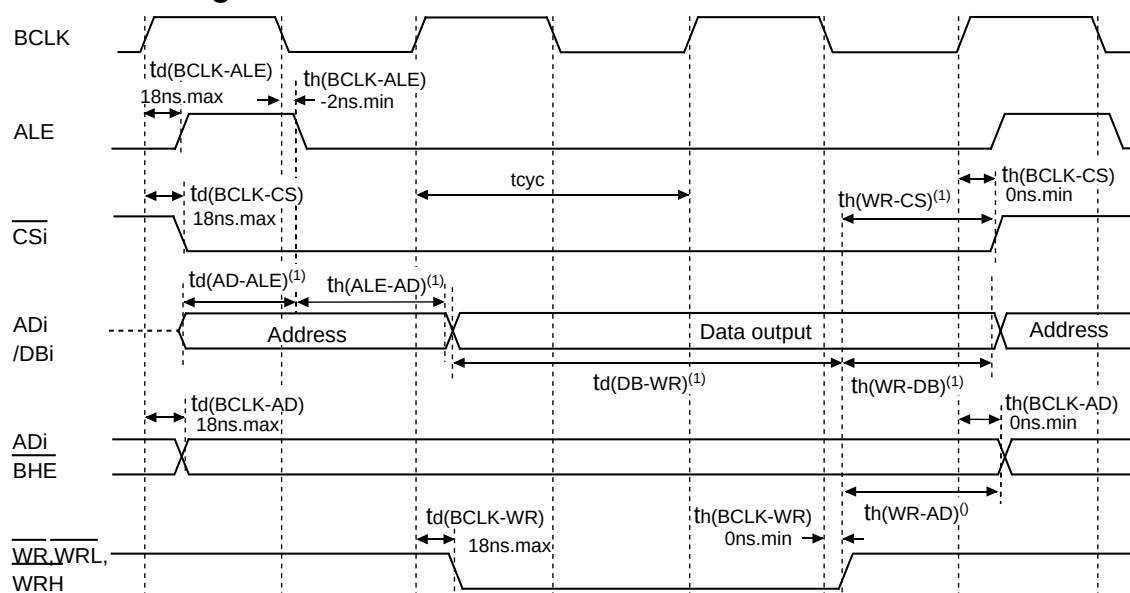
1. Varies with operation frequency.

$$t_d(\text{AD-ALE}) = (t_{\text{cyc}}/2 - 20)\text{ns.min}$$

$$t_h(\text{ALE-AD}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}, t_h(\text{RD-AD}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}, t_h(\text{RD-CS}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}$$

$$t_{ac3}(\text{RD-DB}) = (t_{\text{cyc}}/2 \times m - 35)\text{ns.max} \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$t_{ac3}(\text{AD-DB}) = (t_{\text{cyc}}/2 \times n - 35)\text{ns.max} \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

Write Timing**NOTES:**

1. Varies with operation frequency.

$$t_d(\text{AD-ALE}) = (t_{\text{cyc}}/2 - 20)\text{ns.min}$$

$$t_h(\text{ALE-AD}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}, t_h(\text{WR-AD}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}$$

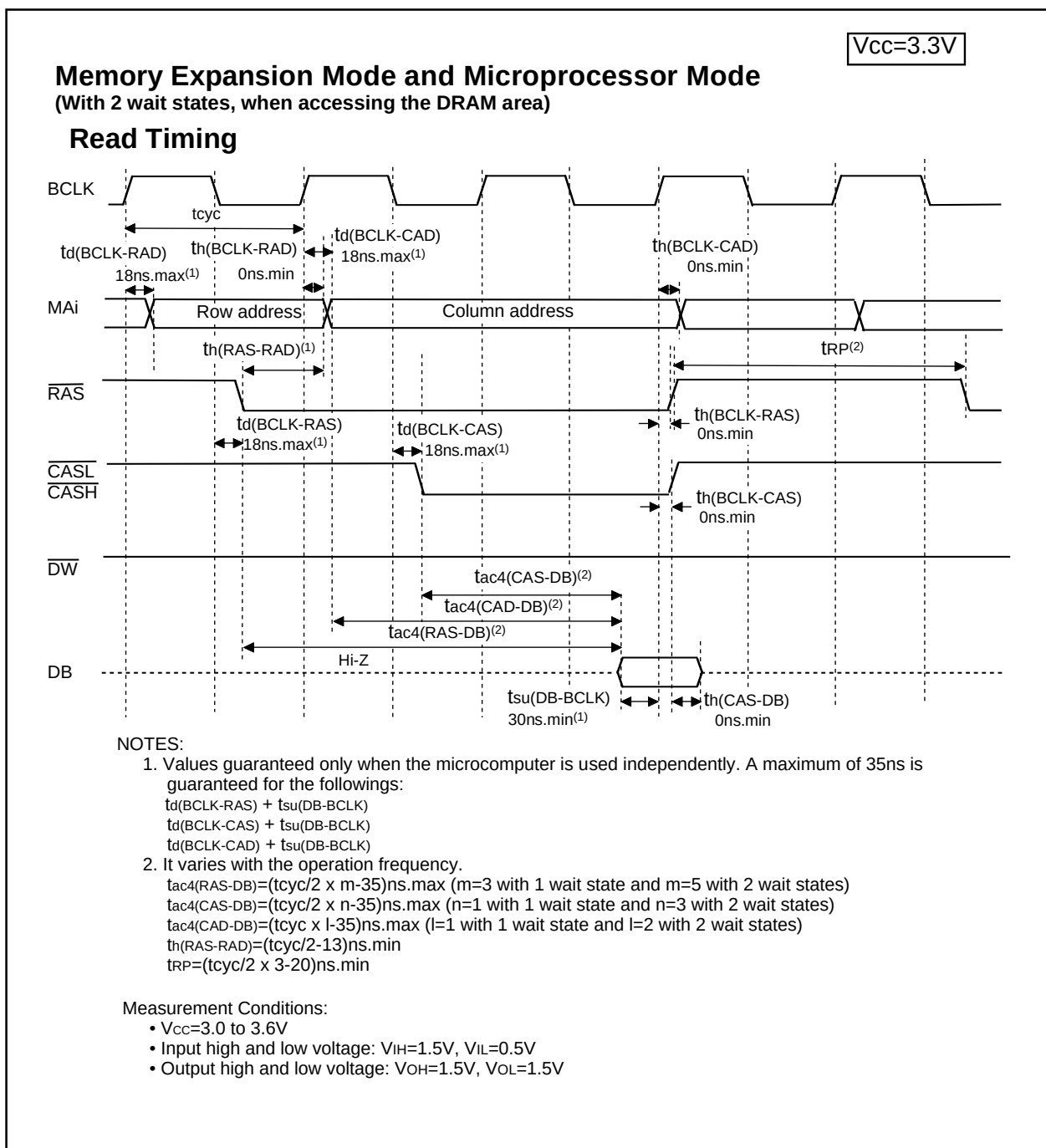
$$t_h(\text{WR-CS}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}, t_h(\text{WR-DB}) = (t_{\text{cyc}}/2 - 10)\text{ns.min}$$

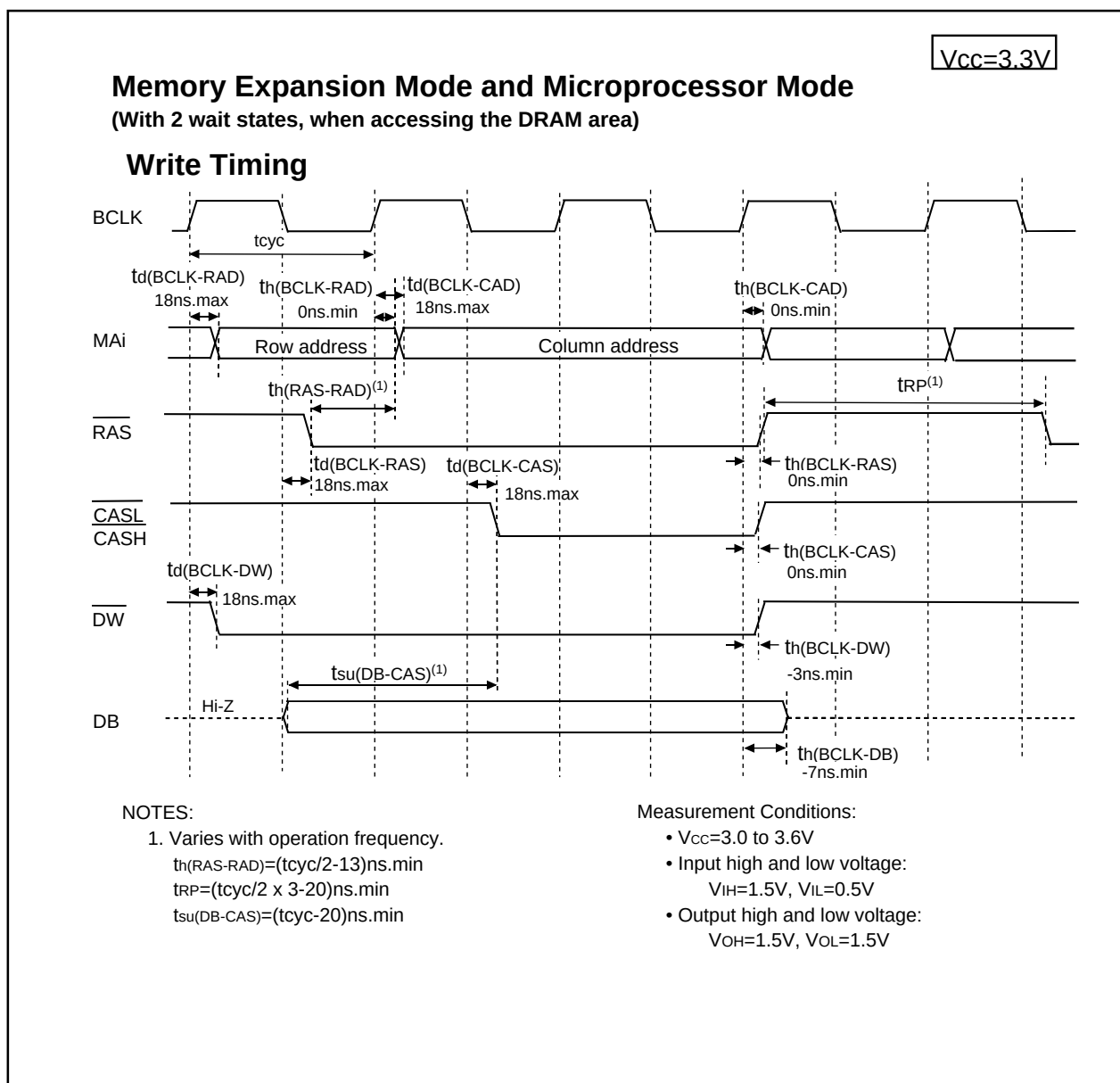
$$t_d(\text{DB-WR}) = (t_{\text{cyc}}/2 \times m - 25)\text{ns.min} \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

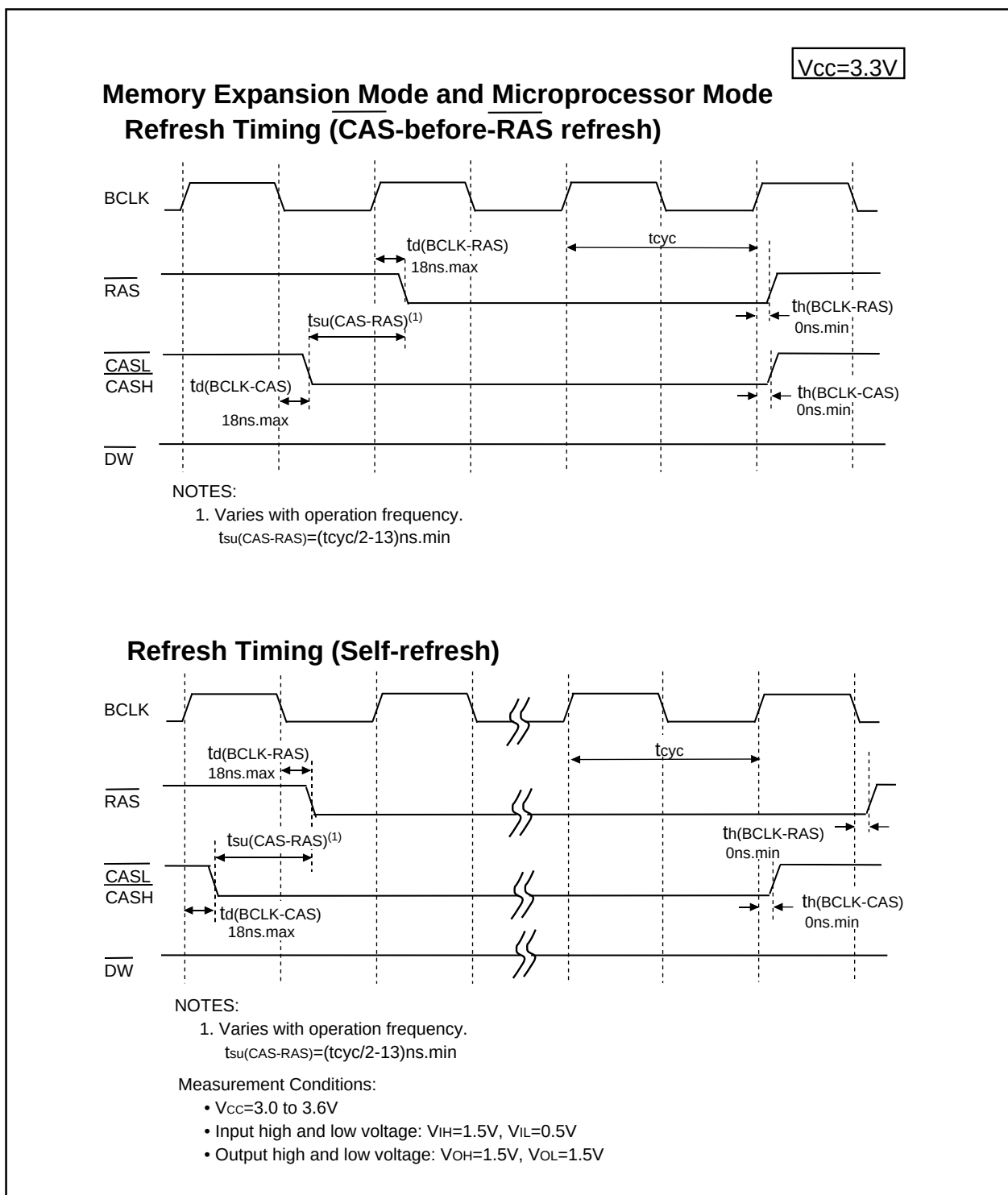
Measurement Conditions:

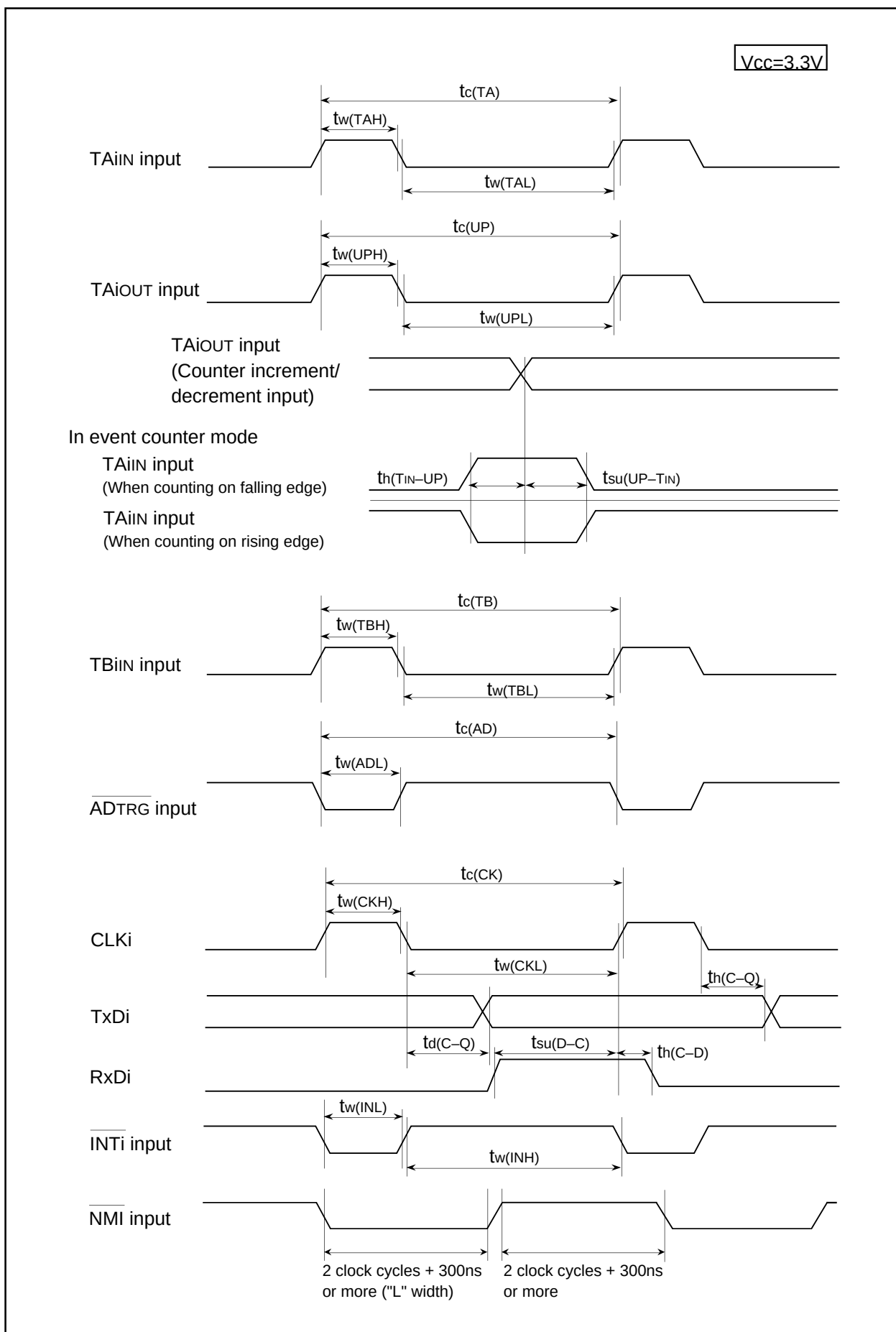
- V_{CC}=3.0 to 3.6V
- Input high and low voltage:
V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.12 V_{CC}=3.3V Timing Diagram (3)

Figure 5.13 $V_{CC}=3.3V$ Timing Diagram (4)

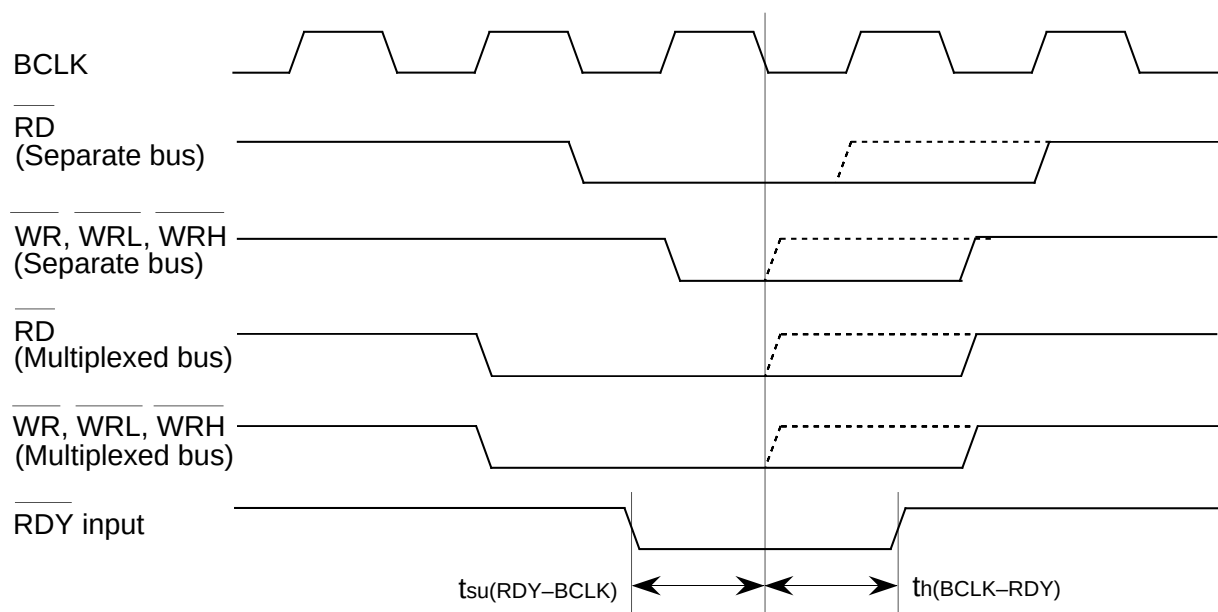
Figure 5.14 V_{CC}=3.3V Timing Diagram (5)

Figure 5.15 V_{CC}=3.3V Timing Diagram (6)

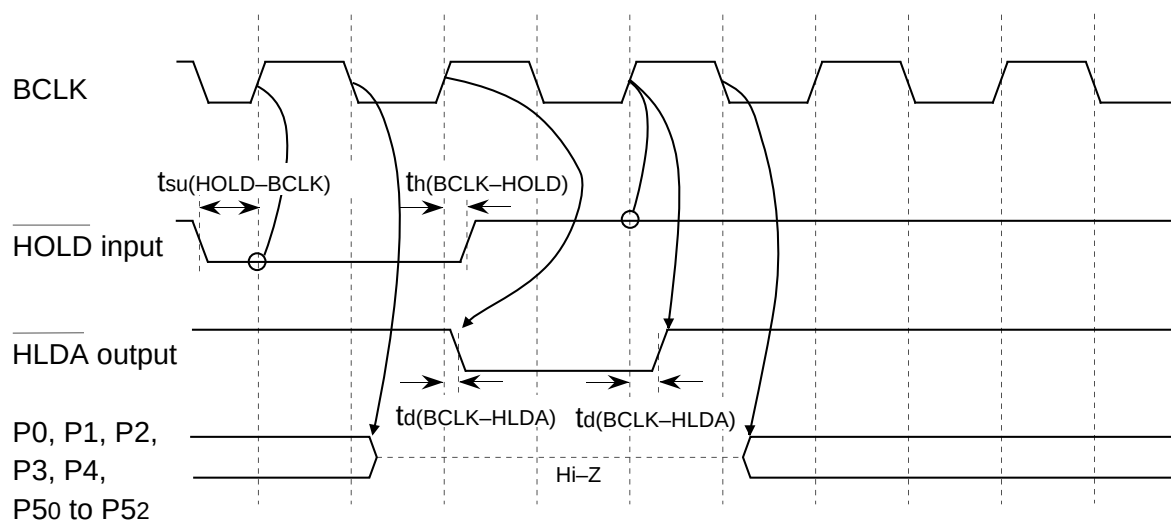
Figure 5.16 $V_{CC}=3.3V$ Timing Diagram (7)

V_{CC}=3.3V

Memory Expansion Mode and Microprocessor Mode (Valid only with a wait state)



(Valid with a wait state and no wait state)



Measurement Conditions:

- V_{CC}=3.0 to 3.6V
- Input high and low voltage: V_{IH}=2.4V, V_{IL}=0.6V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

Figure 5.17 V_{CC}=3.3V Timing Diagram (8)

5.2 Electrical Characteristics (M32C/83T)

Table 5.45 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V _{CC}	Supply Voltage		V _{CC} =AV _{CC}	-0.3 to 6.0	V
AV _{CC}	Analog Supply Voltage		V _{CC} =AV _{CC}	-0.3 to 6.0	V
V _I	Input Voltage	RESET, CNV _{SS} , BYTE, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , V _{REF} , X _{IN}		-0.3 to V _{CC} +0.3	V
		P7 ₀ , P7 ₁		-0.3 to 6.0	V
V _O	Output Voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{OUT}		-0.3 to V _{CC} +0.3	V
P _d	Power Dissipation		T _{opr} =25° C	400	mW
T _{opr}	Operating Ambient Temperature		T version	-40 to 85	° C
T _{stg}	Storage Temperature			-65 to 150	° C

NOTES:

1. P11 to P15 are provided in the 144-pin package.

Table 5.46 Recommended Operating Conditions(V_{CC}=4.2 to 5.5V, V_{SS}=0V at T_{opr} = -40 to 85°C (T version) unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC}	Supply Voltage		4.2	5.0	5.5	V
AV _{CC}	Analog Supply Voltage			V _{CC}		V
V _{SS}	Supply Voltage			0		V
AV _{SS}	Analog Supply Voltage			0		V
V _{IH}	Input High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	0.8V _{CC}		V _{CC}	V
		P70, P71	0.8V _{CC}		6.0	
V _{IL}	Input Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	0		0.2V _{CC}	V
I _{OH(peak)}	Peak Output High ("H") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-10.0	mA
I _{OH(avg)}	Average Output High ("H") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			-5.0	mA
I _{OL(peak)}	Peak Output Low ("L") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			10.0	mA
I _{OL(avg)}	Average Output Low ("L") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁴⁾			5.0	mA
f(X _{IN})	Main Clock Input Frequency	V _{CC} =4.2 to 5.5V	0		32	MHz
f(X _{CIN})	Sub Clock Oscillation Frequency			32.768	50	kHz

NOTES:

- Typical values when average output current is 100ms.
- Total I_{OL(peak)} for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be 80mA or less.
Total I_{OH(peak)} for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be -80mA or less.
Total I_{OL(peak)} for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be 80mA or less.
Total I_{OH(peak)} for P3, P4, P5, P6, P72 to P77, P80 to P84, P12 and P13 must be -80mA or less.
- V_{IH} and V_{IL} reference for P87 applies when P87 is used as a programmable input port.
It does not apply when P87 is used as X_{CIN}.
- P11 to P15 are provided in the 144-pin package only.

**Table 5.47 Electrical Characteristics (V_{CC} = 4.2 to 5.5 V, V_{SS} = 0V
at Topr = -40 to 85°C(T version), f(X_{IN})=32MHz unless otherwise specified)**

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-5mA	V _{CC} -2.0			V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-200μA	V _{CC} -0.3			
		X _{OUT}	I _{OH} =-1mA	3.0			V
		X _{COU} T	No load applied		3.3		V
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =5mA			2.0	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =200μA			0.45	V
		X _{OUT}	I _{OL} =1mA			2.0	V
		X _{COU} T	No load applied		0		V
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0 _{IN} -TA4 _{IN} , TB0 _{IN} -TB5 _{IN} , INT0-INT5, AD _{TRG} , CTS0-CTS4, CLK0-CLK4, TA0 _{OUT} -TA4 _{OUT} , NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =5V			5.0	μA
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	30	50	167	kΩ
R _{fXIN}	Feedback Resistance	X _{IN}			1.5		MΩ
R _{fXCIN}	Feedback Resistance	X _{CIN}			10		MΩ
V _{RAM}	RAM Standby Voltage			2.5			V
I _{CC}	Power Supply Current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to V _{SS}	f(X _{IN})=32 MHz, square wave, no division		40	54	mA
			f(X _{CIN})=32 kHz, with a wait state, Topr=25° C		470		μA
			Topr=25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

Table 5.48 A/D Conversion Characteristics (V_{CC} = AV_{CC} = V_{REF} = 4.2 to 5.5V, V_{SS} = AV_{SS} = 0V at Topr = -40 to 85°C (T version), f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution	V _{REF} =V _{CC}			10	Bits
INL	Integral Nonlinearity Error	V _{REF} =V _{CC} =5V			±3	LSB
						LSB
		External op-amp connection mode			±7	LSB
DNL	Differential Nonlinearity Error				±1	LSB
-	Offset Error				±3	LSB
-	Gain Error				±3	LSB
RLADDER	Resistor Ladder	V _{REF} =V _{CC}	8		40	kΩ
t _{CONV}	10-bit Conversion Time		2.1			μs
t _{CONV}	8-bit Conversion Time		1.8			μs
t _{SAMP}	Sample Time		0.2			μs
V _{REF}	Reference Voltage		2		V _{CC}	V
V _{IA}	Analog Input Voltage		0		V _{REF}	V

NOTES:

1. Divide f(X_{IN}), if exceeding 16 MHz, to keep φ_{AD} frequency at 16 MHz or less.

Table 5.49 D/A Conversion Characteristics (V_{CC} = V_{REF} = 4.2 to 5.5V, V_{SS} = AV_{SS} = 0V at Topr = -40 to 85°C (T version), f(X_{IN}) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	kΩ
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTES:

1. Measurement results when using one D/A converter. The DAI register (i=0, 1) of the D/A converter not being used is set to "00₁₆". The resistor ladder in the A/D converter is excluded. I_{VREF} flows even if the VCUT bit in the ADiCON1 register is set to "0" (no V_{REF} connection).

Table 5.50 Flash Memory Version Electrical Characteristics

Parameter	Standard			Unit
	Min	Typ	Max	
Program Time (per page)		8	120	ms
Block Erase Time (per block)		50	600	ms

NOTES:

1. V_{CC}= 4.2 to 5.5V at Topr= 0 to 60° C, unless otherwise specified

Timing Requirements (V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at T_{opr} = –40 to 85°C (T version) unless otherwise specified)

Table 5.51 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
t _c	External Clock Input Cycle Time	33		ns
t _{w(H)}	External Clock Input High ("H") Pulse Width	13		ns
t _{w(L)}	External Clock Input Low ("L") Pulse Width	13		ns
t _r	External Clock Rise Time		5	ns
t _f	External Clock Fall Time		5	ns

Timing Requirements(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –40 to 85°C (T version) unless otherwise specified)**Table 5.52 Timer A Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAin Input Cycle Time	100		ns
tw(TAH)	TAin Input High ("H") Pulse Width	40		ns
tw(TAL)	TAin Input Low ("L") Pulse Width	40		ns

Table 5.53 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAin Input Cycle Time	400		ns
tw(TAH)	TAin Input High ("H") Pulse Width	200		ns
tw(TAL)	TAin Input Low ("L") Pulse Width	200		ns

Table 5.54 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAin Input Cycle Time	200		ns
tw(TAH)	TAin Input High ("H") Pulse Width	100		ns
tw(TAL)	TAin Input Low ("L") Pulse Width	100		ns

Table 5.55 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TAin Input High ("H") Pulse Width	100		ns
tw(TAL)	TAin Input Low ("L") Pulse Width	100		ns

Table 5.56 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TAiout Input Cycle Time	2000		ns
tw(UPH)	TAiout Input High ("H") Pulse Width	1000		ns
tw(UPL)	TAiout Input Low ("L") Pulse Width	1000		ns
tsu(UP-TIN)	TAiout Input Setup Time	400		ns
th(TIN-UP)	TAiout Input Hold Time	400		ns

Timing Requirements(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –40 to 85°C (T version) unless otherwise specified)**Table 5.57 Timer B Input (Count Source Input in Event Counter Mode)**

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiIn Input Cycle Time (counted on one edge)	100		ns
tw(TBH)	TBiIn Input High ("H") Pulse Width (counted on one edge)	40		ns
tw(TBL)	TBiIn Input Low ("L") Pulse Width (counted on one edge)	40		ns
tc(TB)	TBiIn Input Cycle Time (counted on both edges)	200		ns
tw(TBH)	TBiIn Input High ("H") Pulse Width (counted on both edges)	80		ns
tw(TBL)	TBiIn Input Low ("L") Pulse Width (counted on both edges)	80		ns

Table 5.58 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiIn Input Cycle Time	400		ns
tw(TBH)	TBiIn Input High ("H") Pulse Width	200		ns
tw(TBL)	TBiIn Input Low ("L") Pulse Width	200		ns

Table 5.59 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiIn Input Cycle Time	400		ns
tw(TBH)	TBiIn Input High ("H") Pulse Width	200		ns
tw(TBL)	TBiIn Input Low ("L") Pulse Width	200		ns

Table 5.60 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(AD)	ADTRG Input Cycle Time (required for re-trigger)	1000		ns
tw(ADL)	ADTRG Input Low ("L") Pulse Width	125		ns

Table 5.61 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(CK)	CLKi Input Cycle Time	200		ns
tw(CKH)	CLKi Input High ("H") Pulse Width	100		ns
tw(CKL)	CLKi Input Low ("L") Pulse Width	100		ns
td(CQ)	TxDi Output Delay Time		80	ns
th(CQ)	TxDi Hold Time	0		ns
tsu(DQ)	RxDi Input Set Up Time	30		ns
th(CQ)	RxDi Input Hold Time	90		ns

Table 5.62 External Interrupt INTi Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(INH)	INTi Input High ("H") Pulse Width	250		ns
tw(INL)	INTi Input Low ("L") Pulse Width	250		ns

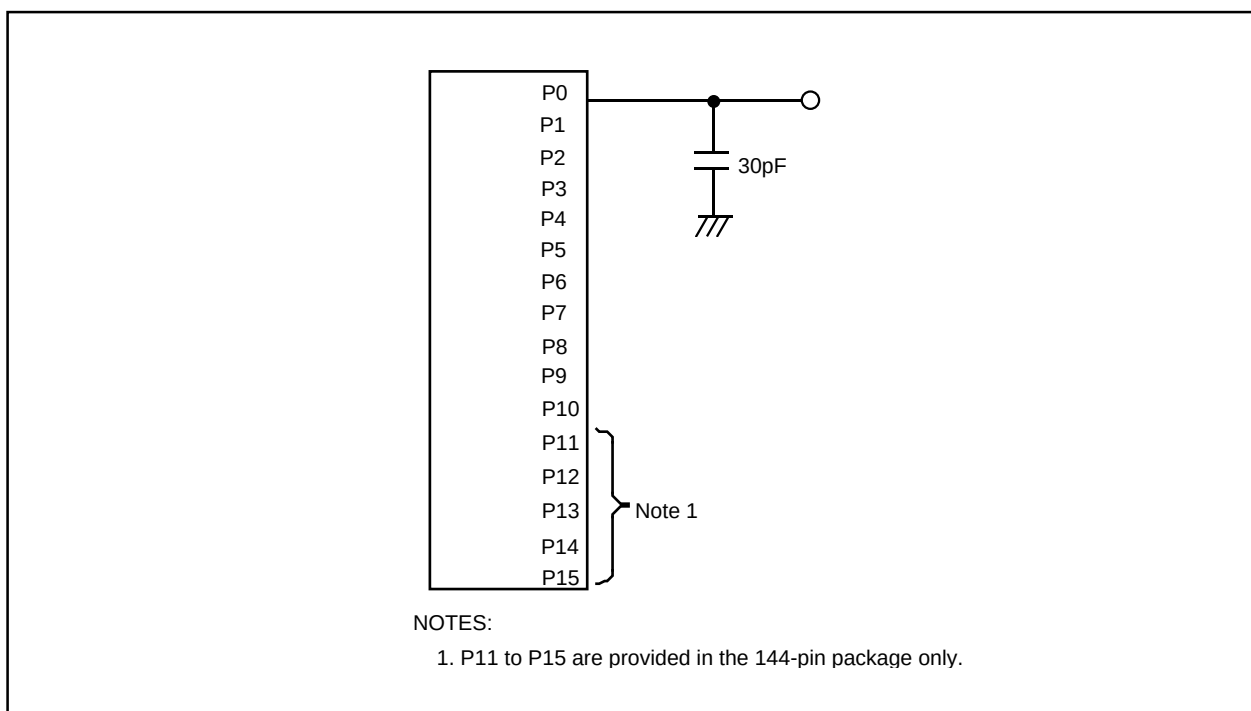


Figure 5.18 P0 to P15 Measurement Circuit

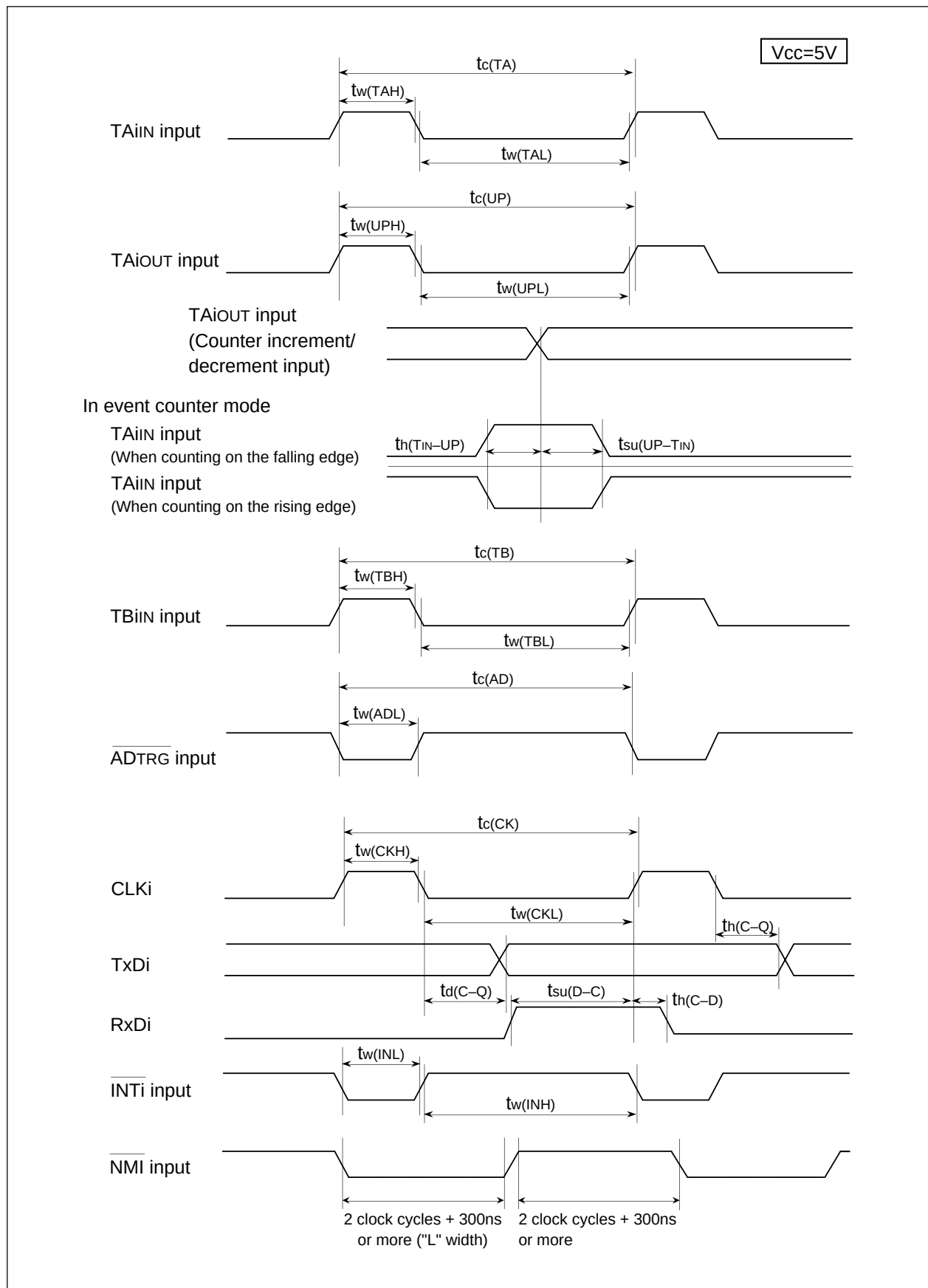
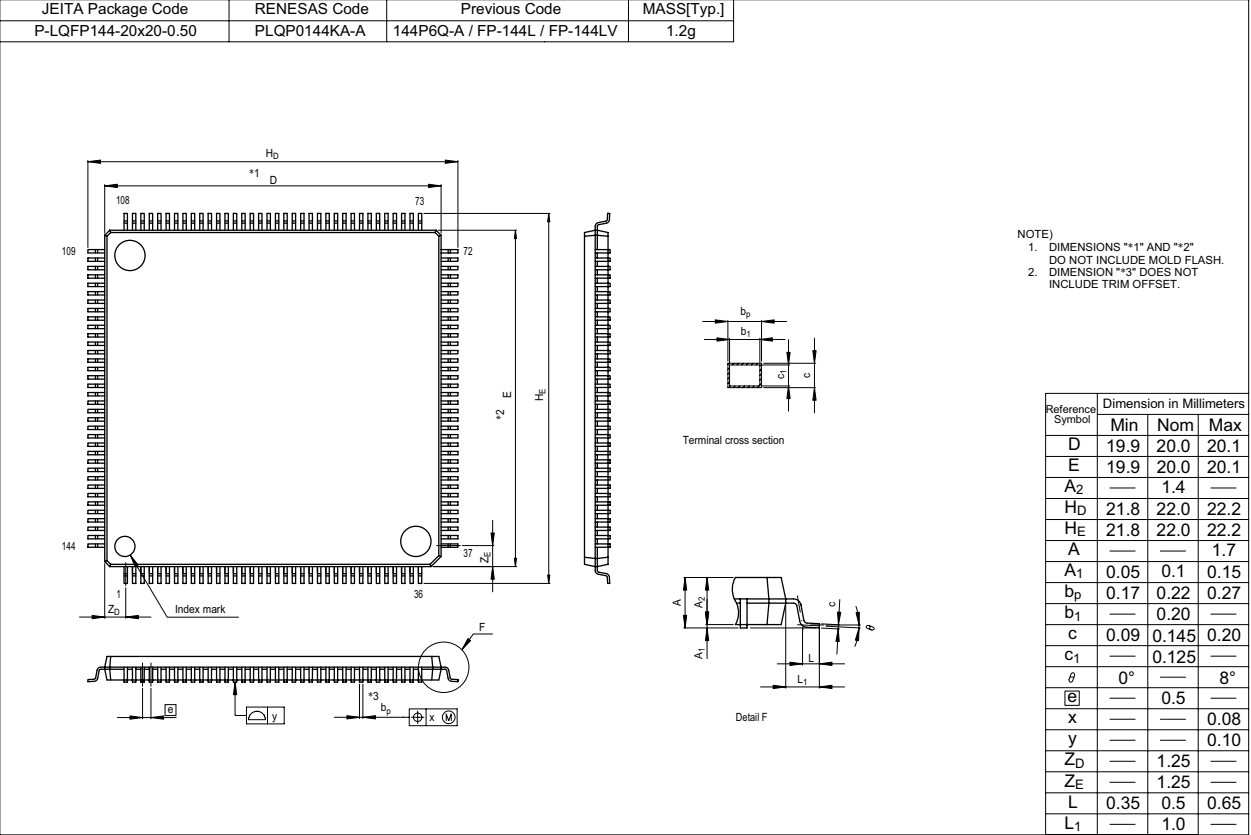


Figure 5.19 VCC = 5 V Timing Diagram(1)

Package Dimensions

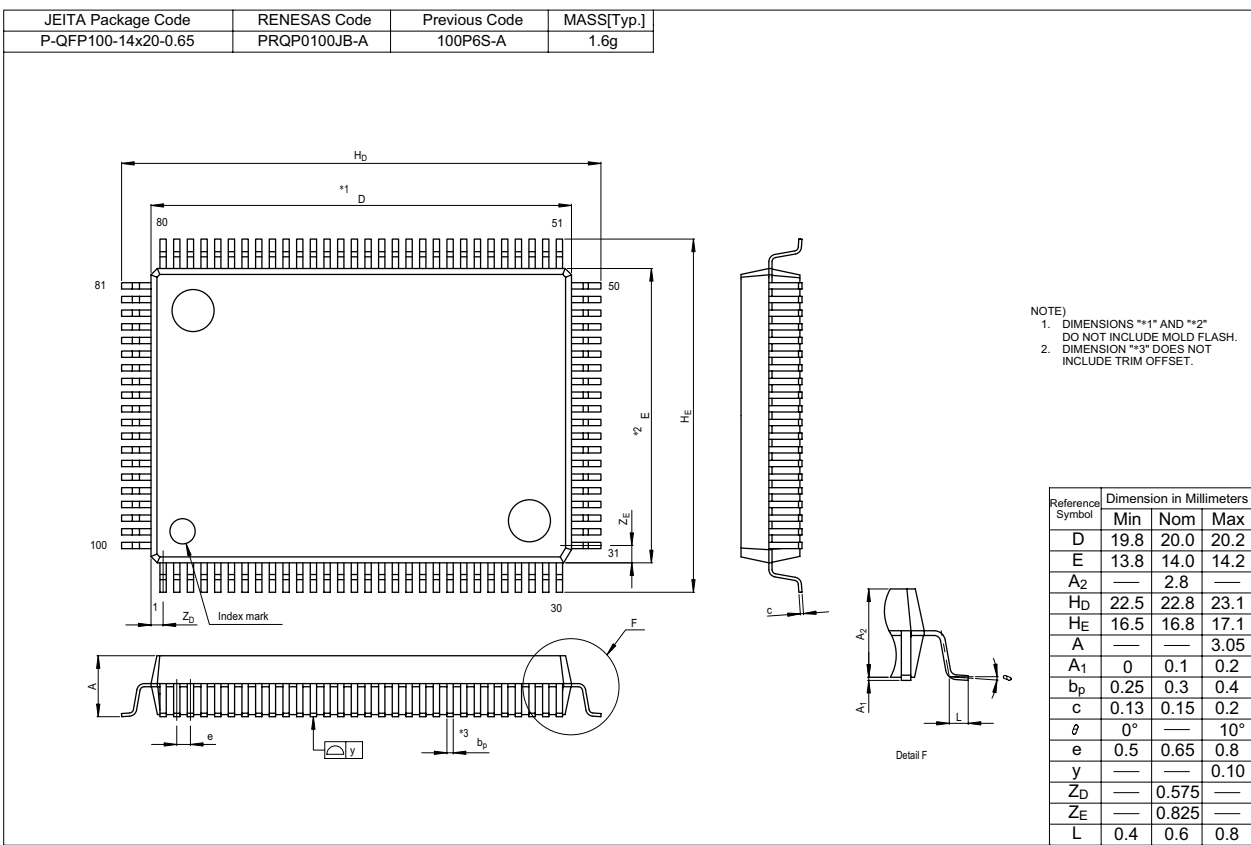
PLQ0144KA-A (144P6Q-A)

Plastic 144pin 20 X 20 mm body LQFP



PRQP0100JB-A (100P6S-A)

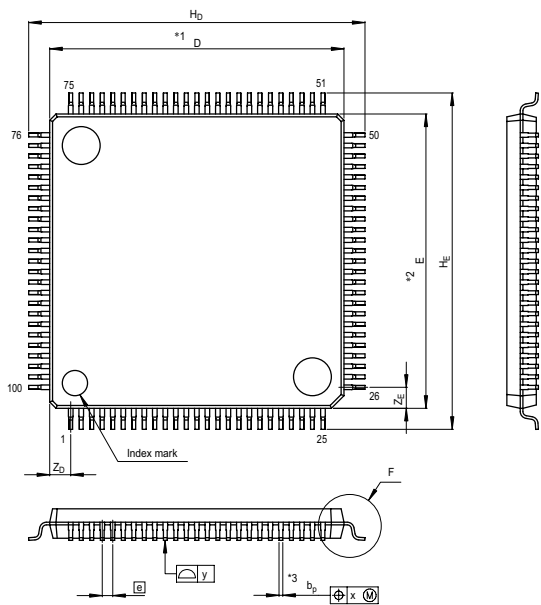
Plastic 100pin 14 X 20 mm body LQFP



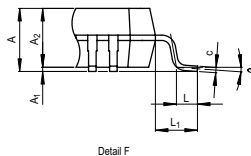
PLQP0100KB-A (100P6Q-A)

Plastic 100pin 14 X 14 mm body LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



Terminal cross section



Detail F

NOTE)

- NOTE)
1. DIMENSIONS "1" AND "2" DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION "3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A ₂	—	1.4	—
H _D	15.8	16.0	16.2
H _E	15.8	16.0	16.2
A	—	—	1.7
A ₁	0.05	0.1	0.15
b _p	0.15	0.20	0.25
b ₁	—	0.18	—
c	0.09	0.145	0.20
c ₁	—	0.125	—
θ	0°	—	8°
Ⓔ	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z _D	—	1.0	—
Z _E	—	1.0	—
L	0.35	0.5	0.65
L ₁	—	1.0	—

REVISION HISTORY

M32C/83 GROUP (M32C/83, M32C/83T) Datasheet

Rev.	Date	Description	
		Page	Summary
1.10	2003-9	-	New Document
1.20	2003-12		Maximum operating frequency changed from 30 MHz to 32 MHz. Overview, Electrical Characteristics Table 1.1 M32C/83 Group Performance (144-Pin Package) Table 1.2 M32C/83 Group Performance (100-Pin Package) Table 5.2 Recommended Operating Conditions Table 5.3 Electrical Characteristics
1.30	2004-06	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
1.41	2006-01	All Pages	M32C/83T version added; Package code changed: 144P6Q-A to PLQP0144KA-A, 100P6Q-A to PLQP0100KB-A, 100P6S-A to PRQP0100JB-A
		All Pages	Word standardized: Clock Generation Circuit , On-chip Oscillator, A/D Converter, D/A Converter, XY Conversion, Low -power consumption
		1 2, 3 5	Overview • 1.1 Applications Automobile added • Tables 1.1 and 1.2 M32C/83 Group (M32C/83, M32C/83T) Performance • Table 1.3 M32C/83 Group (1) (M32C/83) Information updated • Table 1.3 M32C/83 Group (2) (M32C/83T) M32C/83T product information added • Figure 1.2 Product Numbering System Classification modified • Table 1.4 Pin Characteristics for 144-Pin Package Note 1 added • Table 1.5 Pin Characteristics for 100-Pin Package Note 1 added • Table 1.6 Pin Description modified, notes added
		21	Memory • Figure 3.1 Memory Map modified; Note 2 modified, notes 3 and 4 added
		22 to 23	Special Function Registers (SFR) • Note 2 added
		45	Reset • Figure 5.2 Reset Sequence Note 2 added
		46 54 62 64	Electrical Characteristics • Table 5.3 Electrical Characteristics Minimum standard values for V_{OH} revised, values for I_{CC} when f(X_{IN})=32 MHz, square wave, no division revised, one condition of "f(X_{IN})=32 MHz, square wave, no division" deleted • Table 5.23 Memory Expansion Mode and Microprocessor Mode Symbols for Row Address Output Delay Time and for Row Address Output Hold Time (BCLK standard) modified • Figure 5.8 V_{CC}=5 V Timing Diagram (7) Timing for $\overline{\text{NMI}}$ input added • Table 5.24 Electrical Characteristics Minimum standard value for V_{OH} revised

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