

# DS90CP22 2x2 LVDS Switch Demonstration Kit Documentation

Rev2

**Interface Products** 

National Semiconductor Corporation Interface Products LIT# LVDSCP22EVK.DOC Date: Feb. 2000

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#### Introduction:

National Semiconductor's Interface Products Group provides this demonstration kit of the DS90CP22 to help demonstrate the use and performance of the device. The user needs to provide the proper signal levels (TTL/CMOS, LVDS or LVPECL) to the inputs of the device. This board is mainly intended to allow the user to evaluate the performance of the device.

The DS90CP22 board is designed with a  $50\Omega$  single-ended transmission line, which accepts LVDS signals or LVPECL levels to the inputs IN0+/- and IN1+/- from a signal generator. The SEL0 and SEL1 pins can also be driven by a signal generator. These inputs to the DS90CP22 are terminated with a  $50\Omega$  to ground.

The EN0, EN1 (enable pins), SEL0 and SEL1 accepts TTL/CMOS logic. The maximum voltage to these pins is 3.6V.

#### **Contents of Demonstration Kit:**

- 1) One DS90CP22 board
- 2) DS90CP22 Demonstration kit documentation (LIT#LVDSCP22EVK.DOC)

# Example of how to set-up the DS90CP22 demonstration board to take AC measurements

#### AC Set-Up:

- 1. Apply Vcc=3.3V and Ground to the board power pads.
- 2. Apply V\_bias=8.25V from a separate source other than Vcc to the board. Depending on the resistor variation, this voltage should be changed to ensure that the output Vos is +1.2V. To do this, simply TRI-STATE the output and monitor the voltage node after the  $1.62k\Omega$  resistor (bottom PCB traces). This should be at +1.2V. In order to probe using  $50\Omega$  load the V\_bias is used because LVDS cannot drive  $50\Omega$  load to ground. The resistors 10:1 (20dB) attenuation (453 $\Omega$  with  $50\Omega$  scope load) are also used because  $50\Omega$  scopes have a max voltage of 1-2V.
- Input signals
  - A. Connect all 4 inputs (IN0+/-, IN1+/-) from the differential signal generator.
  - B. Place shunt connectors to the 3 header connector of EN0 and EN1. The outputs are enabled when positioned to H (high).
  - C. SEL0 and SEL1 are used for switch configurations. They accept TTL/CMOS logic signal (0-Vcc). Please reference the datasheet for the switch matrix table. When using a signal generator as a source, the shunt

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connectors to the 3 header post of SEL0 and SEL1 must be removed. When any of the SEL are applied to Vcc using the shunt jumper, the current consumption increase (I=3.3V/50 $\Omega$  = 6.6mA) because of the 50 $\Omega$  termination resistor.

- 4. Output signals
  - A. Connect all 4 output lines (OUT0+/-, OUT1+/-) to probe on scope (50 $\Omega$  & High B/W).
- 5. Generate LVDS input signals or LVPECL to the device using a signal generator by setting the high and low voltage level.
- 6. EN0 and EN1 are used to enable the outputs (Vcc must be applied to these pins to enable).
- 7. Measure propagation delay between input at 0V differential crossing point to output 0V differential crossing point. Typical propagation delay is 1.3ns.
- Measure rise and fall time by generating a third signal from the OUT+ and OUT- output signals

Vdiff = (OUT+) - (OUT-) and measure from 20% to 80%

#### **Recommended Equipment:**

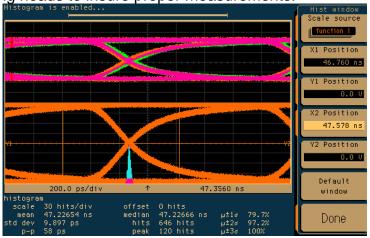
- HFS9009 Signal Generator (differential output for Din w/HFS9DG2, singleended output for EN0, EN1, SEL0, SEL1 w/HFS9DG1)
- ◆ Tektronix SD-22 Sampling Heads in a SM-11 using a Tektronix 11801B Digital Sampling Scope
- Pasternack 20dB attenuators

#### **Recommended Cables:**

Matched length RG142B double-shielded cables for high speed measurements and RG58AX coax cables acceptable for low speed measurements.

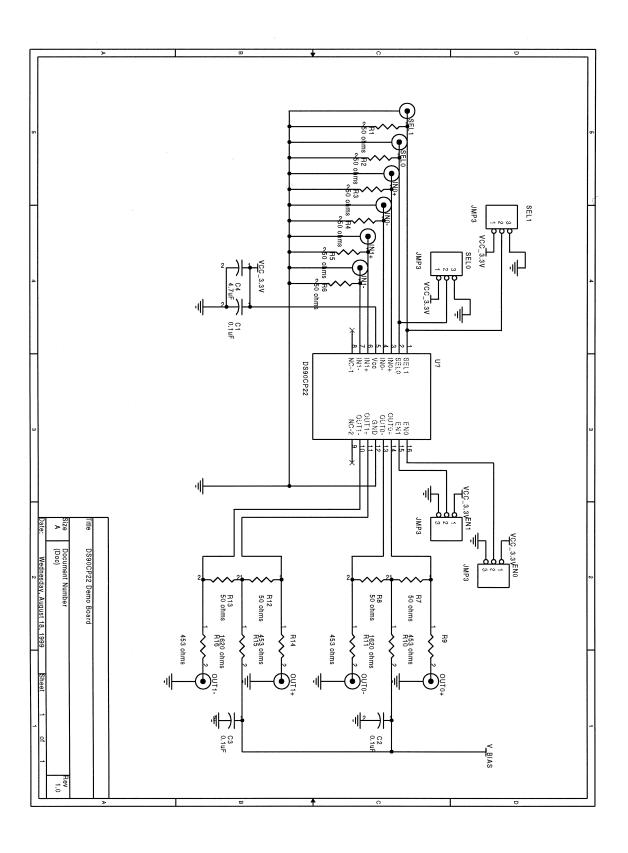
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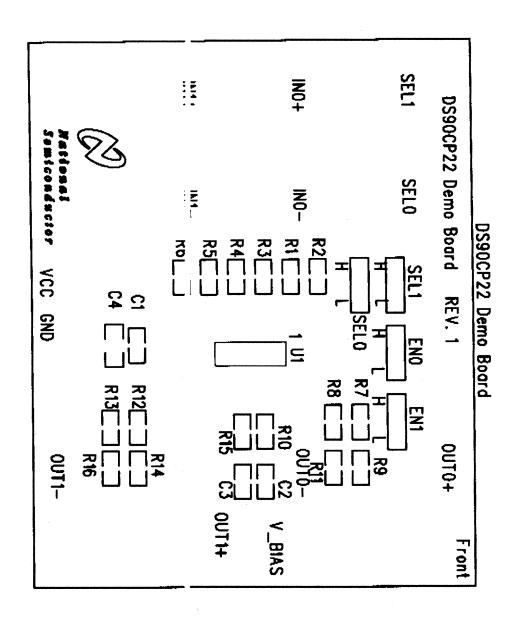
Do not attempt to measure only 1 channel by connecting only one driver's inputs and outputs. All inputs/outputs must be connected to either the signal generator or  $50\Omega$  sampling heads to insure proper measurements.



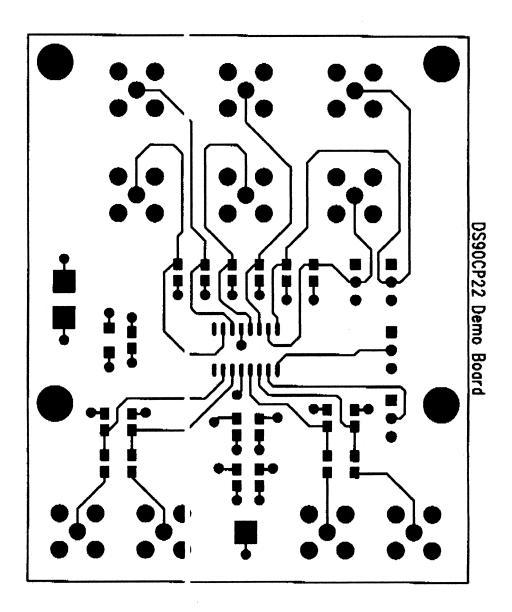
# **Bill of Materials**

	Labels	Value	Footprint
Resistors	R1,R2,R3,R4,R5,R6,R7,R8,R12,R13	50Ω	SMT-0805
	R10,R15	1.62ΚΩ	SMT-0805
	R9,R11,R14,R16	453Ω	SMT-0805
Capacitors	C1,C2,C3	0.1uF	SMT-0805
	C4	4.7uF	SMT-caseB
Connectors	SEL0,SEL1,IN0+,IN0-,IN1+,IN1-, OUT0+,OUT0-,OUT1+,OUT1-	Johnson Components: 142-0701-231	SMA Straight Receptacle
	SEL0,SEL1,EN0,EN1	3 Header Posts	0.1" spacing
	VCC,GND,V_BIAS	Power pads	1/8" square
Device	U1	DS90CP22	16L SOIC



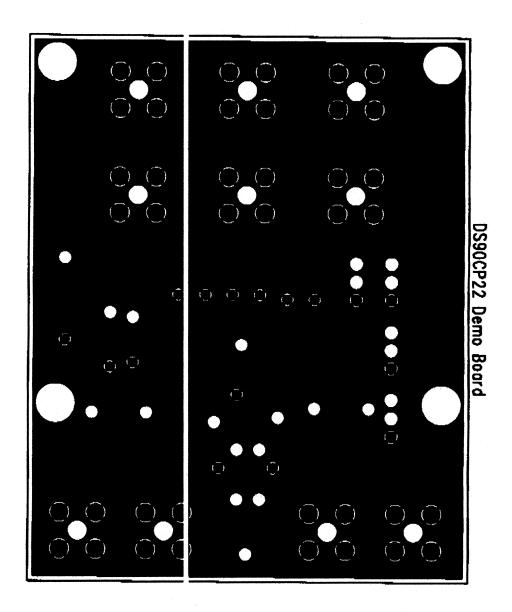


Layer: SILK

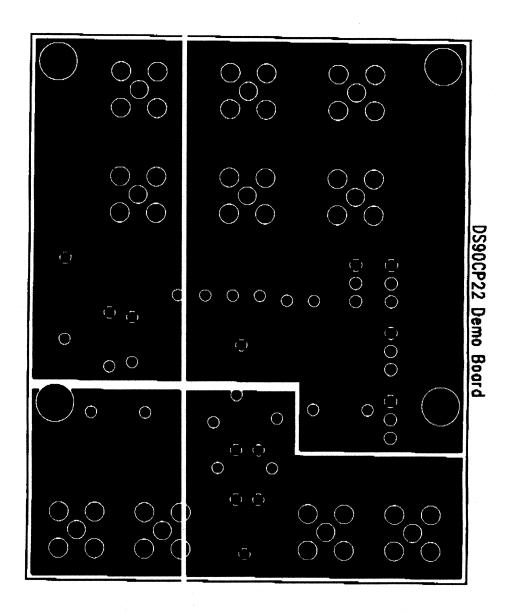


**Layer: TOP** 

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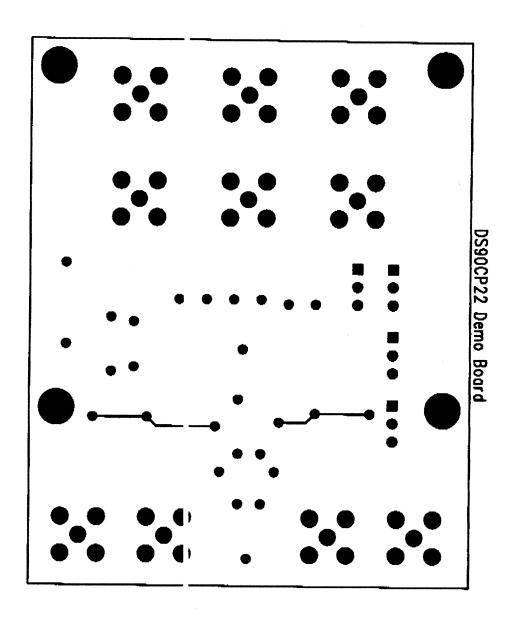


Layer: GND



**Layer: VCC** 

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**Layer: Bottom** 

# References & helpful hints:

For more information on LVDS, refer to the Datasheets and Application notes.

#### **Datasheets:**

DS90CP22 – 2x2 800Mbps LVDS Crosspoint Switch

#### **Application Notes:**

- An Overview of LVDS Technology: AN-971
- Low-Voltage Signal Yields Megatransfers per second with Milliwatts of Power: AN-1060
- Common Data Transmission Parameters and their Definitions: AN-912

Additional Information available on the Internet: http://www.national.com/appinfo/lvds

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