



LPC3130/3131

Low-cost, low-power ARM926EJ microcontrollers with USB
High-speed OTG, SD/MMC, and NAND flash controller

Rev. 0.12 — 19 December 2008

Preliminary data sheet

1. General description

FOR GUIDANCE ONLY.

THE CONTENTS OF THIS DATASHEET ARE SUBJECT TO CHANGE AND THEIR ACCURACY SHOULD NOT BE RELIED UPON.

TO ENSURE A DESIGN WITH THE LPC3130/31 IS BASED ON THE LATEST INFORMATION, PLEASE CAREFULLY CHECK ALL SPECIFICATIONS / FUNCTIONALITY PRIOR TO USE ONCE A VERSION OF THIS DATASHEET HAS BEEN ISSUED THAT DOES NOT CONTAIN THIS NOTICE

The NXP LPC3130/3131 combine an 180 MHz ARM926EJ-S CPU core, High Speed USB 2.0 OTG, up to 192 KB SRAM, NAND Flash Controller, flexible external bus interface, four channel 10-bit A/D, and a myriad of serial and parallel interfaces in a single chip targeted at consumer, industrial, medical, and communication markets. To optimize system power consumption, the LPC313x has multiple power domains and a very flexible Clock Generation Unit (CGU) that provides dynamic clock gating and scaling.

2. Features

2.1 Key features

- CPU platform
 - ◆ 180 MHz, 32-bit ARM926EJ-S
 - ◆ 16 kB D-cache and 16 kB I-cache
 - ◆ Memory Management Unit (MMU)
- Internal memory
 - ◆ 96 kB (LPC3130) or 192 kB (LPC3131) embedded SRAM
- External memory interface
 - ◆ NAND flash controller with 8-bit ECC
 - ◆ 8/16-bit Multi-Port Memory Controller (MPMC): SDRAM and SRAM
- Communication and connectivity
 - ◆ High-speed USB 2.0 (OTG, Host, Device) with on-chip PHY
 - ◆ Two I²S interfaces
 - ◆ Integrated master/slave SPI
 - ◆ Two master/slave I²C-bus interfaces
 - ◆ Fast UART
 - ◆ Memory Card Interface (MCI): MMC/SD/SDIO/CE-ATA
 - ◆ Four-channel 10-bit ADC

- ◆ Integrated 4/8/16-bit 6800/8080 compatible LCD interface
- System functions
 - ◆ Dynamic clock gating and scaling
 - ◆ Multiple power domains
 - ◆ Selectable boot-up: SPI flash, NAND flash, SD/MMC cards, UART, or USB
 - ◆ DMA controller
 - ◆ Four 32-bit timers
 - ◆ Watchdog timer
 - ◆ PWM module
 - ◆ Random Number Generator (RNG)
 - ◆ General Purpose I/O pins (GPIO)
 - ◆ Flexible and versatile interrupt structure
 - ◆ JTAG interface with boundary scan and ARM debug access
- Operating voltage and temperature
 - ◆ Core voltage: 1.2 V
 - ◆ I/O voltage: 1.8 V, 2.8 V, 3.3 V
 - ◆ Temperature: –40 °C to +85 °C
- TFBGA180 package: 12 x 12 mm², 0.8 mm pitch

3. Ordering information

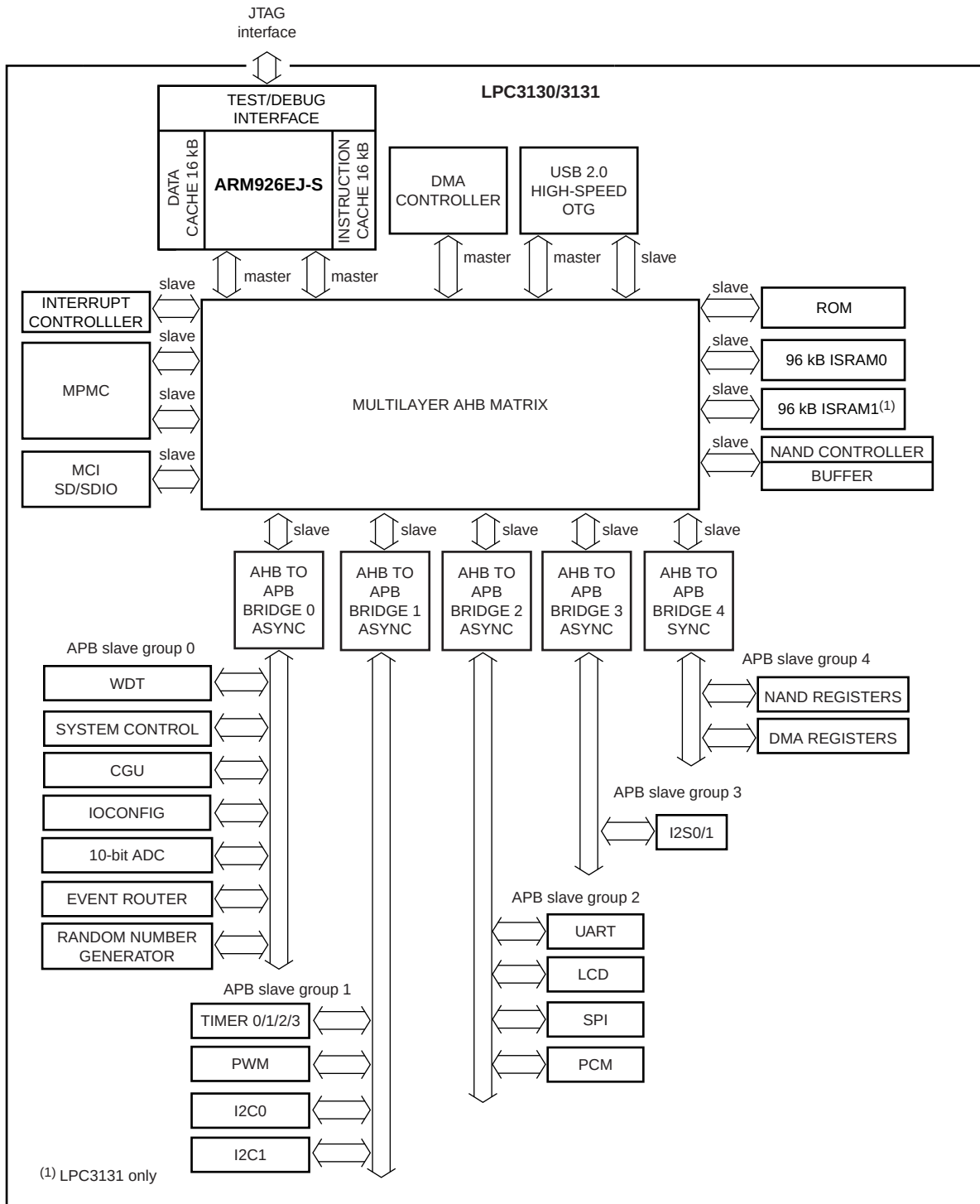
Table 1. Ordering information

Type number	Package		Version
	Name	Description	
LPC3130FET180	TFBGA180	Plastic thin fine pitch ball grid array package, 180 balls, body 12 x 12 x 0.8 mm	SOT570-3
LPC3131FET180	TFBGA180	Plastic thin fine pitch ball grid array package, 180 balls, body 12 x 12 x 0.8 mm	SOT570-3

Table 2. Ordering options for LPC3130/3131

Type number	Core/bus frequency	Total SRAM	High-speed USB	10-bit ADC channels	I ² S/I ² C -bus	MCI SDHC/SDIO/CE_ATA	Temperature range
LPC3130FET180	180 MHz/90 MHz	96 kB	Device/Host/OTG	4	2 each	yes	–40 °C to +85 °C
LPC3131FET180	180 MHz/90 MHz	192 kB	Device/Host/OTG	4	2 each	yes	–40 °C to +85 °C

4. Block diagram



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Fig 1. LPC3130/3131 block diagram

5. Pinning information

5.1 Pinning

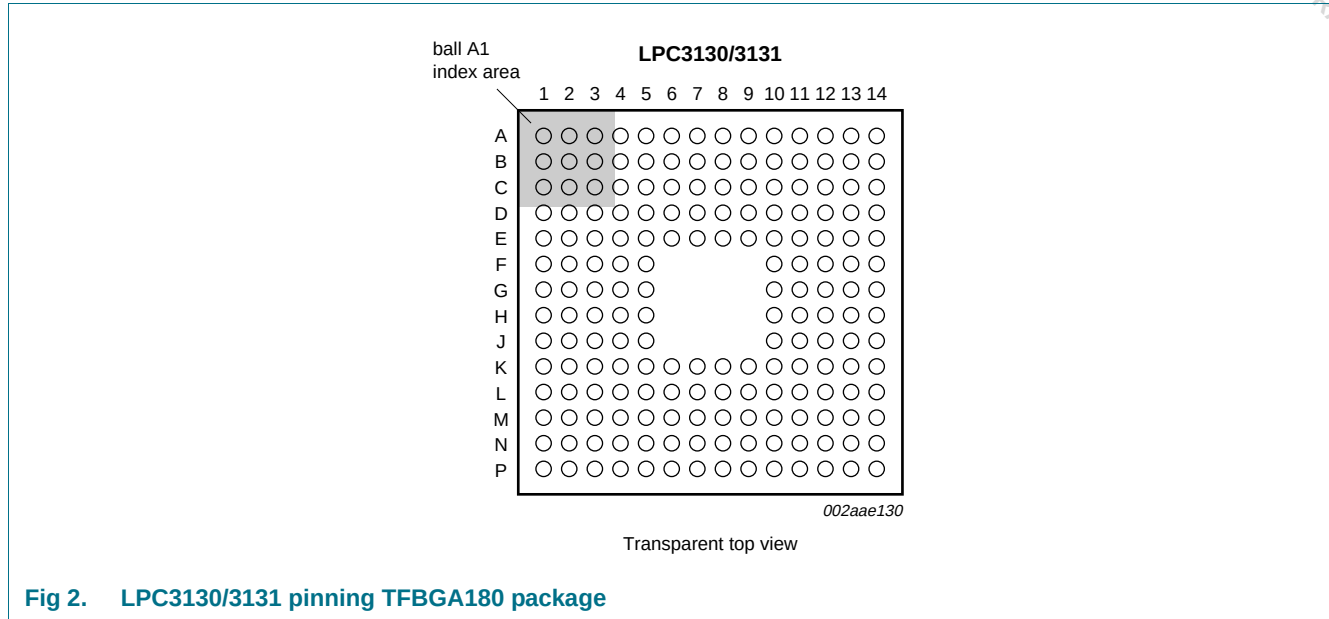


Fig 2. LPC3130/3131 pinning TFBGA180 package

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	EBI_D_10	2	EBI_A_1_CLE	3	EBI_D_9	4	mGPIO10
5	mGPIO7	6	mGPIO6	7	SPI_CS_OUT0	8	SPI_SCK
9	VDDI	10	FFAST_IN	11	VSSI	12	ADC10B_GNDA
13	ADC10B_VDDA33	14	ADC10B_GPA1	-	-	-	-
Row B							
1	EBI_D_8	2	VDDE_IOA	3	EBI_A_0_ALE	4	mNAND_RYBN2
5	mGPIO8	6	mGPIO5	7	SPI_MOSI	8	SPI_CS_IN
9	PWM_DATA	10	FFAST_OUT	11	GPIO3	12	VSSE_IOC
13	ADC10B_GPA2	14	ADC10B_GPA0	-	-	-	-
Row C							
1	EBI_D_7	2	EBI_D_11	3	VSSE_IOA	4	VSSE_IOA
5	mGPIO9	6	VDDI	7	VSSI	8	SPI_MISO
9	VDDI	10	I2C_SDA0	11	GPIO4	12	VDDI
13	VDDE_IOC	14	ADC10B_GPA3	-	-	-	-
Row D							
1	EBI_D_5	2	EBI_D_6	3	EBI_D_13	4	mNAND_RYBN3
5	VDDE_IOC	6	VSSE_IOC	7	VDDE_IOC	8	VSSE_IOC
9	VSSE_IOC	10	I2C_SCL0	11	VDDA12	12	VSSI
13	BUF_TCK	14	BUF_TMS	-	-	-	-

Table 3. Pin allocation table ...continued

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row E							
1	EBI_D_3	2	EBI_D_4	3	EBI_D_14	4	VSSE_IOA
5	VDDE_IOA	6	mNAND_RYBN0	7	mNAND_RYBN1	8	VDDE_IOC
9	VSSA12	10	VDDA12_B	11	ARM_TDO	12	I2C_SDA1
13	I2C_SCL1	14	I2STX_BCK1	-	-	-	-
Row F							
1	EBI_D_2	2	EBI_D_1	3	EBI_D_15	4	VSSE_IOA
5	VDDE_IOA	10	SCAN_TDO	11	BUF_TRST_N	12	I2STX_DATA1
13	I2SRX_WS1	14	I2SRX_BCK1	-	-	-	-
Row G							
1	EBI_NCAS_BLOUT_0	2	EBI_D_0	3	EBI_D_12	4	VSSI
5	VDDE_IOA	10	I2STX_WS1	11	VSSE_IOC	12	VDDE_IOC
13	SYSCLK_O	14	I2SRX_DATA1	-	-	-	-
Row H							
1	EBI_DQM_0_NOE	2	EBI_NRAS_BLOUT_1	3	VDDI	4	VSSE_IOA
5	VDDE_IOA	10	GPIO12	11	GPIO19	12	CLK_256FS_0
13	GPIO11	14	RSTIN_N_I	-	-	-	-
Row J							
1	NAND_NCS_0	2	EBI_NWE	3	NAND_NCS_1	4	CLOCK_OUT
5	USB_RREF	10	GPIO1	11	GPIO16	12	GPIO13
13	GPIO15	14	GPIO14	-	-	-	-
Row K							
1	NAND_NCS_2	2	NAND_NCS_3	3	VSSE_IOA	4	USB_VSSA_REF
5	mLCD_DB_12	6	mLCD_DB_6	7	mLCD_DB_10	8	mLCD_CSB
9	TDI	10	GPIO0	11	VDDE_ESD	12	GPIO17
13	GPIO20	14	GPIO18	-	-	-	-
Row L							
1	USB_VDDA12_PLL	2	USB_VBUS	3	USB_VSSA_TERM	4	VDDE_IOB
5	mLCD_DB_9	6	VSSI	7	VDDI	8	mLCD_E_RD
9	VSSE_IOC	10	VDDE_IOC	11	VSSI	12	VDDI
13	VSSE_IOC	14	GPIO2	-	-	-	-
Row M							
1	USB_ID	2	USB_VDA33_DRV	3	VSSE_IOB	4	VSSE_IOB
5	VDDE_IOB	6	VSSE_IOB	7	VDDE_IOB	8	VSSE_IOB
9	VDDE_IOB	10	I2SRX_DATA0	11	mI2STX_WS0	12	mI2STX_BCK0
13	mI2STX_DATA0	14	TCK	-	-	-	-
Row N							
1	USB_GNDA	2	USB_DM	3	mLCD_DB_15	4	mLCD_DB_11
5	mLCD_DB_8	6	mLCD_DB_2	7	mLCD_DB_4	8	mLCD_DB_0
9	mLCD_RW_WR	10	I2SRX_BCK0	11	JTAGSEL	12	UART_TXD
13	mUART_CTS_N	14	mI2STX_CLK0	-	-	-	-

Table 3. Pin allocation table ...continued

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row P							
1	USB_VDDA33	2	USB_DP	3	mLCD_DB_14	4	mLCD_DB_13
5	mLCD_DB_7	6	mLCD_DB_3	7	mLCD_DB_5	8	mLCD_RS
9	mLCD_DB_1	10	TMS	11	I2SRX_WS0	12	UART_RXD
13	TRST_N	14	mUART_RTS_N	-	-	-	-

Table 4. Pin description

Pin names with prefix *m* are multiplexed pins. See [Table 10](#) for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset	Cell Type [2]	Description
Clock Generation Unit						
FFAST_IN	A10	SUP1	AI	-	AIO2	12 MHz oscillator clock input
FFAST_OUT	B10	SUP1	AO		AIO2	12 MHz oscillator clock output
VDDA12	D11; E10	SUP1	Supply		PS3	12 MHz oscillator/PLLs Analog supply
VSSA12	E9		Ground	-	CG1	12 MHz oscillator/PLLs Analog ground
RSTIN_N	H14	SUP3	DI	I	DIO2	System Reset Input (active low)
CLK_256FS_O	H12	SUP3	DO	O	DIO1	Programmable clock output; fractionally derived from CLK1024FS_BASE clock domain. Generally used for Audio Codec master clock.
CLOCK_OUT	J4	SUP3	DO	O	DIO1	Programmable clock output; fractionally derived from SYS_BASE clock domain.
SYSCLK_O[3]	G13	SUP3	DO	O	DIO1	Programmable clock output. Output one of seven base/reference input clocks. No fractional divider.
10-bit ADC						
ADC10B_VDDA33	A13	SUP3	Supply	-	PS3	10-bit ADC Analog Supply
ADC10B_GNDA	A12		Ground	-	CG1	10-bit ADC Analog Ground
ADC10B_GPA0	B14	SUP3	AI	-	AIO1	10-bit ADC Analog Input
ADC10B_GPA1	A14	SUP3	AI	-	AIO1	10-bit ADC Analog Input
ADC10B_GPA2	B13	SUP3	AI	-	AIO1	10-bit ADC Analog Input
ADC10B_GPA3	C14	SUP3	AI	-	AIO1	10-bit ADC Analog Input
USB HS 2.0 OTG						
USB_VBUS	L2	SUP5	AI	-	AIO3	USB supply detection line
USB_ID	M1	SUP3	AI	-	AIO1	Indicates to the USB transceiver whether in device (USB_ID high) or host (USB_ID low) mode (contains internal pull-up resistor)
USB_RREF	J5	SUP3	AIO	-	AIO1	USB Connection for external reference resistor (12 kΩ +/- 1%) to analog ground supply
USB_DP	P2	SUP3	AIO	-	AIO1	USB D+ connection with integrated 45 Ohm termination resistor
USB_DM	N2	SUP3	AIO	-	AIO1	USB D- connection with integrated 45 Ohm termination resistor

Table 4. Pin description

Pin names with prefix *m* are multiplexed pins. See [Table 10](#) for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset	Cell Type [2]	Description
USB_VDDA12_PLL	L1	SUP1	Supply	-	PS3	USB PLL supply
USB_VDDA33_DRV	M2	SUP3	Supply	-	PS3	USB Analog supply for driver
USB_VDDA33	P1	SUP3	Supply	-	PS3	USB Analog supply for PHY
USB_VSSA_TERM	L3		Ground	-	CG1	USB Analog ground for clean reference for on chip termination resistors
USB_GNDA	N1		Ground	-	CG1	USB Analog ground
USB_VSSA_REF	K4		Ground	-	CG1	USB Analog ground for clean reference
JTAG						
JTAGSEL	N11	SUP3	DI	I	DIO1	JTAG selection. Controls output function of SCAN_TDO and ARM_TDO signals.
TDI	K9	SUP3	DI	I	DIO1	JTAG Data Input
TRST_N	P13	SUP3	DI	I	DIO1	JTAG Reset Input
TCK	M14	SUP3	DI	I	DIO1	JTAG Clock Input
TMS	P10	SUP3	DI	I	DIO1	JTAG Mode Select Input
SCAN_TDO	F10	SUP3	DO	O/Z	DIO1	JTAG TDO signal from scan TAP controller. Pin state is controlled by JTAGSEL.
ARM_TDO	E11	SUP3	DO	O	DIO1	JTAG TDO signal from ARM926 TAP controller.
BUF_TRST_N	F11	SUP3	DO	O	DIO1	Buffered TRST_N out signal. Used for connecting an on board TAP controller (FPGA, DSP, etc.).
BUF_TCK	D13	SUP3	DO	O	DIO1	Buffered TCK out signal. Used for connecting an on board TAP controller (FPGA, DSP, etc.).
BUF_TMS	D14	SUP3	DO	O	DIO1	Buffered TMS out signal. used for connecting an on board TAP controller (FPGA, DSP, etc.).
UART						
mUART_CTS_N [3][4]	N13	SUP3	DI / GPIO	I	DIO1	UART Clear To Send (active low)
mUART_RTS_N [3][4]	P14	SUP3	DO / GPIO	O	DIO1	UART Ready To Send (active low)
UART_RXD [3]	P12	SUP3	DI / GPIO	I	DIO1	UART Serial Input
UART_TXD [3]	N12	SUP3	DO / GPIO	O	DIO1	UART Serial Output
I²C master/slave interface						
I ² C_SDA0	C10	SUP3	DIO	I	IICD	I ² C Data Line
I ² C_SCL0	D10	SUP3	DIO	I	IICC	I ² C Clock line
I ² C_SDA1 [3]	E12	SUP3	DIO	O	DIO1	I ² C Data Line
I ² C_SCL1 [3]	E13	SUP3	DIO	O	DIO1	I ² C Clock line
Serial Peripheral Interface						
SPI_CS_OUT0 [3]	A7	SUP3	DO	O	DIO4	SPI Chip Select Output (Master)
SPI_SCK [3]	A8	SUP3	DIO	I	DIO4	SPI Clock Input (Slave) / Clock Output (Master)
SPI_MISO [3]	C8	SUP3	DIO	I	DIO4	SPI Data Input (Master) / Data Output (Slave)

Table 4. Pin description

Pin names with prefix *m* are multiplexed pins. See [Table 10](#) for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset	Cell Type [2]	Description
SPI_MOSI [3]	B7	SUP3	DIO	I	DIO4	SPI Data Output (Master) / Data Input (Slave)
SPI_CS_IN [3]	B8	SUP3	DI	I	DIO4	SPI Chip Select Input (Slave)
Digital power supply						
VDDI	H3; L7; L12; C12; C6	SUP1	Supply	-	CS2	Digital Core Supply
VSSI	A11; C7; D12; G4; L6; L11		Ground	-	CG2	Digital Core Ground
Peripheral power supply						
VDDE_IOA	B2; E5; F5; G5; H5	SUP4	Supply	-	PS1	Peripheral supply for NAND flash interface
VDDE_IOB	L4; M5; M7; M9	SUP8	Supply	-	PS1	Peripheral supply for SDRAM/LCD
VDDE_IOC	C13; D5; D7; E8; G12; L10;	SUP3	Supply	-	PS1	Peripheral supply
VDDE_ESD	K11	SUP8	Supply	-	PS1	
VSSE_IOA	C3; C4; E4; F4; H4; K3		Ground	-	PG1	
VSSE_IOB	M3; M4; M6; M8		Ground	-	PG1	

Table 4. Pin description

Pin names with prefix *m* are multiplexed pins. See [Table 10](#) for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset	Cell Type [2]	Description
VSSE_IOC	B12; D6; D8; D9; G11; L9; L13		Ground	-	PG1	
LCD Interface						
mLCD_CSB [3]	K8	SUP8	DO	O	DIO4	LCD Chip Select (active low)
mLCD_E_RD [3]	L8	SUP8	DO	O	DIO4	LCD, 6800 Enable, 8080 Read Enable (active high)
mLCD_RS [3]	P8	SUP8	DO	O	DIO4	LCD, Instruction Register ('low')/ Data Register ('high') select
mLCD_RW_WR [3]	N9	SUP8	DO	O	DIO4	LCD, 6800 Read/write Select, 8080 Write Enable (active high)
mLCD_DB_0 [3]	N8	SUP8	DIO	O	DIO4	LCD Data 0
mLCD_DB_1 [3]	P9	SUP8	DIO	O	DIO4	LCD Data 1
mLCD_DB_2 [3]	N6	SUP8	DIO	O	DIO4	LCD Data 2
mLCD_DB_3 [3]	P6	SUP8	DIO	O	DIO4	LCD Data 3
mLCD_DB_4 [3]	N7	SUP8	DIO	O	DIO4	LCD Data 4
mLCD_DB_5 [3]	P7	SUP8	DIO	O	DIO4	LCD Data 5
mLCD_DB_6 [3]	K6	SUP8	DIO	O	DIO4	LCD Data 6
mLCD_DB_7 [3]	P5	SUP8	DIO	O	DIO4	LCD Data 7
mLCD_DB_8 [3]	N5	SUP8	DIO	O	DIO4	LCD Data 8 / 8-bit Data 0
mLCD_DB_9 [3]	L5	SUP8	DIO	O	DIO4	LCD Data 9 / 8-bit Data 1
mLCD_DB_10 [3]	K7	SUP8	DIO	O	DIO4	LCD Data 10 / 8-bit Data 2
mLCD_DB_11 [3]	N4	SUP8	DIO	O	DIO4	LCD Data 11 / 8-bit Data 3
mLCD_DB_12 [3]	K5	SUP8	DIO	O	DIO4	LCD Data 12 / 8-bit Data 4 / 4-bit Data 0
mLCD_DB_13 [3]	P4	SUP8	DIO	O	DIO4	LCD Data 13 / 8-bit Data 5 / 4-bit Data 1 / Serial Clock Output
mLCD_DB_14 [3]	P3	SUP8	DIO	O	DIO4	LCD Data 14 / 8-bit Data 6 / 4-bit Data 2 / Serial Data Input
mLCD_DB_15 [3]	N3	SUP8	DIO	O	DIO4	LCD Data 15 / 8-bit Data 7 / 4-bit Data 3 / Serial Data Output

Table 4. Pin description

Pin names with prefix *m* are multiplexed pins. See [Table 10](#) for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level [1]	Application function	Pin state after reset	Cell Type [2]	Description
I²S/Digital Audio Input						
I2SRX_DATA0 [3]	M10	SUP3	DI / GPIO	I	DIO1	I2S Serial Data Receive Input
I2SRX_DATA1 [3]	G14	SUP3	DI / GPIO	I	DIO1	I2S Serial Data Receive Input
I2SRX_BCK0 [3]	N10	SUP3	DIO / GPIO	I	DIO1	I2S Bitclock
I2SRX_BCK1 [3]	F14	SUP3	DIO / GPIO	I	DIO1	I2S Bitclock
I2SRX_WS0 [3]	P11	SUP3	DIO / GPIO	I	DIO1	I2S Word select
I2SRX_WS1 [3]	F13	SUP3	DIO / GPIO	I	DIO1	I2S Word select
I²S/Digital Audio Output						
mI2STX_DATA0 [3]	M13	SUP3	DO / GPIO	O	DIO1	I2S Serial Data Transmit Output
mI2STX_BCK0 [3]	M12	SUP3	DO / GPIO	O	DIO1	I2S Bitclock
mI2STX_WS0 [3]	M11	SUP3	DO / GPIO	O	DIO1	I2S Word select
mI2STX_CLK0 [3]	N14	SUP3	DO / GPIO	O	DIO1	I2S Serial Clock
I2STX_DATA1 [3]	F12	SUP3	DO / GPIO	O	DIO1	I2S Serial Data Transmit Output
I2STX_BCK1 [3]	E14	SUP3	DO / GPIO	O	DIO1	I2S Bitclock
I2STX_WS1 [3]	G10	SUP3	DO / GPIO	O	DIO1	I2S Word select
General Purpose IO (IOConf module)						
GPIO0	K10	SUP3	GPIO	I	DIO1	General Purpose IO Pin 0 (Mode pin 0)
GPIO1	J10	SUP3	GPIO	I	DIO1	General Purpose IO Pin 1 (Mode pin 1)
GPIO2	L14	SUP3	GPIO	I	DIO1	General Purpose IO Pin 2 (Mode pin 2)
GPIO3	B11	SUP3	GPIO	I	DIO1	General Purpose IO Pin 3
GPIO4	C11	SUP3	GPI	I	DIO1	General Purpose Input Pin 4
mGPIO5 [3]	B6	SUP3	GPIO	I	DIO4	General Purpose IO Pin 5
mGPIO6 [3]	A6	SUP3	GPIO	I	DIO4	General Purpose IO Pin 6
mGPIO7 [3]	A5	SUP3	GPIO	I	DIO4	General Purpose IO Pin 7
mGPIO8 [3]	B5	SUP3	GPIO	I	DIO4	General Purpose IO Pin 8
mGPIO9 [3]	C5	SUP3	GPIO	I	DIO4	General Purpose IO Pin 9
mGPIO10 [3]	A4	SUP3	GPIO	I	DIO4	General Purpose IO Pin 10
GPIO11	H13	SUP3	GPIO	I	DIO1	General Purpose IO Pin 11
GPIO12	H10	SUP3	GPIO	I	DIO1	General Purpose IO Pin 12
GPIO13	J12	SUP3	GPIO	I	DIO1	General Purpose IO Pin 13
GPIO14	J14	SUP3	GPIO	I	DIO1	General Purpose IO Pin 14
GPIO15	J13	SUP3	GPIO	I	DIO1	General Purpose IO Pin 15
GPIO16	J11	SUP3	GPIO	I	DIO1	General Purpose IO Pin 16
GPIO17	K12	SUP3	GPIO	I	DIO1	General Purpose IO Pin 17
GPIO18	K14	SUP3	GPIO	I	DIO1	General Purpose IO Pin 18
GPIO19	H11	SUP3	GPIO	I	DIO1	General Purpose IO Pin 19
GPIO20	K13	SUP3	GPIO	I	DIO1	General Purpose IO Pin 20

Table 4. Pin description

Pin names with prefix *m* are multiplexed pins. See [Table 10](#) for pin function selection of multiplexed pins.

Pin name	BGA Ball	Digital I/O level ^[1]	Application function	Pin state after reset	Cell Type ^[2]	Description
External Bus Interface (NAND flash controller)						
EBI_A_0_ALE ^[3]	B3	SUP4	DO	O	DIO4	EBI Address Latch Enable
EBI_A_1_CLE ^[3]	A2	SUP4	DO	O	DIO4	EBI Command Latch Enable
EBI_D_0 ^[3]	G2	SUP4	DIO	I	DIO4	EBI Data I/O 0
EBI_D_1 ^[3]	F2	SUP4	DIO	I	DIO4	EBI Data I/O 1
EBI_D_2 ^[3]	F1	SUP4	DIO	I	DIO4	EBI Data I/O 2
EBI_D_3 ^[3]	E1	SUP4	DIO	I	DIO4	EBI Data I/O 3
EBI_D_4 ^[3]	E2	SUP4	DIO	I	DIO4	EBI Data I/O 4
EBI_D_5 ^[3]	D1	SUP4	DIO	I	DIO4	EBI Data I/O 5
EBI_D_6 ^[3]	D2	SUP4	DIO	I	DIO4	EBI Data I/O 6
EBI_D_7 ^[3]	C1	SUP4	DIO	I	DIO4	EBI Data I/O 7
EBI_D_8 ^[3]	B1	SUP4	DIO	I	DIO4	EBI Data I/O 8
EBI_D_9 ^[3]	A3	SUP4	DIO	I	DIO4	EBI Data I/O 9
EBI_D_10 ^[3]	A1	SUP4	DIO	I	DIO4	EBI Data I/O 10
EBI_D_11 ^[3]	C2	SUP4	DIO	I	DIO4	EBI Data I/O 11
EBI_D_12 ^[3]	G3	SUP4	DIO	I	DIO4	EBI Data I/O 12
EBI_D_13 ^[3]	D3	SUP4	DIO	I	DIO4	EBI Data I/O 13
EBI_D_14 ^[3]	E3	SUP4	DIO	I	DIO4	EBI Data I/O 14
EBI_D_15 ^[3]	F3	SUP4	DIO	I	DIO4	EBI Data I/O 15
EBI_DQM_0_NOE ^[3]	H1	SUP4	DO	O	DIO4	NAND Read Enable (active low)
EBI_NWE ^[3]	J2	SUP4	DO	O	DIO4	NAND Write Enable (active low)
NAND_NCS_0 ^[3]	J1	SUP4	DO	O	DIO4	NAND Chip Enable 0
NAND_NCS_1 ^[3]	J3	SUP4	DO	O	DIO4	NAND Chip Enable 1
NAND_NCS_2 ^[3]	K1	SUP4	DO	O	DIO4	NAND Chip Enable 2
NAND_NCS_3 ^[3]	K2	SUP4	DO	O	DIO4	NAND Chip Enable 3
mNAND_RYBN0 ^[3]	E6	SUP4	DI	I	DIO4	NAND Ready/Busy 0
mNAND_RYBN1 ^[3]	E7	SUP4	DI	I	DIO4	NAND Ready/Busy 1
mNAND_RYBN2 ^[3]	B4	SUP4	DI	I	DIO4	NAND Ready/Busy 2
mNAND_RYBN3 ^[3]	D4	SUP4	DI	I	DIO4	NAND Ready/Busy 3
EBI_NCAS_BLOUT_0 ^[3]	G1	SUP4	DO	O	DIO4	EBI Lower lane byte select (7:0)
EBI_NRAS_BLOUT_1 ^[3]	H2	SUP4	DO	O	DIO4	EBI Upper lane byte select (15:8)
Pulse Width Modulation module						
PWM_DATA ^[3]	B9	SUP3	DO / GPIO	O	DIO1	PWM Output

[1] Digital IO levels are explained in [Table 5](#).

[2] Cell types are explained in [Table 6](#).

[3] Pin can be configured as GPIO pin in the IOCONFIG block.

[4] The UART flow control lines (mUART_CTS_N and mUART_RTS_N) are multiplexed. This means that if these balls are not required for UART flow control, they can also be selected to be used for an alternative function: SPI chip select signals (SPI_CS_OUT1 and SPI_CS_OUT2)

Table 5. Supply domains

Supply Domain	Voltage range	Related supply pins	Description
SUP1	1.0 V– 1.3 V	VDDI, VDDA12, USB_VDDA12_PLL,	Digital core supply
SUP3	2.7 V - 3.3 V	VDDE_IOC, ADC10B_VDDA33, USB_VDDA33_DRV, USB_VDDA33,	Peripheral supply
SUP4	1.65 V - 1.95 V (in 1.8 V mode) 2.5 V - 3.1 V (in 2.8 V mode)	VDDE_IOA	Peripheral supply for NAND flash interface
SUP5	4.5 V– 5.5 V	USB_VBUS	USB VBUS voltage
SUP8	1.65 V - 1.95 V (in 1.8 V mode) 2.5 V - 3.1 V (in 2.8 V mode)	VDDE_IOB	Peripheral supply for SDRAM/SRAM/bus-based LCD [1]

[1] When the SDRAM is used, the supply voltage of the NAND flash, SDRAM, and the LCD Interface must be the same, i.e. SUP4 and SUP8 should be connected to the same rail. (See also [Section 6.26.3](#).)

Table 6: I/O pads

Cell type	Pad type	Function	Description
DIO1	bspts3chp	Digital Input/Output	Bi-directional 3.3 V; 3-state Output; 3 ns Slew Rate Control; Plain Input; CMOS with Hysteresis; Programmable Pull Up, Pull Down, Repeater
DIO2	bpts5pcph	Digital Input/Output	Bi-directional 5 V; Plain Input; 3state Output; CMOS with Programmable Hysteresis; Programmable Pull Up, Pull Down, Repeater
DIO4	mem1 bsptz40pchp	Digital Input/Output	Bi-directional 1.8 V or 2.8 V; Plain Input; 3state Output; Programmable Hysteresis; Programmable Pull Up, Pull Down, Repeater
IICC	iic3m4scl	Digital Input/Output	IIC; Clock Signal
IICD	iic3mvsda	Digital Input/Output	IIC; Data Signal
AIO1	apio3v3	Analog Input/Output	Analog Input Output; Protection to external 3.3 V Supply Rail
AIO2	apio	Analog Input/Output	Analog Input Output
AIO3	apiot5v	Analog Input/Output	Analog Input Output; 5 V Tolerant Pad-based ESD Protection
CS1	vddco	Core Supply	-
CS2	vddi	Core Supply	-
PS1	vdde3v3	Peripheral Supply	-
PS2	vdde	Peripheral Supply	-
CG1	vssco	Core Ground	-
CG2	vssis	Core Ground	-
PG1	vsse	Peripheral Ground	-

6. Functional description

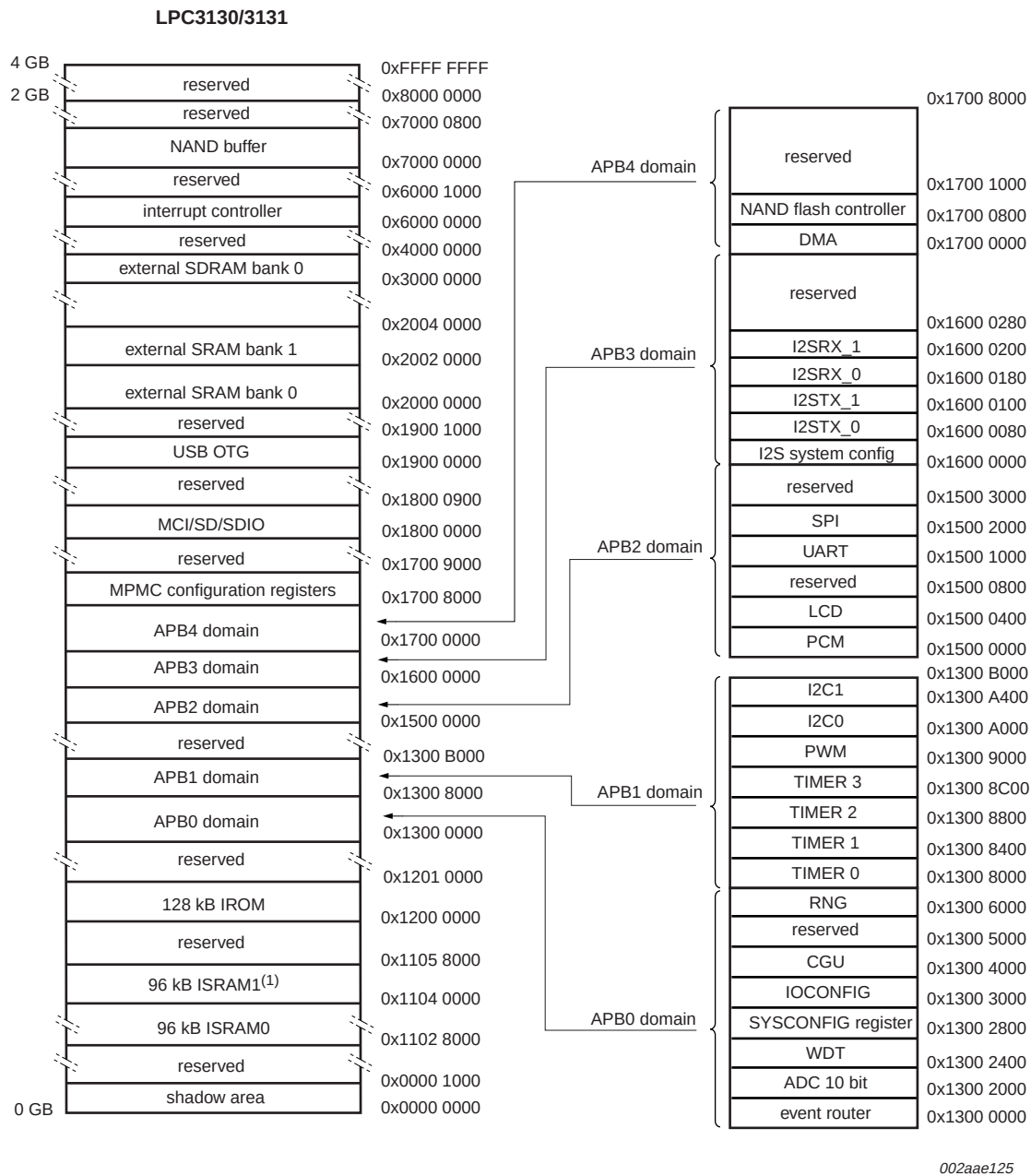
6.1 ARM926EJ-S

The processor embedded in the LPC3130/3131 is the ARM926EJ-S. It is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S is intended for multi-tasking applications where full memory management, high performance, and low power are important.

This module has the following features:

- ARM926EJ-S processor core which uses a five-stage pipeline consisting of fetch, decode, execute, memory, and write stages. The processor supports both the 32-bit ARM and 16-bit Thumb instruction sets, which allows a trade off between high performance and high code density. The ARM926EJ-S also executes an extended ARMv5TE instruction set which includes support for Java byte code execution.
- Contains an AMBA BIU for both data accesses and instruction fetches.
- Memory Management Unit (MMU).
- 16 kB instruction and 16 kB data separate cache memories with an 8 word line length. The caches are organized using Harvard architecture.
- Little Endian is supported.
- The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debugging.
- Supports dynamic clock gating for power reduction.
- The processor core clock can be set equal to the AHB bus clock or to an integer number times the AHB bus clock. The processor can be switched dynamically between these settings.
- ARM stall support.

6.2 Memory map



(1) LPC3131 only.

Fig 3. LPC3130/3131 memory map

6.3 JTAG

The Joint Test Action Group (JTAG) interface allows the incorporation of the LPC3130/3131 in a JTAG scan chain.

This module has the following features:

- ARM926 debug access
- Boundary scan

6.4 NAND flash controller

The NAND flash Controller is used as a dedicated interface to NAND flash devices. [Figure 4](#) shows a block diagram of the NAND flash controller module. The heart of the module is formed by a controller block that controls the flow of data from/to the AHB bus through the NAND flash controller block to/from the (external) NAND flash. An error correction encoder/decoder (ECC enc/dec) module allows for hardware error correction for support of Multi-Level Cell (MLC) NAND flash devices.

Before data is written from the buffer to the NAND flash, optionally it is first protected by an error correction code generated by the ECC module. After data is read from the NAND flash, the error correction module corrects any errors.

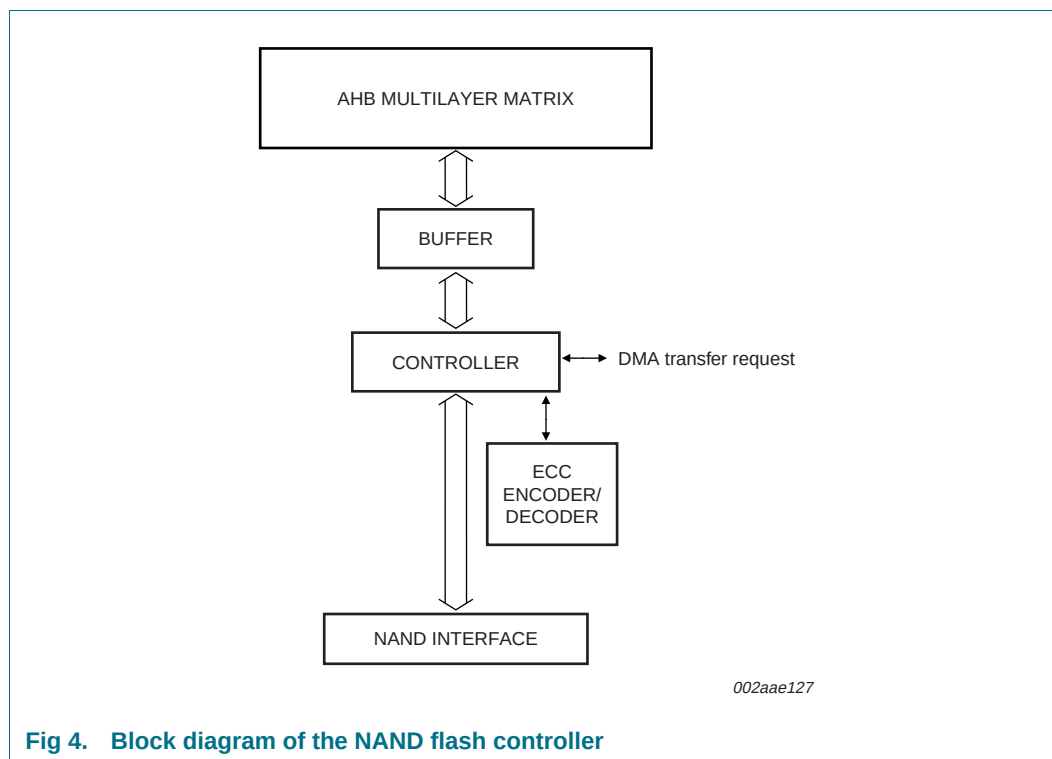


Fig 4. Block diagram of the NAND flash controller

This module has the following features:

- Dedicated NAND flash interface with hardware controlled read and write accesses.
- Wear leveling support with 516 byte mode.
- Software controlled command and address transfers to support wide range of flash devices.

- Software control mode where the ARM is directly master of the flash device.
- Support for 8 bit and 16 bit flash devices.
- Support for any page size from 0.5 kB upwards.
- Programmable NAND flash timing parameters.
- Support for up to 4 NAND devices.
- Error Correction Module (ECC) for MLC NAND flash support:
 - Reed-Solomon error correction encoding and decoding.
 - Uses Reed-Solomon code words with 9-bit symbols over GF(2⁹), a total codeword length of 469 symbols, including 10 parity symbols, giving a minimum Hamming distance of 11.
 - Up to 8 symbol errors can be corrected per codeword.
 - Error correction can be turned on and off to match the demands of the application.
 - Parity generator for error correction encoding.
 - Wear leveling information can be integrated into protected data.
 - Interrupts generated after completion of error correction task with 3 interrupt registers.
 - Error correction statistics distributed to ARM using interrupt scheme.
 - Interface is compatible with the ARM External Bus Interface (EBI).

6.5 Multi-Port Memory Controller (MPMC)

The multi-port memory controller supports the interface to different memory types, for example:

- SDRAM
- Low-power SDRAM
- Static memory interface

This module has the following features:

- Dynamic memory interface support including SDRAM, JEDEC low-power SDRAM.
- Address line supporting up to 64 MB of dynamic memory.
- The MPMC has two AHB interfaces:
 - a. an interface for accessing external memory.
 - b. a separate control interface to program the MPMC. This enables the MPMC registers to be situated in memory with other system peripheral registers.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance, particularly for un-cached processors.
- Static memory features include:
 - asynchronous page mode read
 - programmable wait states
 - bus turnaround delay
 - output enable and write enable delays

- extended wait
- One chip select for synchronous memory and two chip selects for static memory devices.
- Power-saving modes.
- Dynamic memory self-refresh mode supported.
- Controller support for 2K, 4K, and 8K row address synchronous memory parts.
- Support for all AHB burst types.
- Little and big-endian support.
- Support for the External Bus Interface (EBI) that enables the memory controller pads to be shared.

6.6 External Bus Interface (EBI)

The EBI module acts as multiplexer with arbitration between the NAND flash and the SDRAM/SRAM memory modules connected externally through the MPMC.

The main purpose for using the EBI module is to save external pins. However only data and address pins are multiplexed. Control signals towards and from the external memory devices are not multiplexed.

Table 7. Memory map of the external SRAM/SDRAM memory modules

Module	Maximum address space		Data width	Device size
External SRAM0	0x2000 0000	0x2000 FFFF	8 bit	64 kB
	0x2000 0000	0x2001 FFFF	16 bit	128 kB
External SRAM1	0x2002 0000	0x2002 FFFF	8 bit	64 kB
	0x2002 0000	0x2003 FFFF	16 bit	128 kB
External SDRAM0	0x3000 0000	0x33FF FFFF	16 bit	64 MB

6.7 Internal ROM Memory

The internal ROM memory is used to store the boot code of the LPC3130/3131. After a reset, the ARM processor will start its code execution from this memory.

The LPC3130/3131 ROM memory has the following features:

- Supports booting from SPI flash, NAND flash, SD/SDHC/MMC cards, UART, and USB (DFU class) interfaces.
- Supports option to perform CRC32 checking on the boot image.
- Supports booting from managed NAND devices such as moviNAND, iNAND, eMMC-NAND and eSD-NAND using SD/MMC boot mode.
- Contains pre-defined MMU table (16 kB) for simple systems.

The boot ROM determines the boot mode based on reset state of GPIO0, GPIO1, and GPIO2 pins. [Table 8](#) shows the various boot modes supported on the LPC3130/3131:

Table 8. LPC3130/3131 boot modes

Boot mode	GPIO0	GPIO1	GPIO2	Description
NAND	0	0	0	Boots from NAND flash. If proper image is not found, boot ROM will switch to DFU boot mode.
SPI	0	0	1	Boot from SPI NOR flash connected to SPI_CS_OUT0. If proper image is not found, boot ROM will switch to DFU boot mode.
DFU	0	1	0	Device boots via USB using DFU class specification.
SD/MMC	0	1	1	Boot ROM searches all the partitions on the SD/MMC/SDHC/MMC+/eMMC/eSD card for boot image. If partition table is missing, it will start searching from sector 0. A valid image is said to be found if a valid image header is found, followed by a valid image. If a proper image is not found, boot ROM will switch to DFU boot mode.
Reserved 0	1	0	0	Reserved for testing.
NOR flash	1	0	1	Boot from parallel NOR flash connected to EBI_NSTCS_1.
UART	1	1	0	Boot ROM tries to download boot image from UART ((115200 – 8 – n -1) assuming 12MHz FFAST clock).
Test	1	1	1	Boot ROM is testing ISRAM using memory pattern test. After test switches to UART boot mode.

6.8 Internal RAM memory

The ISRAM (Internal Static Memory Controller) module is used as controller between the AHB bus and the internal RAM memory. The internal RAM memory can be used as working memory for the ARM processor and as temporary storage to execute the code that is loaded by boot ROM from external devices such as SPI-flash, NAND flash, and SD/MMC cards.

This module has the following features:

- Capacity of 96 kB (LPC3130) or 192 kB (LPC3131)
- On LPC3131 implemented as two independent 96 kB memory banks

6.9 Memory Card Interface (MCI)

The MCI controller interface can be used to access memory cards according to the Secure Digital (SD) and Multi-Media Card (MMC) standards. The host controller can be used to interface to small form factor expansion cards compliant to the SDIO card standard as well. Finally, the MCI supports CE ATA 1.1 compliant hard disk drives.

This module has the following features:

- One 8-bit wide interface.
- Supports high-speed SD, versions 1.01, 1.10 and 2.0.
- Supports SDIO version 1.10.
- Supports MMCplus, MMCmobile and MMCmicro cards based on MMC 4.1.
- Supports SDHC memory cards.
- CRC generation and checking.

- Supports 1/4-bit SD cards.
- Card detection and write protection.
- FIFO buffers of 16 bytes deep.
- Host pull-up control.
- SDIO suspend and resume.
- 1 to 65 535 bytes blocks.
- Suspend and resume operations.
- SDIO Read-wait.
- Maximum clock speed of 52 MHz (MMC 4.1).
- Supports CE ATA 1.1:
 - 8 bit data width
 - Including ATA module

6.10 Universal Serial Bus 2.0 High Speed On-The-Go (OTG)

The USB OTG module allows the LPC3130/3131 to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode. In addition, the LPC3130/3131 has a special, built-in mode in which it enumerates as a Device Firmware Upgrade (DFU) class, which allows for a (factory) download of the device firmware through USB.

This module has the following features:

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Contains UTMI+ compliant transceiver (PHY).
- Supports Interrupts.
- This module has its own, integrated DMA engine.

6.11 DMA controller

The DMA Controller can perform DMA transfers on the AHB bus without using the CPU.

This module has the following features:

- Supported transfer types:
 - Memory to memory:
 - Memory can be copied from the source address to the destination address with a specified length, while incrementing the address for both the source and destination.
 - Memory to peripheral:

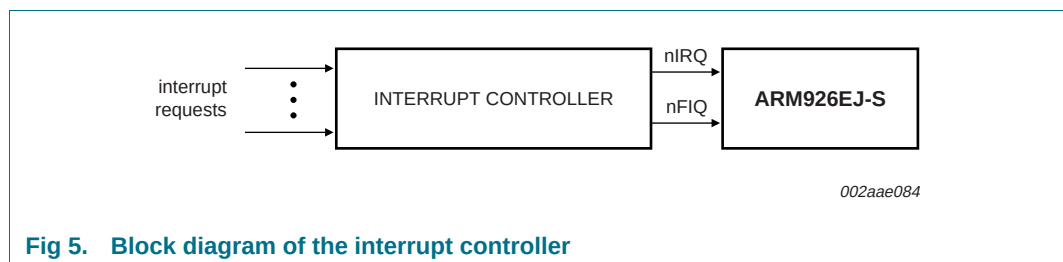
- Data is transferred from incrementing memory to a fixed address of a peripheral.
The flow is controlled by the peripheral.
- Peripheral to memory:
 - Data is transferred from a fixed address of a peripheral to incrementing memory.
The flow is controlled by the peripheral.
- Supports single data transfers for all transfer types.
- Supports burst transfers for memory to memory transfers. A burst always consists of multiples of 4 (32 bit) words.
- The DMA controller has 12 channels.
- Scatter-gather is used to gather data located at different areas of memory. Two channels are needed per scatter-gather action.
- Supports byte, half word and word transfers, and correctly aligns it over the AHB bus.
- Compatible with ARM flow control for single requests (sreq), last single requests (lsreq), terminal count info (tc), and dma clearing (clr).
- Supports swapping in endianness of the transported data.

Table 9: Peripherals that support DMA access

Peripheral name	Supported Transfer Types
NAND flash controller	Memory to memory
SPI	Memory to peripheral and peripheral to memory
MCI	Memory to peripheral and peripheral to memory
LCD interface	Memory to peripheral
UART	Memory to peripheral and peripheral to memory
I ² C0/1 master/slave	Memory to peripheral and peripheral to memory
I ² S0/1 receive	Peripheral to Memory
I ² S0/1 transmit	Memory to peripheral
PCM interface	Memory to peripheral and peripheral to memory

6.12 Interrupt controller

The Interrupt Controller (INTC) collects interrupt requests from multiple devices, masks interrupt requests, and forwards the combined requests to the processor (see [Figure 5](#)). The interrupt controller also provides facilities to identify the interrupt requesting devices to be served.



This module has the following features:

- The interrupt controller decodes all the interrupt requests issued by the on-chip peripherals.

- Two interrupt lines (nFIQ, nIRQ) to the ARM core. The ARM core supports two distinct levels of priority on all interrupt sources, nFIQ for high priority interrupts and nIRQ for normal priority interrupts.
- Software interrupt request capability associated with each request input.
- Visibility of the interrupt's request state before masking.
- Support for nesting of interrupt service routines.
- Interrupts routed to nIRQ and to nFIQ are vectored.
- Level interrupt support.

The following blocks can generate interrupts:

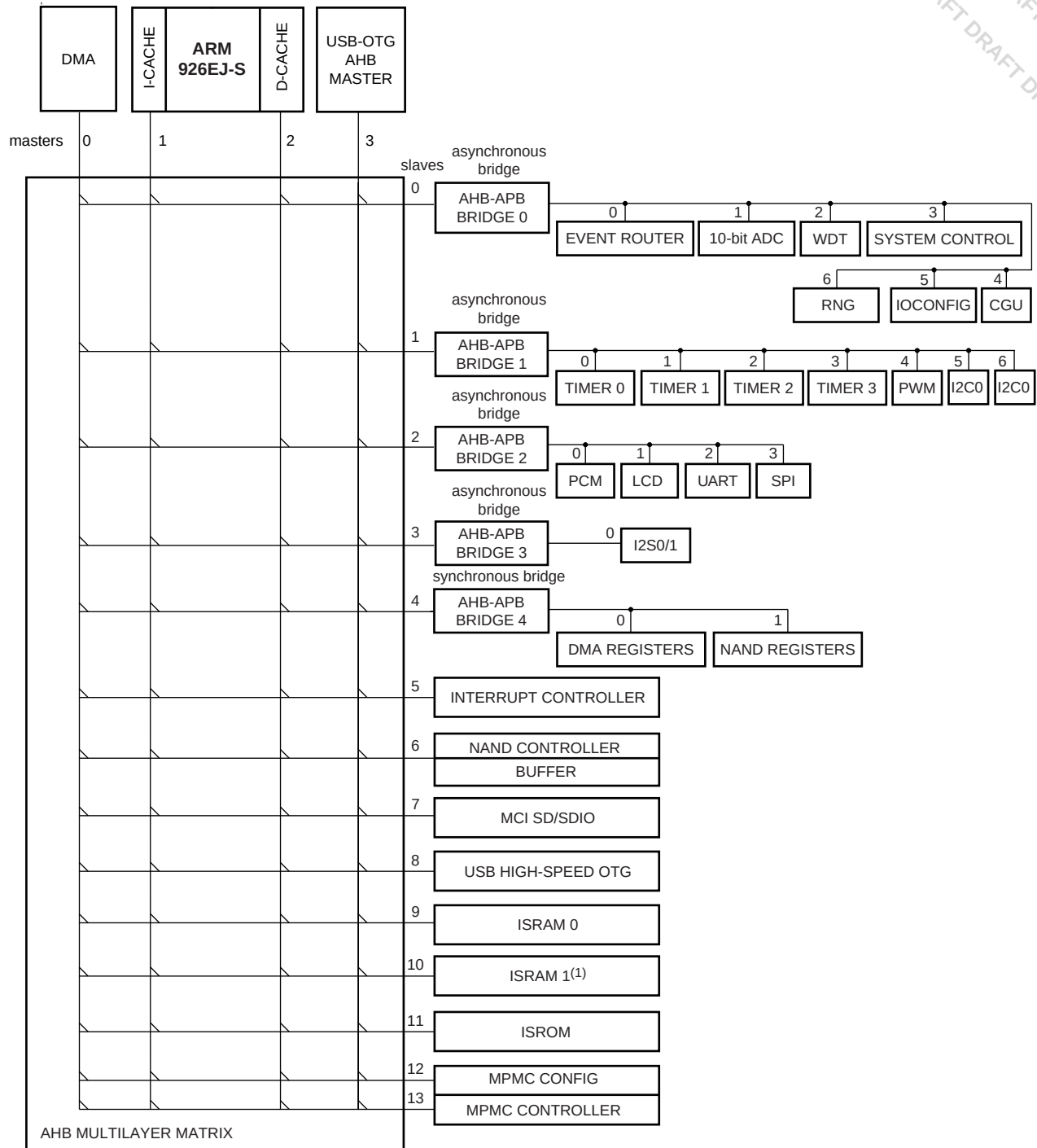
- NAND flash controller
- USB 2.0 HS OTG
- Event router
- 10-bit ADC
- UART
- LCD
- MCI
- SPI
- I²C0 and I²C1
- Timer0, Timer1, Timer2, and Timer3
- I²S transmit: I2STX_0 and I2STX_1
- I²S receive: I2SRX_0 and I2SRX_1
- DMA

6.13 Multi-layer AHB

The multi-layer AHB is an interconnection scheme based on the AHB protocol that enables parallel access paths between multiple masters and slaves in a system.

Multiple masters can have access to different slaves at the same time.

[Figure 6](#) gives an overview of the AHB Multi layer Bus configuration in the LPC3130/3131. AHB masters and slaves are numbered according to their AHB port number.



\ = master/slave connection supported by matrix

002aae126

(1) LPC3131 only.

Fig 6. LPC3130/3131 AHB multilayer matrix connections

This module has the following features:

- Supports all combinations of 32-bit masters and slaves (fully connected interconnect matrix).
- Round-robin priority mechanism for bus arbitration: all masters have the same priority and get bus access in their natural order
- Four devices on a master port (listed in their natural order for bus arbitration):
 - DMA
 - ARM926 instruction port
 - ARM926 data port
 - USB OTG
- Devices on a slave port (some ports are shared between multiple devices):
 - AHB to APB Bridge 0
 - AHB to APB Bridge 1
 - AHB to APB Bridge 2
 - AHB to APB Bridge 3
 - AHB to APB Bridge 4
 - Interrupt Controller
 - NAND flash controller
 - MCI SD/SDIO
 - USB 2.0 HS OTG.
 - 96 kB ISRAM
 - 96 kB ISRAM (LPC3131 only)
 - 128 kB ROM
 - MPMC (Multi-Purpose Memory Controller)

6.14 APB bridge

The APB bridge is a bus bridge between the AMBA Advanced High-performance Bus (AHB) and the ARM Peripheral Bus (APB) interface.

The module supports two different architectures:

- Single Clock Architecture, synchronous bridge. The same clock is used at the AHB side and at the APB side of the bridge. The AHB-to-APB4 bridge uses this architecture.
- Dual Clock Architecture, asynchronous bridge. Different clocks are used at the AHB side and at the APB side of the bridge. The AHB-to-APB0, AHB-to-APB1, AHB-to-APB2, and AHB-to-APB3 bridges use this architecture.

6.15 Clock Generation Unit (CGU)

The clock generation unit generates all clock signals in the system and controls the reset signals for all modules.

The structure of the CGU is shown in [Figure 7](#). Each output clock generated by the CGU belongs to one of the domains. Each clock domain is fed by a single base clock that originates from one of the available clock sources. Within a clock domain, fractional dividers are available to divide the base clock to a lower frequency.

Within most clock domains, the output clocks are again grouped into one or more subdomains. All output clocks within one subdomain are either all generated by the same fractional divider or they are connected directly to the base clock. Therefore all output clocks within one subdomain have the same frequency and all output clocks within one clock domain are synchronous because they originate from the same base clock.

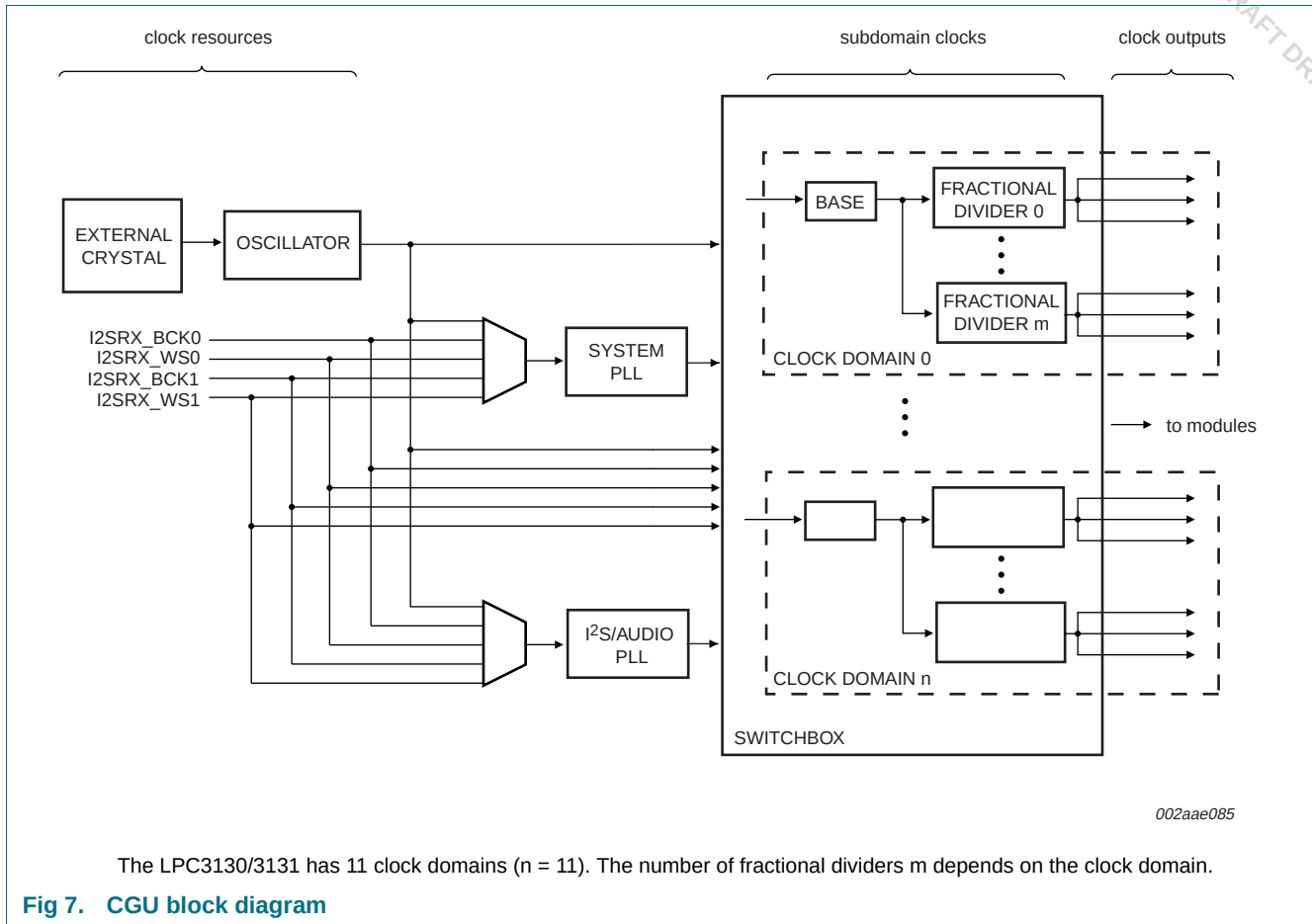
The CGU reference clock is generated by the external crystal. In addition, the CGU has several Phase Locked Loop (PLL) circuits to generate clock signals that can be used for system clocks and/or audio clocks. All clock sources, except the output of the PLLs, can be used as reference input for the PLLs.

This module has the following features:

- Advanced features to optimize the system for low power:
 - All output clocks can be disabled individually for flexible power optimization
 - Some modules have automatic clock gating: they are only active when bus access to the module is required.
 - Variable clock scaling for automatic power optimization of the AHB bus (high clock frequency when the bus is active, low clock frequency when the bus is idle).
 - Clock wake-up feature: module clocks can be programmed to be activated automatically on the basis of an event detected by the Event Router (see also [Section 6.19](#)). For example, all clocks (including the ARM /bus clocks) are off and activated automatically when a button is pressed.
- Supports five clock sources:
 - Reference clock generated by the oscillator with an external crystal.
 - Pins I2SRX_BCK0, I2SRX_WS0, I2SRX_BCK1 and I2SRX_WS1 are used to input external clock signals (used for generating audio frequencies in I2SRX slave mode, see also [Section 6.4](#)).
- Two PLLs:
 - System PLL generates programmable system clock frequency from its reference input.
 - I²S PLL generates programmable audio clock frequency (typically $256 \times f_s$) from its reference input.

Remark: Both the System PLL and the I²S PLL generate their frequencies based on their (individual) reference clocks. The reference clocks can be programmed to the oscillator clock or one of the external clock signals.
- Highly flexible switchbox to distribute the signals from the clock sources to the module clocks.
 - Each clock generated by the CGU is derived from one of the base clocks and optionally divided by a fractional divider.
 - Each base clock can be programmed to have any one of the clock sources as an input clock.
 - Fractional dividers can be used to divide a base clock by a fractional number to a lower clock frequency.
 - Fractional dividers support clock stretching to obtain a (near) 50% duty cycle output clock.
- Register interface to reset all modules under software control.

- Based on the input of the Watchdog timer (see also [Section 6.16](#)), the CGU can generate a system-wide reset in the case of a system stall.



6.16 Watchdog Timer (WDT)

The Watchdog Timer can be used to generate a system reset if there is a CPU/software crash. In addition, the watchdog timer can be used as an ordinary timer. [Figure 8](#) shows how the Watchdog Timer module is connected in the system.

This module has the following features:

- In the event of a software or hardware failure, generates a chip-wide reset request when its programmed time-out period has expired (output m1).
- Watchdog counter can be reset by a periodical software trigger.
- After a reset, a register will indicate whether a reset has occurred because of a watchdog generated reset.
- Watchdog timer can also be used as a normal timer (output m0).

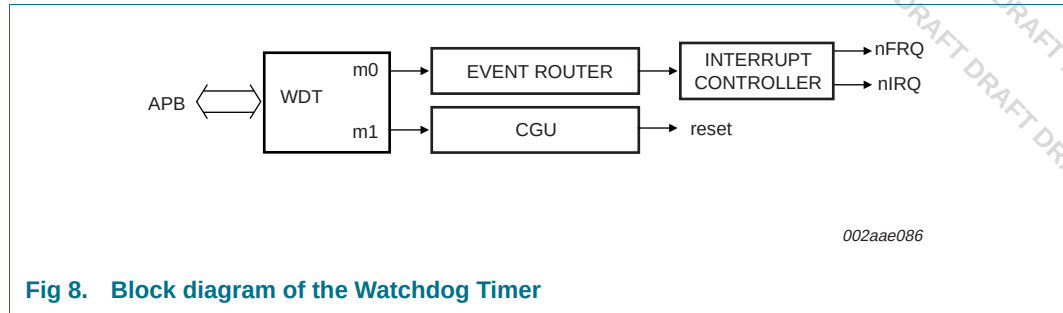


Fig 8. Block diagram of the Watchdog Timer

6.17 IO configuration

The General Purpose Input/Output (GPIO) pins can be controlled through the register interface provided in the Input/Output configuration module (IOCONF). Next to several dedicated GPIO pins, most digital IO pins can also be used as GPIO if they are not required for their normal, dedicated function.

This module has the following features:

- Provides control for the digital pins that can double as GPIO (next to their normal function). The pinning list in [Table 4](#) indicates which pins can double as GPIO.
- Each pin controlled by the IOCONFIG can be configured for four operational modes:
 - Normal operation (i.e. controlled by a function block).
 - Driven low.
 - Driven high.
 - High impedance/input.
- The GPIO pins can be observed (read) in any mode.
- The register interface provides set and clear access methods for choosing the operational mode.

6.18 10-bit Analog-to-Digital Converter (ADC)

This module is a 10-bit successive approximation Analog-to-Digital Converter (ADC10B) with an input multiplexer to allow for multiple analog signals on its input. A common use of this module is to read out multiple keys on one input from a resistor network.

This module has the following features:

- Four analog input channels, selected by an analog multiplexer.
- Programmable ADC resolution from 2 bit to 10 bit.
- The maximum conversion rate is 400 k samples/s for 10 bit resolution and 1500 k samples/s for 2 bit resolution.
- Single A/D conversion scan mode and continuous A/D conversion scan mode.
- Power-down mode.

6.19 Event router

The Event router extends the interrupt capability of the system by offering a flexible and versatile way of generating interrupts. Combined with the wake-up functionality of the CGU, it also offers a way to wake-up the system from suspend mode (with all clocks deactivated).

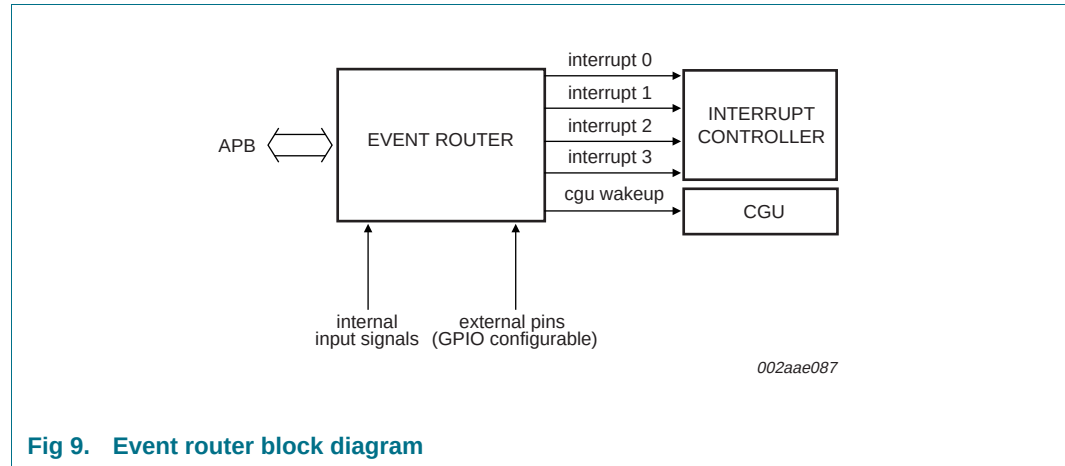


Fig 9. Event router block diagram

The Event Router has four interrupt outputs connected to the interrupt controller and one wake-up output connected to the CGU as shown in [Figure 9](#). The output signals are activated when an event (for instance a rising edge) is detected on one of the input signals. The input signals of the Event Router are connected to relevant internal control signals in the system or to external signals through pins of the LPC3130/3131.

This module has the following features:

- Provides programmable routing of input events to multiple outputs for use as interrupts or wake up signals.
- Input events can come from internal signals or from the pins that can be used as GPIO.
- Inputs can be used either directly or latched (edge detected) as an event source.
- The active level (polarity) of the input signal for triggering events is programmable.
- Direct events will disappear when the input becomes inactive.
- Latched events will remain active until they are explicitly cleared.
- Each input can be masked globally for all inputs at once.
- Each input can be masked for each output individually.
- Event detect status can be read for each output separately.
- Event detection is fully asynchronous (no active clock required).
- Module can be used to generate a system wake-up from suspend mode.

Remark: All pins that can be used as GPIO are connected to the Event Router (see [Figure 9](#)). Note that they can be used to trigger events when in normal functional mode or in GPIO-input mode but not in GPIO-output mode.

6.20 Random number generator

The Random Number Generator (RNG) generates true random numbers for use in advanced security and Digital Rights Management (DRM) related schemes. These schemes rely upon truly random, i.e. completely unpredictable numbers.

This module has the following features:

- True random number generator.
- The random number register does not rely on any kind of reset.
- The generators are free running in order to ensure randomness and security.

6.21 Serial Peripheral Interface (SPI)

The SPI module is used for synchronous serial data communication with other devices which support the SPI/SSI protocol. Examples are memories, cameras, or WiFi-g. The SPI/SSI-bus is a 5-wire interface, and it is suitable for low, medium, and high data rate transfers.

This module has the following features:

- Supports Motorola SPI frame format with a word size of 8/16 bits.
- Texas Instruments SSI (Synchronous Serial Interface) frame format with a word size of 4 bit to 16 bit.
- Receive FIFO and transmit FIFO of 64 half-words each.
- Serial clock rate master mode maximum 45 MHz.
- Serial clock rate slave mode maximum 25 MHz.
- Support for single data access DMA.
- Full-Duplex operation.
- Supports up to three slaves.
- Supports maskable interrupts.
- Supports DMA transfers.

6.22 Universal Asynchronous Receiver Transmitter (UART)

The UART module supports the industry standard serial interface.

This module has the following features:

- Programmable baud rate with a maximum of 1049 kilobaud.
- Programmable data length (5 bit to 8 bit).
- Implements only asynchronous UART.
- Transmit break character length indication.
- Programmable one to two stops bits in transmission.
- Odd/Even/Force parity check/generation.
- Frame error, overrun error and break detection.
- Automatic hardware flow control.
- Independent control of transmit, receive, line status, data set interrupts, and FIFO's.

- SIR-IrDA encoder/decoder (from 2400 to 115 kilobaud).
- Supports maskable interrupts.
- Supports DMA transfers.

6.23 Pulse Code Modulation (PCM) interface

The PCM interface supports the PCM and IOM interfaces.

The IOM (ISDN Oriented Modular) interface is primarily used to interconnect telecommunications ICs providing ISDN compatibility. It delivers a symmetrical full-duplex communication link containing user data, control/programming lines, and status channels.

PCM (Pulse Code Modulation) is a very common method used for transmitting analog data in digital format. Most common applications of PCM are Digital audio as in Audio CD and computers, digital telephony and digital videos.

This module has the following features:

- Four-wire serial interface.
- Can function in both Master and Slave modes.
- Supports:
 - PCM: Pulse code modulation. Single clocking physical format.
 - MP PCM: Multi-Protocol PCM. Configurable directional per slot.
 - IOM-2: Extended ISDN-Oriented modular. Double clocking physical format.
- Twelve eight bit slots in a frame with enabling control per slot.
- Internal frame clock generation in master mode.
- Receive (RX) and Transmit (TX) DMA handshaking using a request/clear protocol.
- Interrupt generation per frame.

6.24 LCD interface

The dedicated LCD interface contains logic to interface to a 6800 (Motorola) or 8080 (Intel) compatible LCD controllers which support 4/8/16 bit modes. This module also supports a serial interface mode. The speed of the interface can be adjusted in software to match the speed of the connected LCD display.

This module has the following features:

- 4/8/16 bit parallel interface mode: 6800-series, 8080-series.
- Serial interface mode.
- Supports multiple frequencies for the 6800/8080 bus to support high- and low-speed controllers.
- Supports polling the busy flag from LCD controller to off-load the CPU from polling.
- Contains an 16 byte FIFO for sending control and data information to the LCD controller.
- Supports maskable interrupts.
- Supports DMA transfers.

6.25 I²C-bus master/slave interface

The LPC3130/3131 contains two I²C master/slave interfaces.

This module has the following features:

- **I²C0 interface:** I²C0 is a standard I²C-compliant bus interface with open-drain pins. This interface supports functions described in the I²C-bus specification for speeds up to 400 kHz. This includes multi-master operation and allows powering off this device in a working system while leaving the I²C-bus functional.
- **I²C1 interface:** The I²C1-bus interface uses standard I/O pins and is intended for use with a single-master I²C-bus and does not support powering off of this device. Standard I/Os also do not support multi-master I²C implementations.
- Supports normal mode (100 kHz SCL).
- Fast mode (400 kHz SCL with 24 MHz APB clock; 325 kHz with 12 MHz APB clock; 175 kHz with 6 MHz APB clock).
- Interrupt support.
- Supports DMA transfers (single).
- Four modes of operation:
 - Master transmitter
 - Master receiver
 - Slave transmitter
 - Slave receiver

6.26 LCD/NAND flash/SDRAM multiplexing

The LPC3130/3131 contains a rich set of specialized hardware interfaces but the TFBGA package does not contain enough pins to allow use of all signals of all interfaces simultaneously. Therefore a pin-multiplexing scheme is created, which allows the selection of the right interface for the application.

Pin multiplexing is enabled between the following interfaces:

- between the dedicated LCD interface and the external bus interface.
- between the NAND flash controller and the memory card interface.
- between UART and SPI.
- between I2STX_0 output and the PCM interface.

The pin interface multiplexing is subdivided into five categories: storage, video, audio, NAND flash, and UART related pin multiplexing. Each category supports several modes, which can be selected by programming the corresponding registers in the SysCReg.

6.26.1 Pin connections

Table 10. Signals to pins for the pin interface multiplexing

Pin Name	Default Signal	Alternate Signal	Description
mLCD_CSB	LCD_CSB	EBI_NSTCS_0	Video related pin multiplexing.
mLCD_DB_1	LCD_DB_1	EBI_NSTCS_1	Video related pin multiplexing.
mLCD_DB_0	LCD_DB_0	EBI_CLKOUT	Video related pin multiplexing.

Table 10. Signals to pins for the pin interface multiplexing

Pin Name	Default Signal	Alternate Signal	Description
mLCD_E_RD	LCD_E_RD	EBI_CKE	Video related pin multiplexing.
mLCD_RS	LCD_RS	EBI_NDYCS	Video related pin multiplexing.
mLCD_RW_WR	LCD_RW_WR	EBI_DQM_1	Video related pin multiplexing.
mLCD_DB_2	LCD_DB_2	EBI_A_2	Video related pin multiplexing.
mLCD_DB_3	LCD_DB_3	EBI_A_3	Video related pin multiplexing.
mLCD_DB_4	LCD_DB_4	EBI_A_4	Video related pin multiplexing.
mLCD_DB_5	LCD_DB_5	EBI_A_5	Video related pin multiplexing.
mLCD_DB_6	LCD_DB_6	EBI_A_6	Video related pin multiplexing.
mLCD_DB_7	LCD_DB_7	EBI_A_7	Video related pin multiplexing.
mLCD_DB_8	LCD_DB_8	EBI_A_8	Video related pin multiplexing.
mLCD_DB_9	LCD_DB_9	EBI_A_9	Video related pin multiplexing.
mLCD_DB_10	LCD_DB_10	EBI_A_10	Video related pin multiplexing.
mLCD_DB_11	LCD_DB_11	EBI_A_11	Video related pin multiplexing.
mLCD_DB_12	LCD_DB_12	EBI_A_12	Video related pin multiplexing.
mLCD_DB_13	LCD_DB_13	EBI_A_13	Video related pin multiplexing.
mLCD_DB_14	LCD_DB_14	EBI_A_14	Video related pin multiplexing.
mLCD_DB_15	LCD_DB_15	EBI_A_15	Video related pin multiplexing.
mGPIO5	GPIO5	MCI_CLK	Storage related pin multiplexing.
mGPIO6	GPIO6	MCI_CMD	Storage related pin multiplexing.
mGPIO7	GPIO7	MCI_DAT_0	Storage related pin multiplexing.
mGPIO8	GPIO8	MCI_DAT_1	Storage related pin multiplexing.
mGPIO9	GPIO9	MCI_DAT_2	Storage related pin multiplexing.
mGPIO10	GPIO10	MCI_DAT_3	Storage related pin multiplexing.
mNAND_RYBN0	NAND_RYBN0	MCI_DAT_4	NAND flash related pin multiplexing.
mNAND_RYBN1	NAND_RYBN1	MCI_DAT_5	NAND flash related pin multiplexing.
mNAND_RYBN2	NAND_RYBN2	MCI_DAT_6	NAND flash related pin multiplexing.
mNAND_RYBN3	NAND_RYBN3	MCI_DAT_7	NAND flash related pin multiplexing.
ml2STX_DATA0	I2STX_DATA0	PCM_DA	Digital Audio related pin multiplexing.
ml2STX_BCK0	I2STX_BCK0	PCM_FSC	Digital Audio related pin multiplexing.
ml2STX_WS0	I2STX_WS0	PCM_DCK	Digital Audio related pin multiplexing.
ml2STX_CLK0	I2STX_CLK0	PCM_DB	Digital Audio related pin multiplexing.
mUART_CTS_N	UART_CTS_N	SPI_CS_OUT1	UART related pin multiplexing.
mUART_RTS_N	UART_RTS_N	SPI_CS_OUT2	UART related pin multiplexing.

6.26.2 Multiplexing between LCD and MPMC

The multiplexing between the LCD interface and MPMC allows for the following two modes of operation:

- MPMC-mode: SDRAM and bus-based LCD or SRAM.
- LCD-mode: Dedicated LCD-Interface.

The external NAND flash is accessible in both modes.

The block diagram [Figure 10](#) gives a high level overview of the modules in the chip that are involved in the pin interface multiplexing between the EBI, NAND flash controller, MPMC, and RAM-based LCD interface.

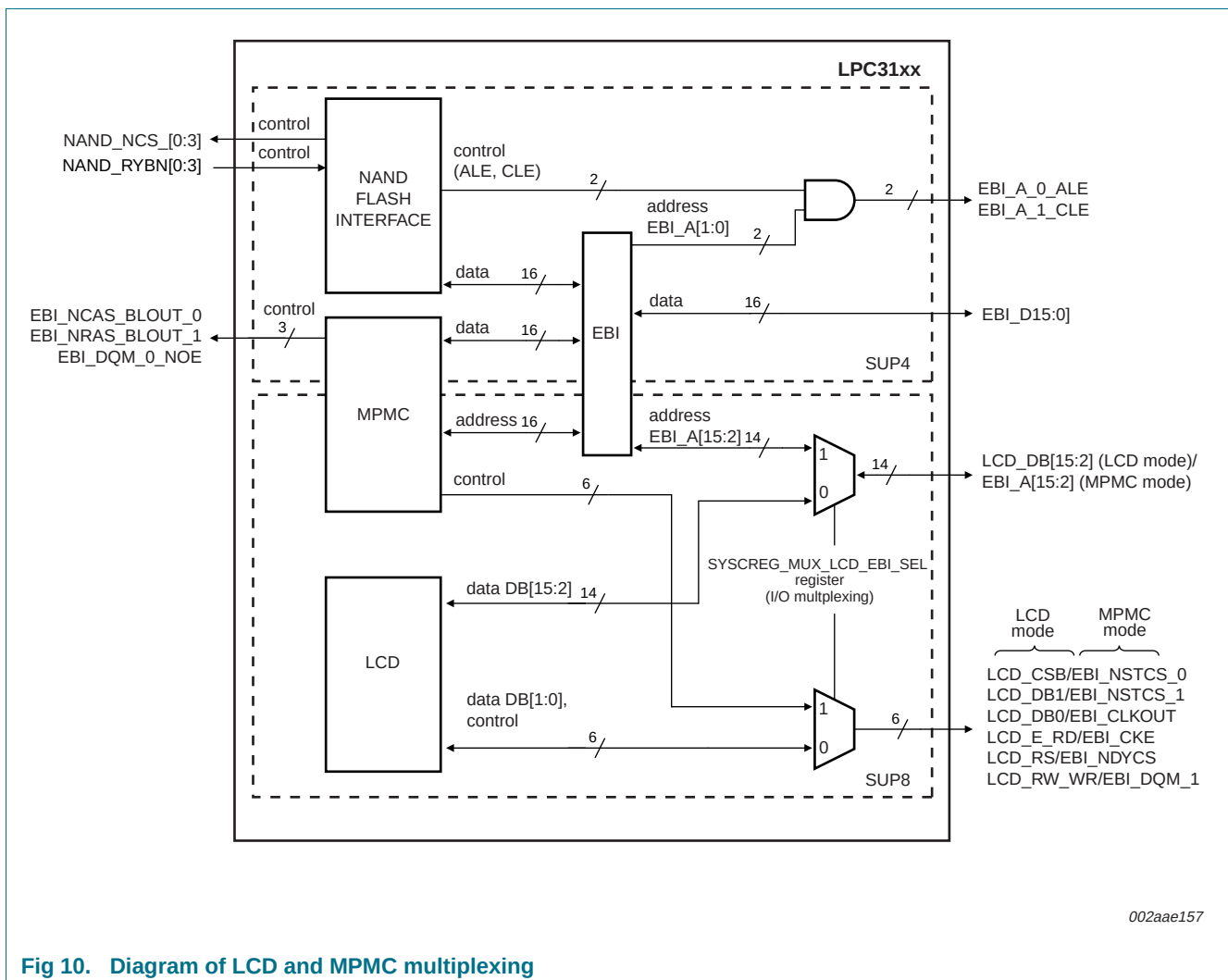


Fig 10. Diagram of LCD and MPMC multiplexing

[Figure 10](#) only shows the signals that are involved in pad-muxing, so not all interface signals are visible.

The EBI unit between the NAND flash interface and the MPMC contains an arbiter that determines which interface is muxed to the outside world. Both NAND flash and SDRAM/SRAM initiate a request to the EBI unit. This request is granted using round-robin arbitration (see [Section 6.6](#)).

6.26.3 Supply domains

As is shown in [Figure 10](#) the EBI (NAND flash/MPMC-control/data) is connected to a different supply domain than the LCD interface. The EBI control and address signals are muxed with the LCD interface signals and are part of supply domain SUP8. The SDRAM/SRAM data lines are shared with the NAND flash through the EBI and are part of supply domain SUP4. Therefore the following rules apply for connecting memories:

1. SDRAM and bus-based LCD or SRAM: This is the MPMC mode. The supply voltage for SDRAM/SRAM/bus-based LCD and NAND flash must be the same. The dedicated LCD interface is not available in this MPMC mode.
2. Dedicated LCD interface only: This is the LCD mode. The NAND flash supply voltage (SUP4) can be different from the LCD supply voltage (SUP8).

6.27 Timer module

The LPC3130/3131 contains four fully independent timer modules, which can be used to generate interrupts after a pre-set time interval has elapsed.

This module has the following features:

- Each timer is a 32 bit wide down-counter with selectable pre-scale. The pre-scaler allows using either the module clock directly or the clock divided by 16 or 256.
- Two modes of operation:
 - Free-running timer: The timer generates an interrupt when the counter reaches zero. The timer wraps around to 0xFFFFFFFF and continues counting down.
 - Periodic timer: The timer generates an interrupt when the counter reaches zero. It reloads the value from a load register and continues counting down from that value. An interrupt will be generated every time the counter reaches zero. This effectively gives a repeated interrupt at a regular interval.
- At any time the current timer value can be read.
- At any time the value in the load register may be re-written, causing the timer to restart.

6.28 Pulse Width Modulation (PWM) module

This PWM can be used to generate a pulse width modulated or a pulse density modulated signal. With an external low pass filter, the module can be used to generate a low-frequency analog signal. A typical use of the output of the module is to control the backlight of an LCD display.

This module has the following features:

- Supports Pulse Width Modulation (PWM) with software controlled duty cycle.
- Supports Pulse Density Modulation (PDM) with software controlled pulse density.

6.29 System control registers

The System Control Registers (SysCReg) module provides a register interface for some of the high-level settings in the system such as multiplexers and mode settings. This is an auxiliary module included in this overview for the sake of completeness.

6.30 I²S0/1 interfaces

The I²S0/1 receive and I²S0/1 transmit modules have the following features:

- Audio interface compatible with the I²S standard.
- I²S0/1 receive supports master mode and slave mode.
- I²S0/1 transmit supports master mode.
- Supports LSB justified words of 16, 18, 20 and 24 bits.
- Supports a configurable number of bit clock periods per Word Select period (up to 128 bit clock periods).
- Supports DMA transfers.
- Transmit FIFO (I²S transmit) or receive FIFO (I²S receive) of 4 stereo samples.
- Supports single 16 bit transfers to/from the left or right FIFO.
- Supports single 24 bit transfers to/from the left or right FIFO.
- Supports 32-bit interleaved transfers, with the lower 16 bits representing the left audio sample, and the higher 16 bits representing the right audio sample.
- Supports two 16-bit audio samples combined in a 32-bit word (2 left or 2 right samples) to reduce busload.
- Provides maskable interrupts for audio status: FIFO underrun/overflow/full/half_full/not empty for left and right channel separately.

7. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
All digital I/O pins						
V_i	input voltage		−0.5	-	+3.6	V
V_o	output voltage		−0.5	-	+3.6	V
I_o	output current	VDDE_IOC = 3.3 V	-	4	-	mA
Temperature values						
T_j	junction temperature		−40	25	125	°C
T_{stg}	storage temperature	^[2]	−65	-	+150	°C
T_{amb}	ambient temperature		−40	+25	+85	°C
Electrostatic handling						
V_{esd}	electrostatic discharge voltage	human body model ^[3]	−500	-	+500	V
		machine model	−100	-	+100	V
		charged device model	-	500	-	V

[1] The following applies to the limiting values:

- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Dependent on package type.

[3] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8. Static characteristics

This chapter gives an overview of the most important static characteristics of the LPC3130/3131. More detailed specifications will be given in future versions of this document.

Table 12: Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply pins						
$V_{DD(IO)}$	input/output supply voltage	NAND flash controller pads (SUP4) and LCD interface (SUP8); 1.8 V mode	1.65	1.8	1.95	V
		NAND flash controller pads (SUP4) and LCD interface (SUP8); 2.8 V mode	2.5	2.8	3.1	V
		other peripherals (SUP 3)	2.7	3.3	3.6	V
$V_{DD(CORE)}$	core supply voltage	(SUP1)	1.0	1.2	1.3	V
$V_{DD(OSC_PLL)}$	oscillator and PLL supply voltage	on pin VDDA12; for 12 MHz oscillator (SUP1)	1.0	1.2	1.3	V
$V_{DD(ADC)}$	ADC supply voltage	on pin ADC10B_VDDA33; for 10-bit ADC (SUP 3)	2.7	3.3	3.6	V
V_{BUS}	bus supply voltage	on pin USB_VBUS (SUP5)	-	5.0	-	V
$V_{DDA(USB)(3V3)}$	USB analog supply voltage (3.3 V)	on pin USB_VDDA33 (SUP 3)	3.0	3.3	3.6	V
		on pin USB_VDDA33_DRV (SUP 3); driver	2.7	3.3	3.6	V
$V_{DDA(PLL)(1V2)}$	PLL analog supply voltage (1.2 V)	on pin USB_VDDA12_PLL (SUP1)	1.1	1.2	1.3	V
Input pins and I/O pins configured as input						
V_I	input voltage		0	-	VDDE_IOC	V
V_{IH}	HIGH-level input voltage	SUP3; SUP4; SUP8	$0.7VDDE_IOx$ ($x = A, B, C$)	-	-	V
V_{IL}	LOW-level input voltage	SUP3; SUP4; SUP8	-	-	$0.3VDDE_IOx$ ($x = A, B, C$)	V
V_{hys}	hysteresis voltage	SUP4; SUP8				V
		1.8 V mode	400	-	600	mV
		2.8 V mode	550	-	850	mV
		SUP3	$0.1VDDE_IOC$	-	-	V
I_{IL}	LOW-level input current	$V_I = 0\text{ V}$; no pull-up	-	-	<td>	μA

Table 12: Static characteristics $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DD(I/O)}$; no pull-down	-	-	<tbd>	μA
I_{latch}	I/O latch-up current	$-(1.5V_{DD(I/O)}) < V_I < (1.5V_{DD(I/O)})$	-	-	<tbd>	mA
I_{pu}	pull-up current	inputs with pull-up; $V_I = 0$				
		SUP4/SUP8; 1.8 V mode	<tbd>	<tbd>	<tbd>	μA
		SUP4/SUP8; 2.8 V mode	<tbd>	<tbd>	<tbd>	μA
		SUP3	<tbd>	<tbd>	<tbd>	μA
I_{pd}	pull-down current	inputs with pull-down; $V_I = V_{DD}$				
		SUP4/SUP8; 1.8 V mode	<tbd>	<tbd>	<tbd>	μA
		SUP4/SUP8; 2.8 V mode	<tbd>	<tbd>	<tbd>	μA
		SUP3	<tbd>	<tbd>	<tbd>	μA
C_i	input capacitance	excluding bonding pad capacitance	-	-	<tbd>	pF

Output pins and I/O pins configured as output

V_O	output voltage		<tbd>	-	$V_{DD(I/O)}$	V
V_{OH}	HIGH-level output voltage	SUP4; SUP8; $I_{OH} = 6\text{ mA}$:				
		1.8 V mode	<tbd>	<tbd>	<tbd>	V
		2.8 V mode	$V_{DD(I/O)} - 0.26$	<tbd>	<tbd>	V
		SUP3; $I_{OH} = 6\text{ mA}$	$V_{DD(I/O)} - 0.26$	-	-	V
		SUP3; $I_{OH} = 30\text{ mA}$	$V_{DD(I/O)} - 0.38$	-	-	V
V_{OL}	LOW-level output voltage	SUP4; SUP8 outputs; $I_{OL} = 4\text{ mA}$				
		1.8 V mode	<tbd>	<tbd>	<tbd>	V
		2.8 V mode	<tbd>	<tbd>	<tbd>	V
		SUP3; $I_{OL} = 4\text{ mA}$	-	-	<tbd>	V
I_{OH}	HIGH-level output current	$V_{DD} = V_{DDE_IOx}$ (x = A, B, C); $V_{OH} = V_{DD} - 0.4\text{ V}$	<tbd>	-	-	mA
		$V_{DD} = V_{DDE_IOx}$ (x = A, B, C); $V_{OH} = V_{DD} - 0.4\text{ V}$	<tbd>	-	-	mA
		$V_{DD} = V_{DDE_IOx}$ (x = A, B, C); $V_{OH} = V_{DD} - 0.4\text{ V}$	<tbd>	-	-	mA
I_{OL}	LOW-level output current	$V_{DD} = V_{DDE_IOx}$ (x = A, B, C); $V_{OL} = 0.4\text{ V}$	<tbd>	-	-	mA
		$V_{DD} = V_{DDE_IOx}$ (x = A, B, C); $V_{OL} = 0.4\text{ V}$	<tbd>	-	-	mA

Table 12: Static characteristics $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; no pull-up/down	-	-	0.064	μA
I _{OHS}	HIGH-level short-circuit output current	V _{DD} = VDDE_IOx (x = A, B, C); V _{OH} = 0 V	-	-	<tbd>	mA
		V _{DD} = VDDE_IOx (x = A, B, C); V _{OH} = 0 V	-	-	<tbd>	mA
I _{OLS}	LOW-level short-circuit output current	V _{DD} = VDDE_IOx (x = A, B, C); V _{OL} = V _{DD}	-	-	<tbd>	mA
		V _{DD} = VDDE_IOx (x = A, B, C); V _{OL} = V _{DD}	-	-	<tbd>	mA
Z _o	output impedance	V _{DD} = VDDE_IOx (x = A, B, C)	<tbd>	-	<tbd>	Ω
		V _{DD} = VDDE_IOx (x = A, B, C)	<tbd>	-	<tbd>	Ω
I ² C0-bus pins						
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; no pull-up/down	-	-	7.25	μA
V _{IH}	HIGH-level input voltage		<tbd>	-	-	V
V _{IL}	LOW-level input voltage		-	-	<tbd>	V
V _{hys}	hysteresis voltage		-	<tbd>	-	V
V _{OL}	LOW-level output voltage	I _{OLS} = 3 mA	-	-	0.298	V
I _{LI}	input leakage current	V _I = <tbd>	-	<tbd>	<tbd>	μA
		V _I = 5 V	-	<tbd>	<tbd>	μA
USB						
V _{i(cm)}	common-mode input voltage	high-speed mode	-50	200	500	mV
		full-speed/low-speed mode	800	-	2500	mV
		chirp mode	-50	-	600	mV
V _{i(dif)}	differential input voltage		100	400	1100	mV

Table 13. ADC static characteristics

$V_{DD(ADC)} = 2.7\text{ V to }3.6\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ unless otherwise specified; ADC frequency <tb>.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0 ^[1]	-	$V_{DD(ADC)}$	V
C_{ia}	analog input capacitance		-	-	<tb>	pF
$N_{res(ADC)}$	ADC resolution		2	-	10	bit
E_D	differential linearity error	^[2] ^[3] ^[4]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	^[2] ^[5]	-	-	± 1	LSB
E_O	offset error	^[2] ^[6]	-	-	<tb>	LSB
E_G	gain error	^[2] ^[7]	-	-	<tb>	%
E_T	absolute error	^[2] ^[8]	-	-	<tb>	LSB
$V_{err(O)}$	offset error voltage		-20	-	+20	mV
$V_{err(FS)}$	full-scale offset voltage		<tb>	-	<tb>	mV
R_{vsi}	voltage source interface resistance	^[9]	-	-	<tb>	k Ω

[1] On pin ADC10B_GNDA.

[2] Conditions: $V_{SSA} = 0\text{ V}$ on pin ADC10B_GNDA, $V_{DD(ADC)} = 3.3\text{ V}$.

[3] The ADC is monotonic, there are no missing codes.

[4] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 11](#).

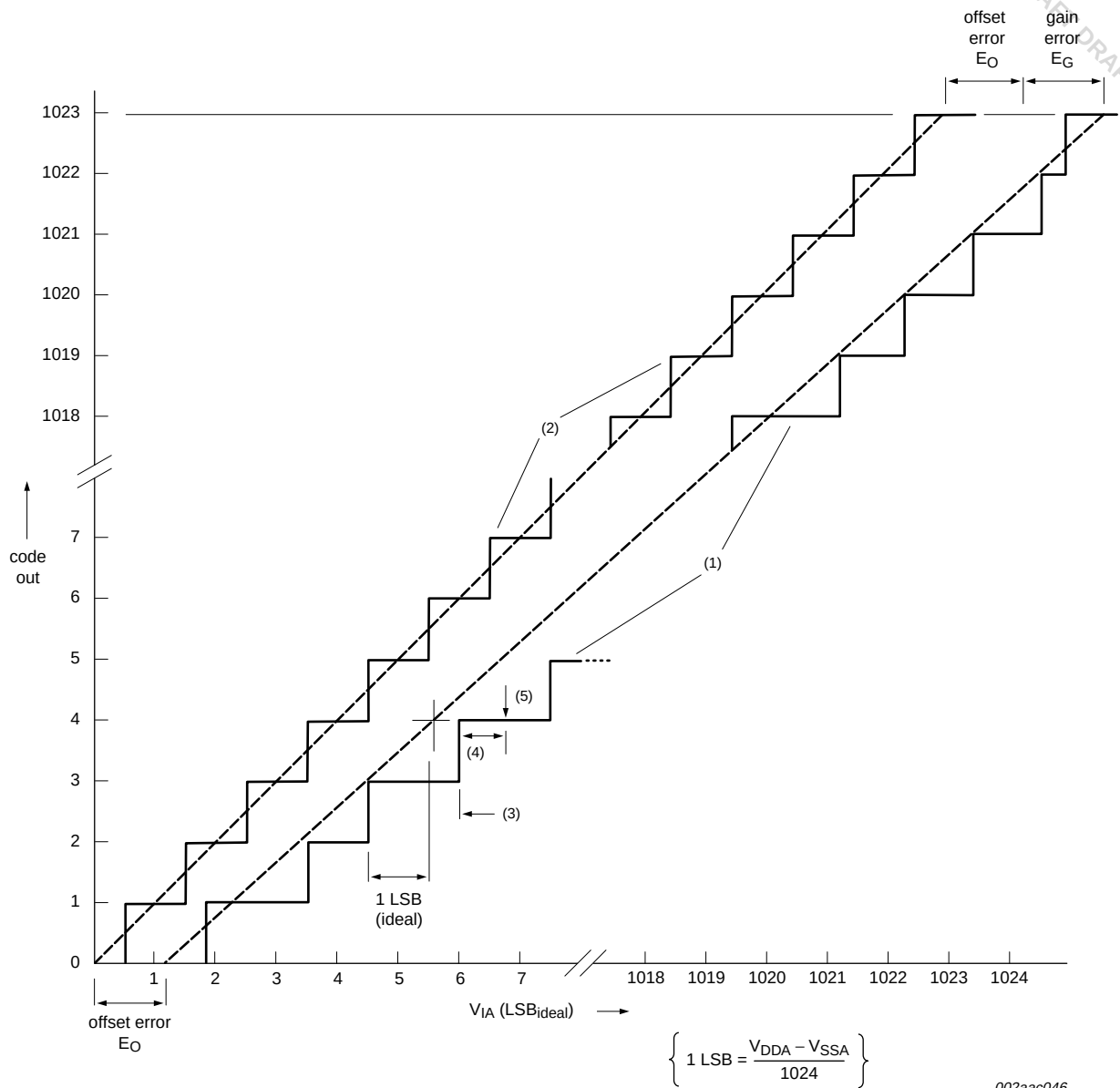
[5] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 11](#).

[6] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 11](#).

[7] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 11](#).

[8] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 11](#).

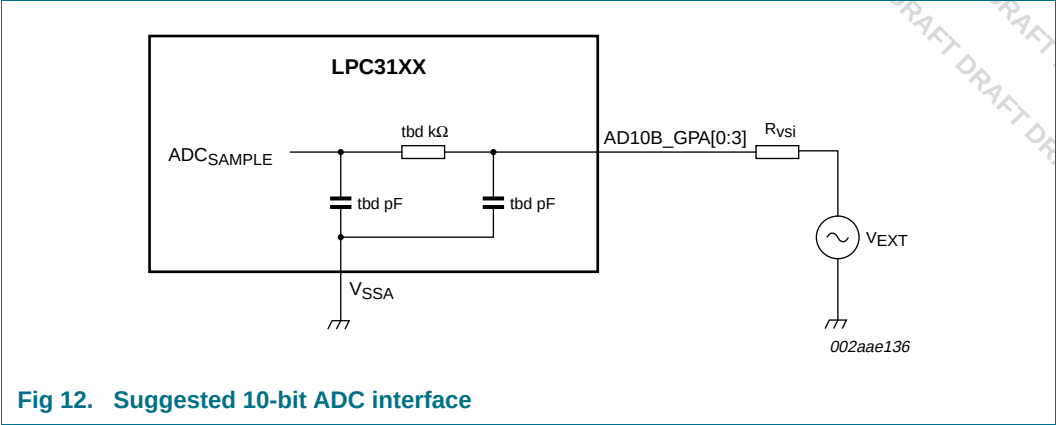
[9] See [Figure 12](#).



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- (1) Example of an actual transfer curve.
- (2) The ideal transfer curve.
- (3) Differential linearity error (E_D).
- (4) Integral non-linearity ($E_{L(adj)}$).
- (5) Center of a step of the actual transfer curve.

Fig 11. ADC characteristics



9. Dynamic characteristics

9.1 LCD controller

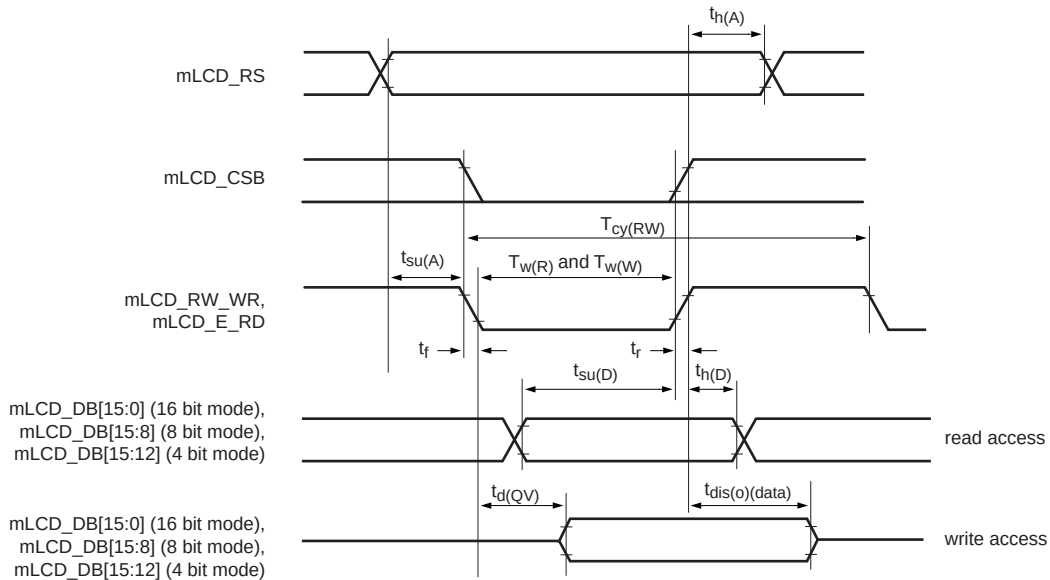
Intel 8080 mode

Table 14. Dynamic characteristics: LCD controller in Intel 8080 mode

$C_L = 25 \text{ pF}$, $T_{amb} = 20 \text{ }^{\circ}\text{C}$, $VDDIO_B = 1.8 \text{ V}$ and 2.8 V .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(A)}$	address set-up time		<tbid>	-	-	ns
$t_{h(A)}$	address hold time		<tbid>	-	-	ns
$T_{cy(RW)}$	read or write cycle time	[1]	<tbid>	-	-	ns
$T_{w(W)}$	write enable pulse width	[1]	<tbid>	-	-	ns
$T_{w(R)}$	read enable pulse width	[1]	<tbid>	-	-	ns
t_r	rise time		-	-	<tbid>	ns
t_f	fall time		-	-	<tbid>	ns
$t_{su(D)}$	data input set-up time		<tbid>	-	-	ns
$t_{h(D)}$	data input hold time		<tbid>	-	-	ns
$t_{d(QV)}$	data output valid delay time		-	-	<tbid>	ns
$t_{dis(o)(data)}$	data output disable time		<tbid>	-	<tbid>	ns

[1] Timing is determined by the LCD Interface Control Register fields: INVERT_CS = 1; MI = 0; PS = 0; INVERT_E_RD = 0. See LPC313x user manual.



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Fig 13. LCD timing (Intel 8080 mode)

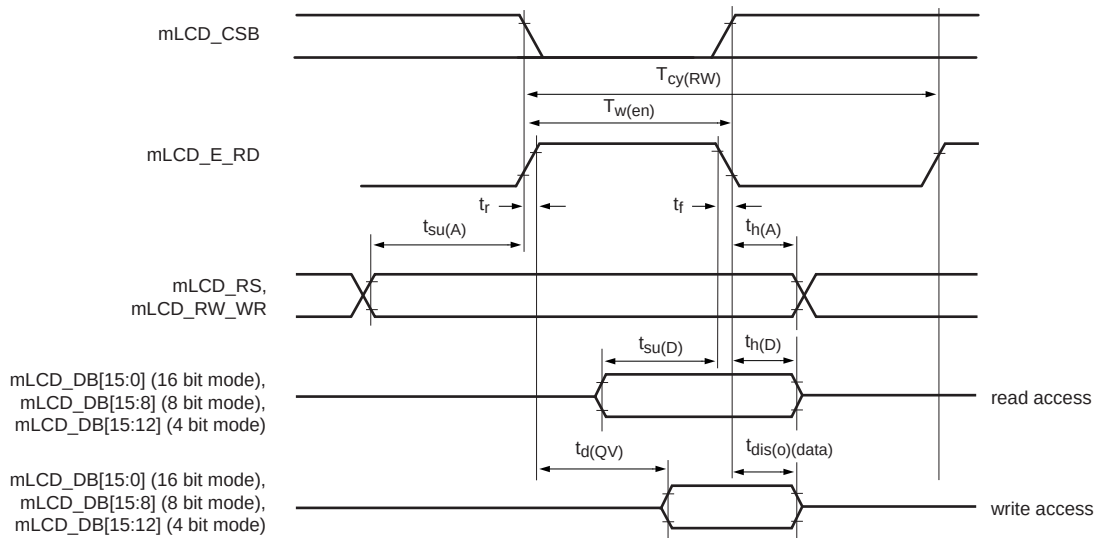
Motorola 6800 mode

Table 15. Dynamic characteristics: LCD controller in Motorola 6800 mode

$C_L = 25 \text{ pF}$, $T_{amb} = 20 \text{ }^\circ\text{C}$, $V_{DDIO_B} = 1.8 \text{ V}$ and 2.8 V .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(A)}$	address set-up time		<tbid>	-	-	ns
$t_{h(A)}$	address hold time		<tbid>	-	-	ns
$T_{cy(RW)}$	read or write cycle time	[1]	<tbid>	-	-	ns
t_r	rise time		-	-	<tbid>	ns
t_f	fall time		-	-	<tbid>	ns
$t_{su(D)}$	data input set-up time		<tbid>	-	-	ns
$t_{h(D)}$	data input hold time		<tbid>	-	-	ns
$t_{d(QV)}$	data output valid delay time		-	-	<tbid>	ns
$t_{dis(o)(data)}$	data output disable time		<tbid>		<tbid>	ns
$T_{w(en)}$	enable pulse width	read cycle	<tbid>	-	-	ns
		write cycle	<tbid>	-	-	ns

[1] Timing is derived from the LCD Interface Control Register fields: INVERT_CS = 1; MI = 1; PS = 0; INVERT_E_RD = 1. See LPC313x User manual.



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Fig 14. LCD timing (Motorola 6800 mode)

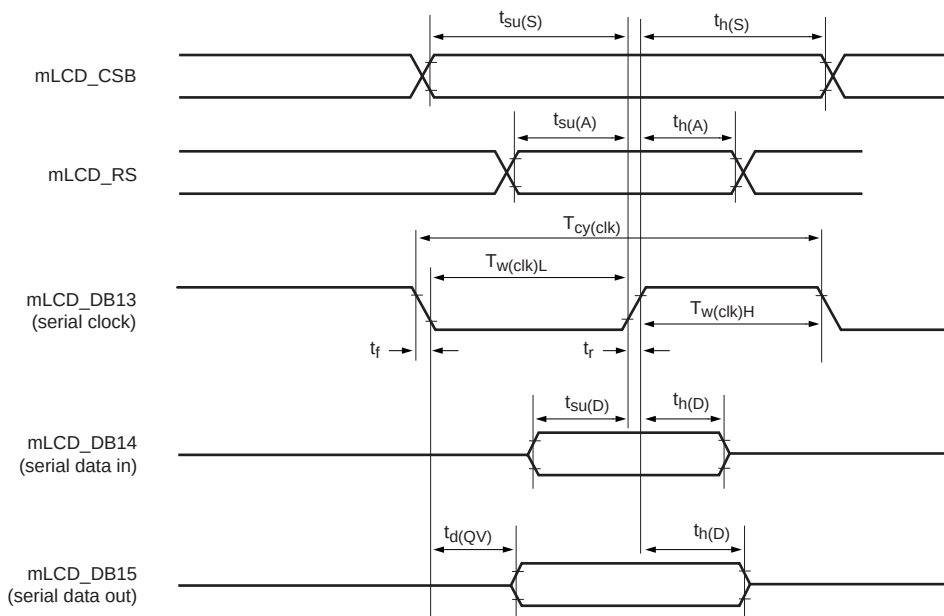
Serial mode

Table 16. Dynamic characteristics: LCD controller serial mode

$C_L = 25 \text{ pF}$, $T_{amb} = 20 \text{ }^\circ\text{C}$, $V_{DDIO_B} = 1.8 \text{ V}$ and 2.8 V .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	[1]	<td>	-	-	ns
$T_{w(clk)H}$	HIGH clock pulse width	[1]	<td>	-	-	ns
$T_{w(clk)L}$	LOW clock pulse width	[1]	<td>	-	-	ns
t_r	rise time		-	-	<td>	ns
t_f	fall time		-	-	<td>	ns
$t_{su(A)}$	address set-up time		<td>	-	-	ns
$t_{h(A)}$	address hold time		<td>	-	-	ns
$t_{su(D)}$	data input set-up time		<td>	-	-	ns
$t_{h(D)}$	data input hold time		<td>	-	-	ns
$t_{su(S)}$	chip select set-up time		<td>	-	-	ns
$t_{h(S)}$	chip select hold time		<td>	-	-	ns
$t_d(QV)$	data output valid delay time		<td>	-	-	ns

[1] Timing is determined by the LCD Interface Control Register fields: PS = 1; SERIAL_CLK_SHIFT = 3; SERIAL_READ_POS = 3. See the LPC313x User manual.



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Fig 15. LCD timing (serial mode)

9.2 SRAM controller

Table 17. Dynamic characteristics: static external memory interface

$C_L = 25\text{ pF}$, $T_{amb} = 20\text{ }^{\circ}\text{C}$, $VDDIO_B = 1.8\text{ V}$ and 2.8 V .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Common to read and write cycles						
t_{CSLAV}	$\overline{CS}$ LOW to address valid time	-	0		-	ns
Read cycle parameters						
t_{OELAV}	$\overline{OE}$ LOW to address valid time	[1]	-	$0 - WAITOEN \times HCLK$	-	ns
t_{BLSLAV}	$\overline{BLS}$ LOW to address valid time	[1]	-	$0 - WAITOEN \times HCLK$	-	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	-		$0 + WAITOEN \times HCLK$	-	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	[1]	-	$0 + WAITOEN \times HCLK$	-	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	[1][2][3]	-	$(WAITRD - WAITOEN + 1) \times HCLK$	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[1][2][3]	-	$(WAITRD - WAITOEN + 1) \times HCLK$	-	ns
$t_{su(DQ)}$	data input/output set-up time	-	8		-	ns
$t_{h(DQ)}$	data input/output hold time	-	0		-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time	-	0		-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time	-	0		-	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time	-		$2 \times HCLK$	-	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time	-		$2 \times HCLK$	-	ns
Write cycle parameters						
t_{CSLDV}	$\overline{CS}$ LOW to data valid time	-	0		-	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	[4]	-	$(WAITWEN + 1) \times HCLK$	-	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	[4]	-	$WAITWEN \times HCLK$	-	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time	[4]	-	$0 - (WAITWEN + 1) \times HCLK$	-	ns
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[4][5][6]	-	$(WAITWR - WAITWEN + 1) \times HCLK$	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[4][5]	-	$(WAITWR - WAITWEN + 3) \times HCLK$	-	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time	-		$1 \times HCLK$	-	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time	-		$1 \times HCLK$	-	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time	-	0		-	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time	-	0		-	ns

[1] Refer to the *LPC3130/31 user manual UM10314_1* for the programming of WAITOEN and HCLK.

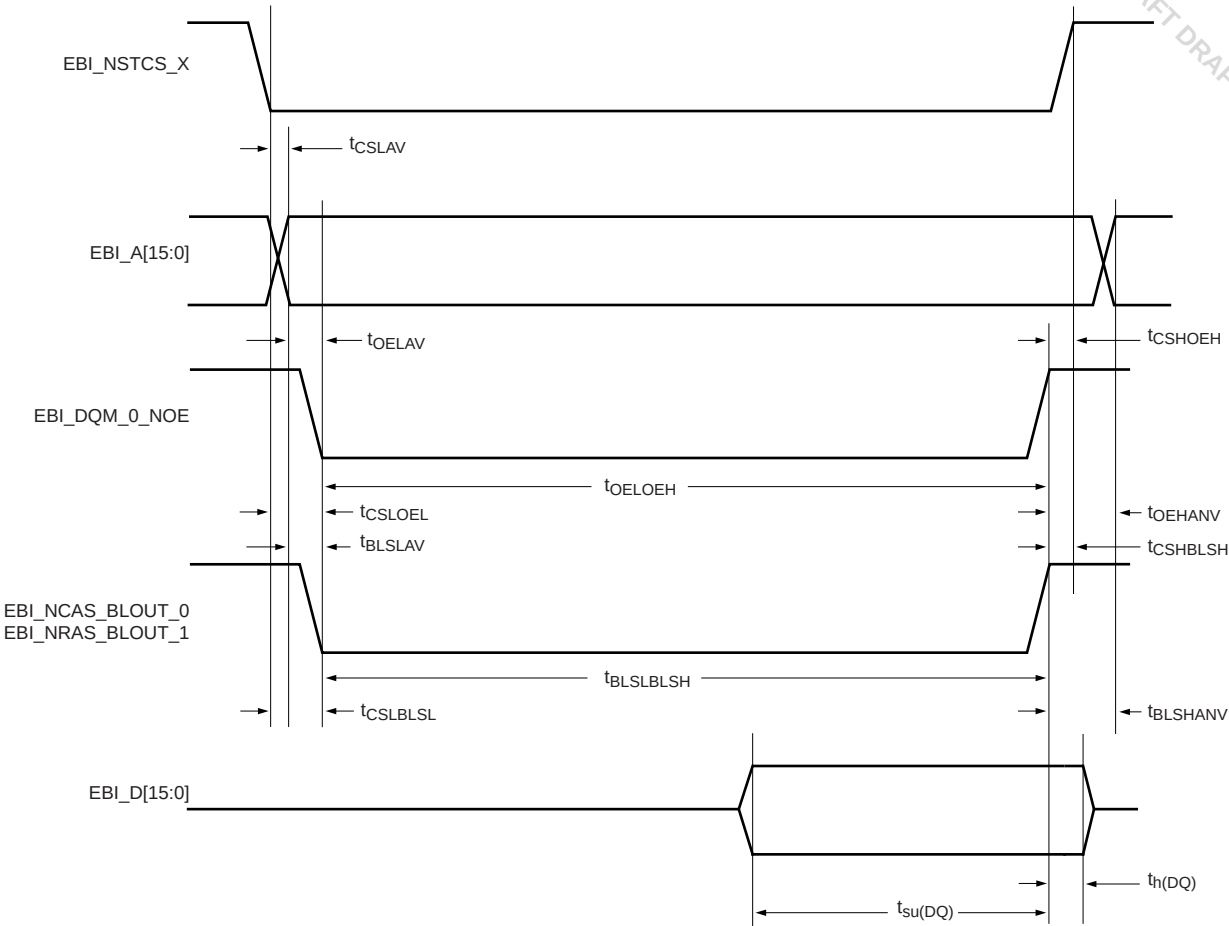
[2] Refer to the *LPC3130/31 user manual UM10314_1* for the programming of WAITRD and HCLK.

[3] $(WAITRD - WAITOEN + 1) = 3\text{ min}$ at 60 MHz.

[4] Refer to the *LPC3130/31 user manual UM10314_1* for the programming of WAITWEN and HCLK.

[5] Refer to the *LPC3130/31 user manual UM10314_1* for the programming of WAITWR and HCLK.

[6] $(WAITWR - WAITWEN + 1) = 3\text{ min}$ at 60 MHz.



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Fig 16. External memory read access to static memory



Fig 17. External memory write access to static memory

9.3 SDRAM controller

Table 18. Dynamic characteristics of SDR SDRAM memory interface

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified. [1][2]

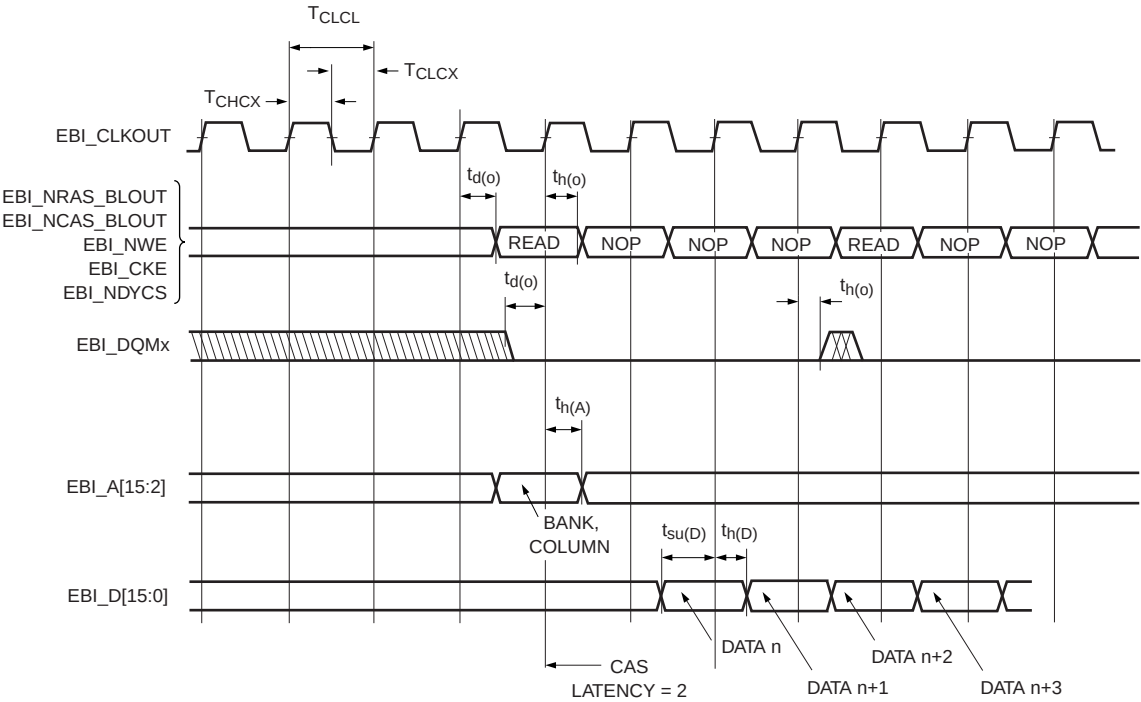
Symbol	Parameter	Conditions	Min	Typical	Max	Unit
f _{oper}	operating frequency	[3]	-	<tbid>	-	MHz
T _{CLCL}	clock cycle time		-	<tbid>	-	ns
t _{CLCX}	clock LOW time		-	<tbid>	-	ns
t _{CHCX}	clock HIGH time		-	<tbid>	-	ns
t _{d(o)}	output delay time	on pin EBI_CKE	-	-	3.5	ns
		on pins EBI_NRAS_BLOUT, EBI_NCAS_BLOUT, EBI_NWE, EBI_NDYCS	-	-	3.5	ns
		on pins EBI_DQM_1, EBI_DQM_0 NOE	-	-	5	ns

Table 18. Dynamic characteristics of SDR SDRAM memory interface $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.^{[1][2]}

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
$t_{h(o)}$	output hold time	on pin EBI_CKE	0.2	-	3.5	ns
		on pins EBI_NRAS_BLOUT, EBI_NCAS_BLOUT, EBI_NWE, EBI_NDYCS	0.23	-	3.5	ns
		on pins EBI_DQM_1, EBI_DQM_0_NOE	2	-	5	ns
$t_{d(AV)}$	address valid delay time		-	-	5	ns
$t_{h(A)}$	address hold time		0.1	-	5	ns
$t_{d(QV)}$	data output valid delay time		-	-	9	ns
$t_{h(Q)}$	data output hold time		4	-	10	ns
$t_{su(D)}$	data input set-up time		<tbd>	-	-	ns
$t_{h(D)}$	data input hold time		<tbd>	-	-	ns
t_{QZ}	data output high-impedance time		-	-	< T_{CLCL}	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

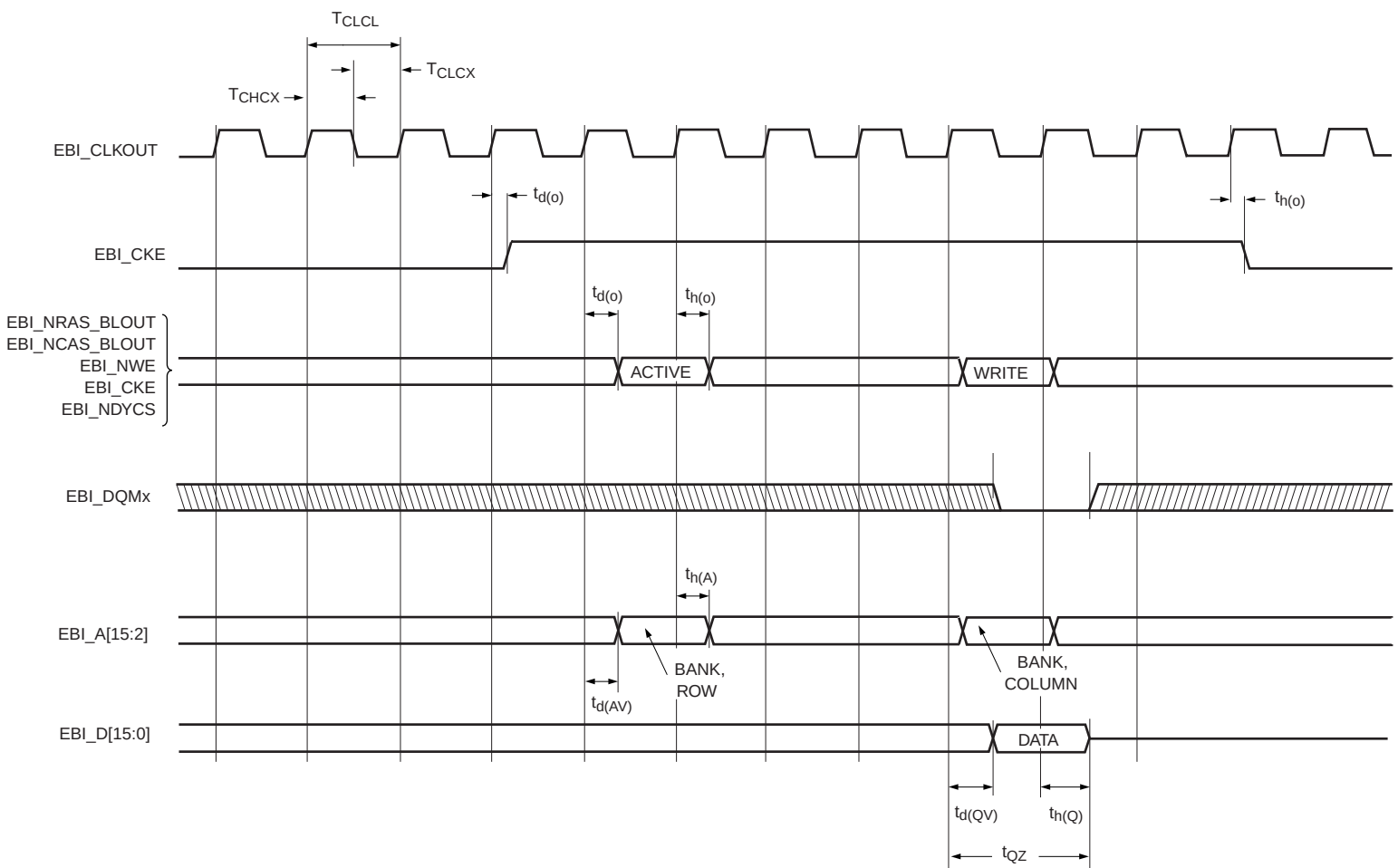
[2] All values valid for pads set to high slew rate. $V_{DDE_IOA} = V_{DDE_IOB} = 1.8 \pm 0.15\text{ V}$. $V_{DDI} = 1.2 \pm 0.1\text{ V}$.[3] $f_{oper} = 1/T_{CLCL}$



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EBI_CKE is high.

Fig 18. SDRAM burst read timing



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Fig 19. SDRAM bank activate and write timing

9.4 NAND flash memory controller

Table 19. Dynamic characteristics of the NAND Flash Memory control

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Typical	Unit
t_{REH}	$\overline{RE}$ HIGH hold time	$T_{HCLK} \times (TREH + 1)$	ns
t_{RP}	$\overline{RE}$ pulse width	$T_{HCLK} \times (TRP + 1)$	ns
t_{WH}	$\overline{WE}$ HIGH hold time	$T_{HCLK} \times (TWH + 1)$	ns
t_{WP}	$\overline{WE}$ pulse width	$T_{HCLK} \times (TWP + 1)$	ns
t_{CLS}	CLE set-up time	$T_{HCLK} \times (TCLS + 1)$	ns
t_{CLH}	CLE hold time	$T_{HCLK} \times (TCLH + 1)$	ns
t_{ALS}	ALS set-up time	$T_{HCLK} \times (TALS + 1)$	ns
t_{ALH}	ALE hold time	$T_{HCLK} \times (TALE + 1)$	ns
t_{CS}	$\overline{CE}$ set-up time	$T_{HCLK} \times (TCS + 1)$	ns
t_{CH}	$\overline{CE}$ hold time	$T_{HCLK} \times (TCH + 1)$	ns

[1] $T_{HCLK} = 1/\text{NANDFLASH_NAND_CLK}$.

[2] See registers NandTiming1 and NandTiming2 in the LPC313x UM.

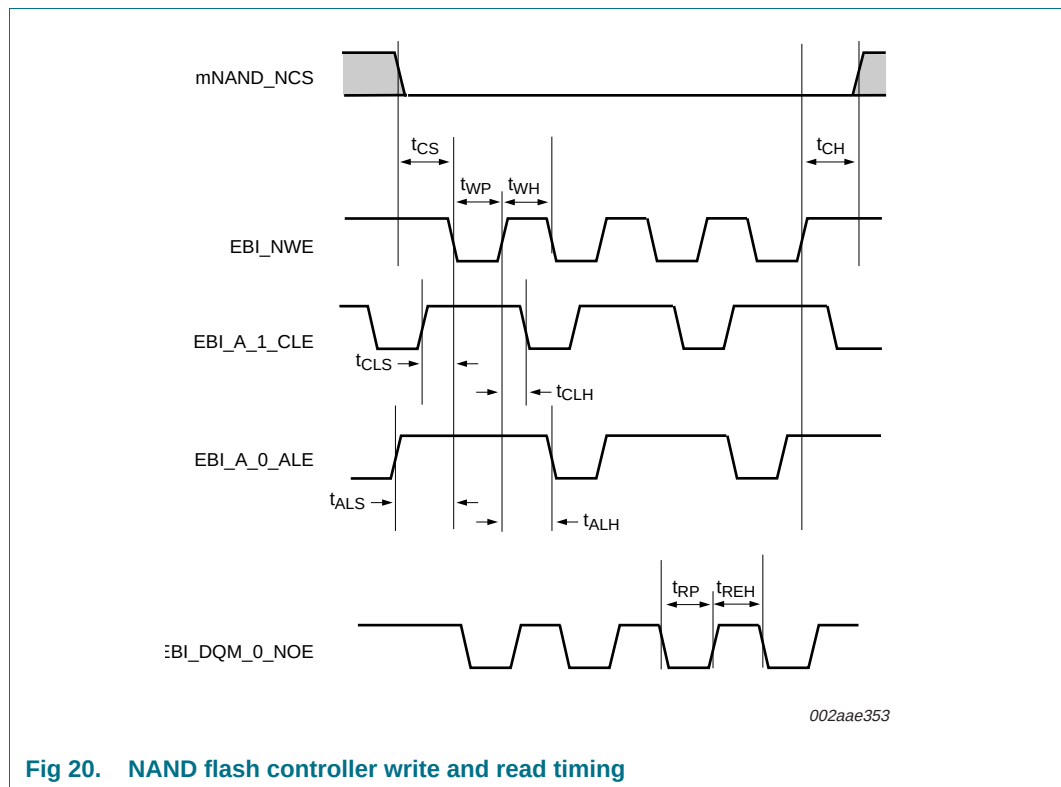


Fig 20. NAND flash controller write and read timing

9.5 Crystal oscillator

Table 20: Dynamic characteristics: crystal oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	oscillator frequency		10	12	25	MHz
δ_{clk}	clock duty cycle		45	50	55	%
C_{xtal}	oscillator capacitance	input; on pin FFAST_IN	-	-	2	pF
		output; on pin FFAST_OUT	-	-	0.74	pF
$t_{startup}$	start-up time		-	500	-	μ s
P_{drive}	drive power		100	-	500	μ W

9.6 SPI

Table 21. Dynamic characteristics of SPI pins

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications

Symbol	Parameter	Min	Typ	Max	Unit
SPI master					
T_{SPICYC}	SPI cycle time	<td>	<td>	<td>	ns
$t_{SPICLK H}$	SPICLK HIGH time	<td>	<td>	<td>	ns
$t_{SPICLK L}$	SPICLK LOW time	<td>	<td>	<td>	ns
t_{SPIDSU}	SPI data set-up time	<td>	<td>	<td>	ns
t_{SPIDH}	SPI data hold time	<td>	<td>	<td>	ns
t_{SPIQV}	SPI data output valid time	<td>	<td>	<td>	ns
t_{SPIOH}	SPI output data hold time	<td>	<td>	<td>	ns
SPI slave					
T_{SPICYC}	SPI cycle time	<td>	<td>	<td>	ns
$t_{SPICLK H}$	SPICLK HIGH time	<td>	<td>	<td>	ns
$t_{SPICLK L}$	SPICLK LOW time	<td>	<td>	<td>	ns
t_{SPIDSU}	SPI data set-up time	<td>	<td>	<td>	ns
t_{SPIDH}	SPI data hold time	<td>	<td>	<td>	ns
t_{SPIQV}	SPI data output valid time	<td>	<td>	<td>	ns
t_{SPIOH}	SPI output data hold time	<td>	<td>	<td>	ns

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagrams.

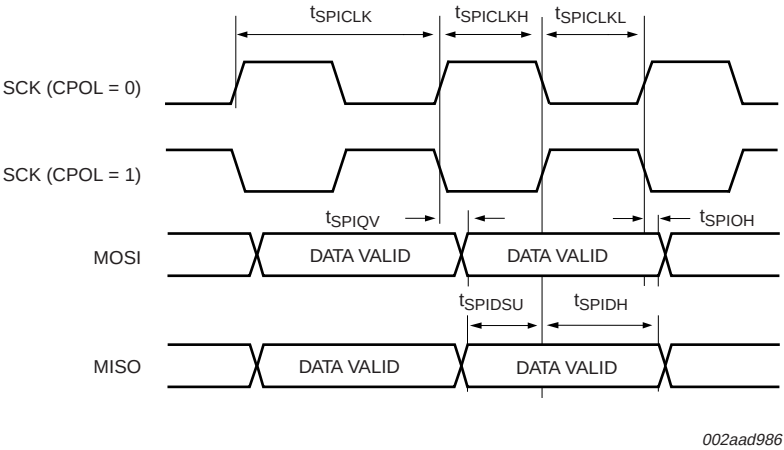


Fig 21. SPI master timing (CPHA = 1)

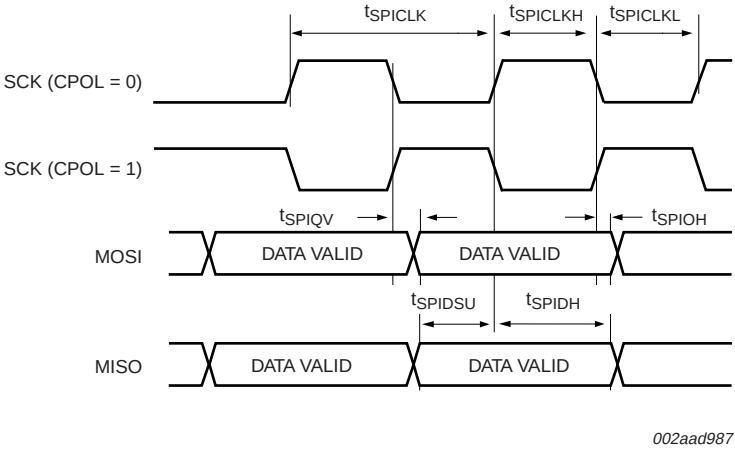
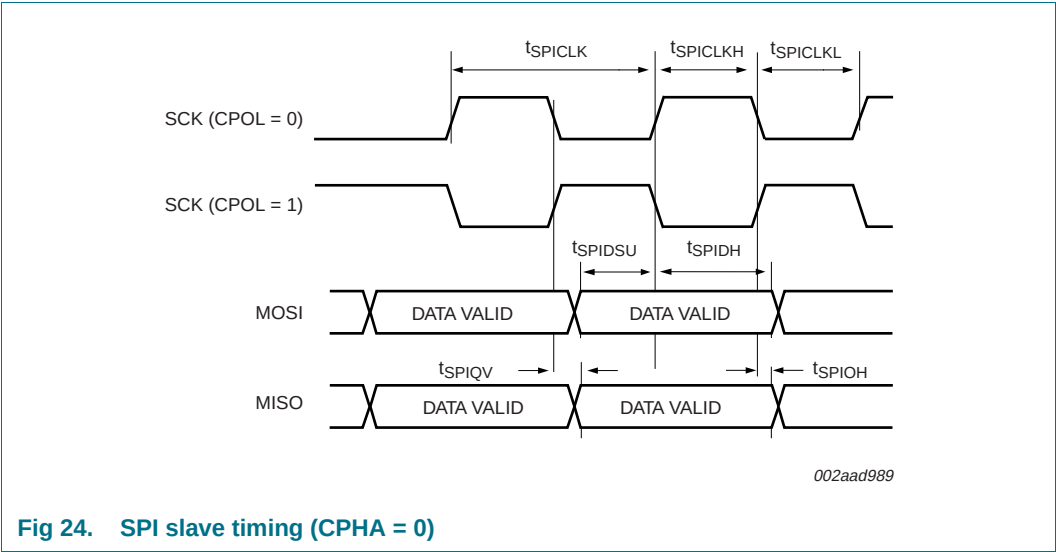
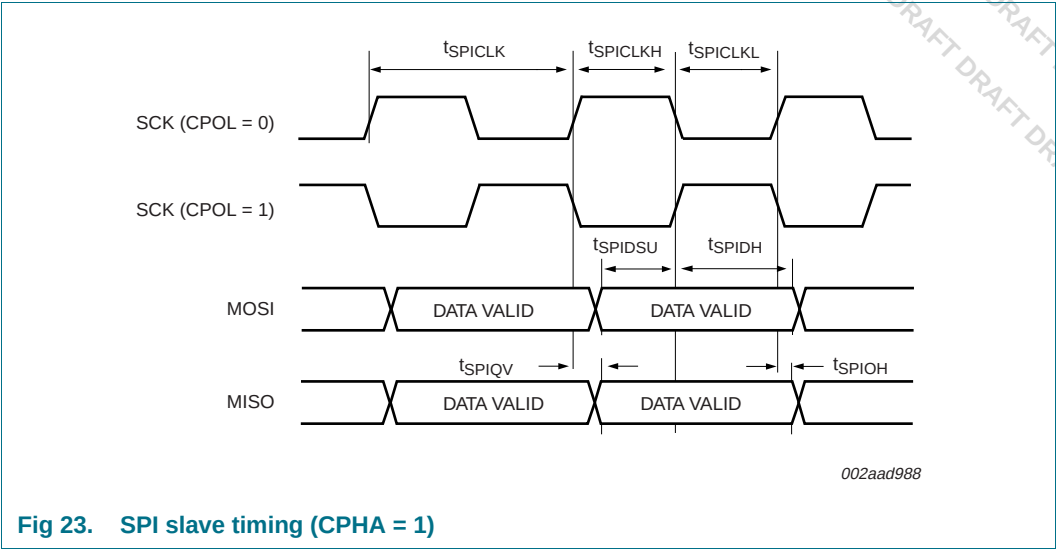


Fig 22. SPI master timing (CPHA = 0)



9.7 I²S-interface

Table 22. Dynamic characteristics: I²S-interface pins

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
common to input and output						
T _{cy(clk)}	clock cycle time		<tbd>	<tbd>	<tbd>	<tbd>
t _f	rise time		<tbd>	<tbd>	<tbd>	<tbd>
t _r	fall time		<tbd>	<tbd>	<tbd>	<tbd>
output						
t _{WH}	pulse width HIGH		<tbd>	<tbd>	<tbd>	<tbd>
t _{WL}	pulse width LOW		<tbd>	<tbd>	<tbd>	<tbd>
t _{v(Q)}	data output valid time	on pin I2STX_DATAx ^[1]	<tbd>	<tbd>	<tbd>	<tbd>
		on pin I2STX_WSx ^[1]	<tbd>	<tbd>	<tbd>	<tbd>
input						
t _{su(d)}	data input set-up time	on pin I2SRX_DATAx ^[1]	<tbd>	<tbd>	<tbd>	<tbd>
		on pin I2SRX_WSx ^[1]	<tbd>	<tbd>	<tbd>	<tbd>
t _{h(d)}	data output hold time	on pin I2SRX_DATAx ^[1]	<tbd>	<tbd>	<tbd>	<tbd>
		on pin I2SRX_WSx ^[1]	<tbd>	<tbd>	<tbd>	<tbd>

[1] x = 0 or 1.

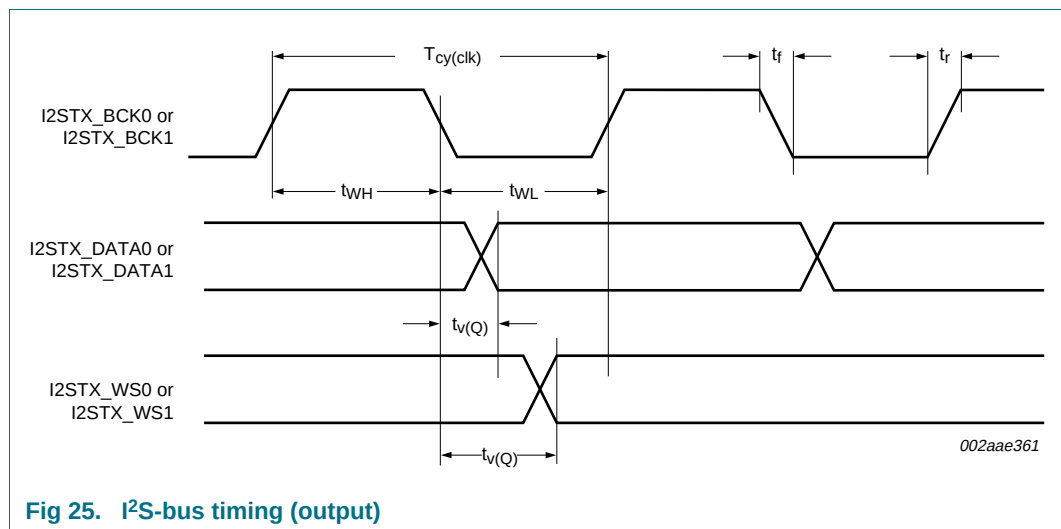
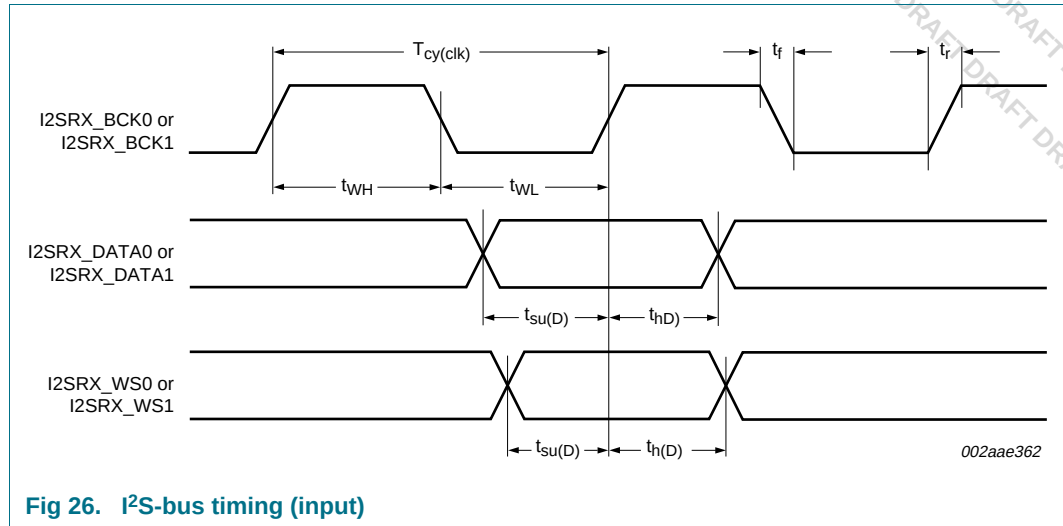


Fig 25. I²S-bus timing (output)



9.8 I²C-bus

Table 23. Dynamic characteristic: I²C-bus pins

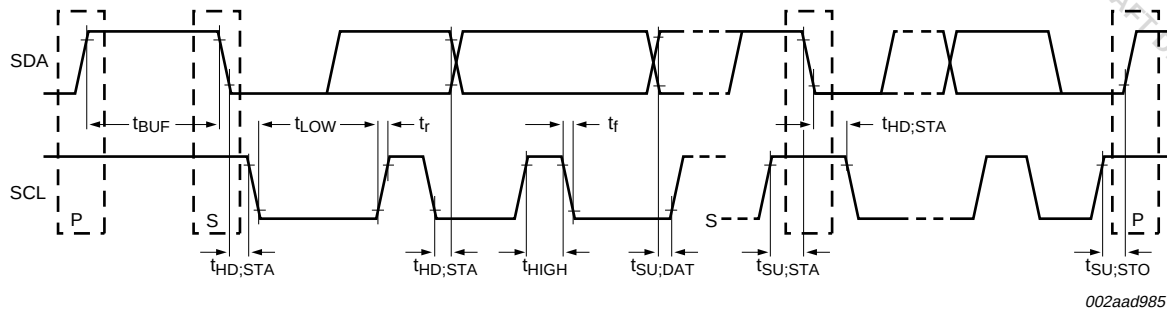
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.^[1]

Symbol	Parameter	Conditions	Min	Typ ^[2]	Max	Unit
f_{SCL}	SCL clock frequency	Standard mode	0	<td>	100	kHz
		Fast mode	0	<td>	400	kHz
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$ ^[3]	-	-	ns
t_r	rise time	Standard mode	<td>	<td>	1000	ns
		Fast mode	$20 + 0.1 \times C_b$ ^[3]	<td>	300	ns
t_f	fall time	Standard mode	<td>	<td>	300	ns
		Fast mode	$20 + 0.1 \times C_b$ ^[3]	<td>	300	ns
t_{BUF}	bus free time between a STOP and START condition	-	<td>	<td>	<td>	
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7	<td>	<td>	μs
		Fast mode	1.3	<td>	<td>	μs
$t_{HD,STA}$	hold time (repeated) START condition	-	<td>	<td>	<td>	
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0	<td>	<td>	μs
		Fast mode	0.6	<td>	<td>	μs
$t_{SU,DAT}$	data set-up time	Standard mode	250	<td>	<td>	ns
		Fast mode	100	<td>	<td>	ns
$t_{SU,STA}$	set-up time for a repeated START condition	-	<td>	<td>	<td>	
$t_{SU,STO}$	set-up time for STOP condition	Standard mode	4.0	<td>	<td>	μs
		Fast mode	0.6	<td>	<td>	μs

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.



Remark: Signals SDA and SCL correspond to pins I2C_SDAx and I2C_SCLx (x = 0, 1).

Fig 27. I²C-bus pins clock timing

9.9 USB interface

Table 24. Dynamic characteristics: USB pins (high-speed)

$C_L = 50 \text{ pF}$; $R_{pu} = 1.5 \text{ k}\Omega$ on D+ to $V_{DD(3V3)}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	<td>	-	<td>	ns
t_f	fall time	10 % to 90 %	<td>	-	<td>	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f	-	-	<td>	%
V_{CRS}	output signal crossover voltage		<td>	-	<td>	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 28	<td>	-	<td>	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 28	<td>	-	<td>	ns
t_{JR1}	receiver jitter to next transition		<td>	-	<td>	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	<td>	-	<td>	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 28	[1] <td>	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 28	[1] <td>	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

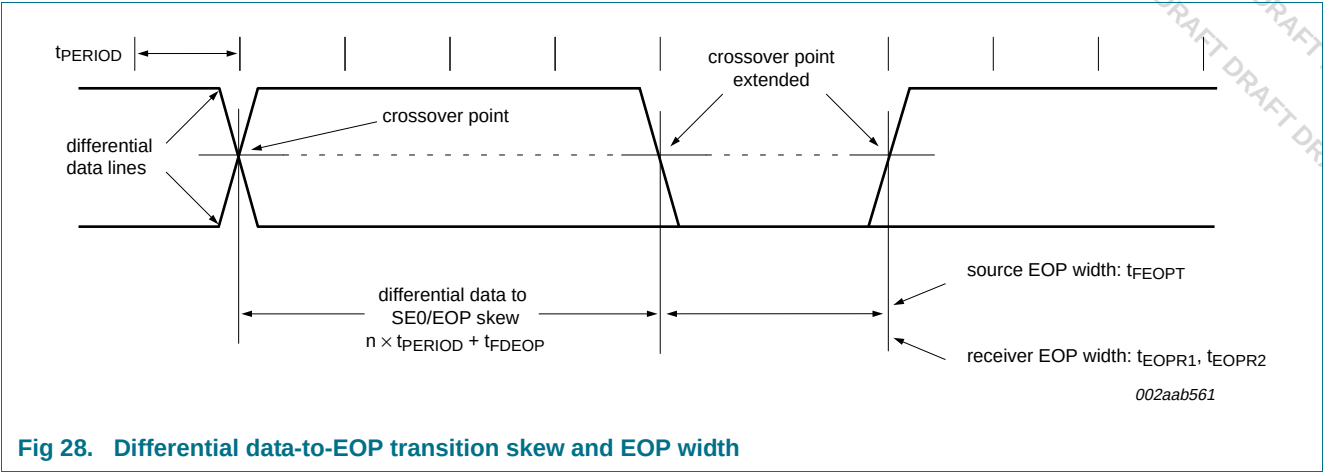


Fig 28. Differential data-to-EOP transition skew and EOP width

9.10 10-bit ADC

Table 25: Dynamic characteristics: 10-bit ADC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_s	sampling frequency	10 bit resolution	400	-	-	k samples/s
		2 bit resolution	-	-	1500	k samples/s
t_{conv}	conversion time	10 bit resolution	-	-	11	clock cycles
		2 bit resolution	3	-	-	clock cycles

10. Application information

Table 26. LCD panel connections

TFBGA pin #	Pin name	Reset function	LCD mode					Serial
			Parallel					
			LCD panel data mapping			Control function		
			16 bit	8 bit	4 bit	6800	8080	
K8	mLCD_CSB/EBI_nSTCS0	mLCD_CSB	-	-	-	LCD_CSB	LCD_CSB	LCD_CSB
L8	mLCD_E_RD/EBI_CKE	mLCD_E_RD	-	-	-	LCD_E	LCD_RD	-
P8	mLCD_RS/EBI_NDYCS	mLCD_RS	-	-	-	LCD_RS	LCD_RS	LCD_RS
N9	mLCD_RW_WR/EBI_DQM1	mLCD_RW_WR	-	-	-	LCD_RW	LCD_WR	-
N8	mLCD_DB0/EBI_CLKOUT	mLCD_DB0	LCD_DB0	-	-	-	-	-
P9	mLCD_DB1/EBI_NSTCS1	mLCD_DB1	LCD_DB1	-	-	-	-	-
N6	mLCD_DB2/EBI_A2	mLCD_DB2	LCD_DB2	-	-	-	-	-
P6	mLCD_DB3/EBI_A3	mLCD_DB3	LCD_DB3	-	-	-	-	-
N7	mLCD_DB3/EBI_A4	mLCD_DB4	LCD_DB4	-	-	-	-	-
P7	mLCD_DB5/EBI_A5	mLCD_DB5	LCD_DB5	-	-	-	-	-
K6	mLCD_DB6/EBI_A6	mLCD_DB6	LCD_DB6	-	-	-	-	-
P5	mLCD_DB3/EBI_A7	mLCD_DB7	LCD_DB7	-	-	-	-	-
N5	mLCD_DB3/EBI_A8	mLCD_DB8	LCD_DB8	LCD_DB0	-	-	-	-
L5	mLCD_DB9/EBI_A9	mLCD_DB9	LCD_DB9	LCD_DB1	-	-	-	-
K7	mLCD_DB10/EBI_A10	mLCD_DB10	LCD_DB10	LCD_DB2	-	-	-	-
N4	mLCD_DB11/EBI_A11	mLCD_DB11	LCD_DB11	LCD_DB3	-	-	-	-
K5	mLCD_DB12/EBI_A12	mLCD_DB12	LCD_DB12	LCD_DB4	LCD_DB0	-	-	-
P4	mLCD_DB13/EBI_A13	mLCD_DB13	LCD_DB13	LCD_DB5	LCD_DB1	-	-	SER_CLK
P3	mLCD_DB14/EBI_A14	mLCD_DB14	LCD_DB14	LCD_DB6	LCD_DB2	-	-	SER_DAT_IN
N3	mLCD_DB15/EBI_A15	mLCD_DB15	LCD_DB15	LCD_DB7	LCD_DB3	-	-	SER_DAT_OUT

11. Marking

Table 27. LPC3130/3131 Marking

Line	Marking	Description
A	LPC3130/3131	BASIC_TYPE

12. Package outline

TFBGA180: thin fine-pitch ball grid array package; 180 balls

SOT570-3

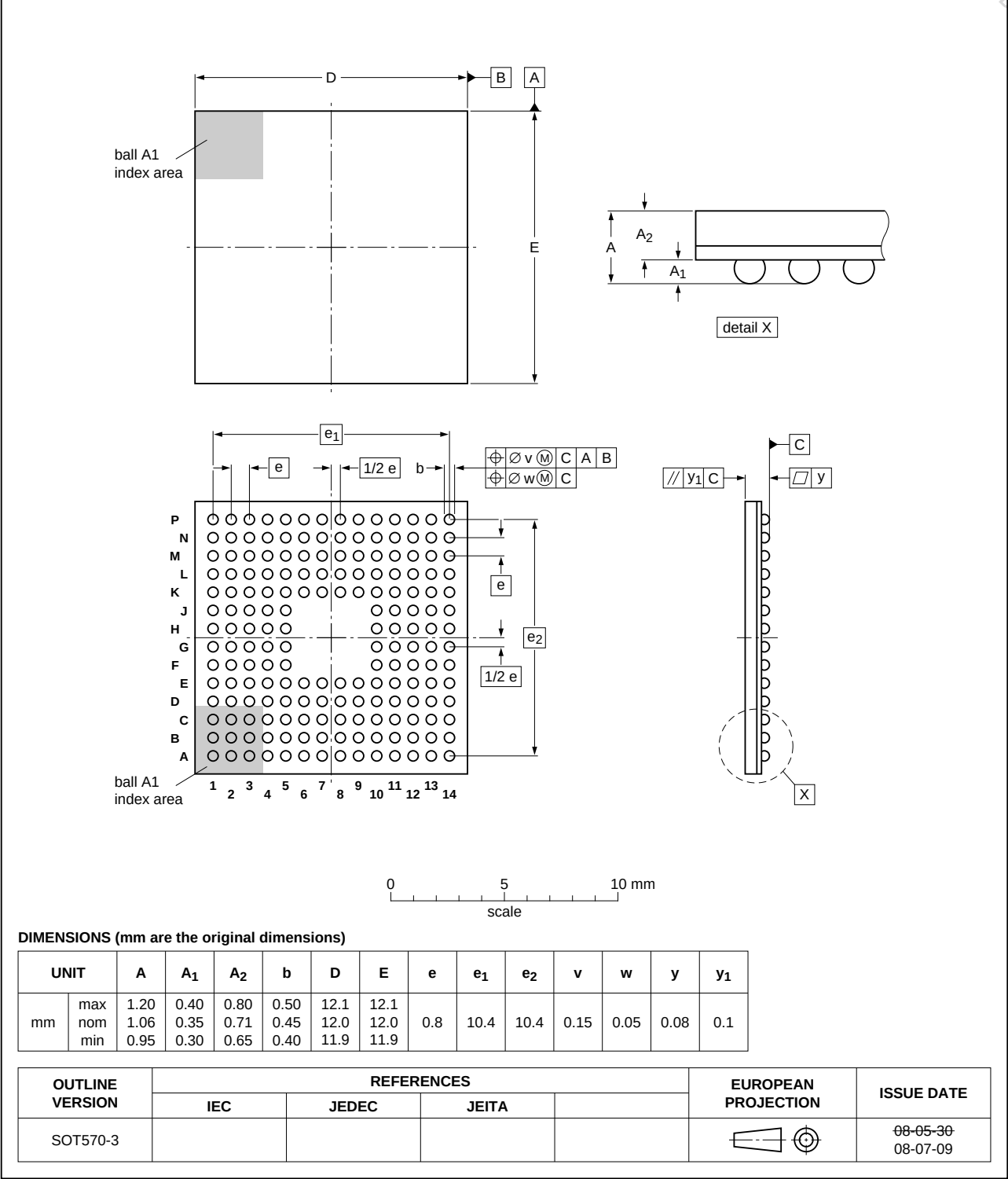


Fig 29. LPC3130/3131 TFBGA180 package outline

13. Abbreviations

Table 28: Abbreviations

Acronym	Description
ADC	Stereo Analog to Digital Converter
ADC10B	10 Bit Analogue to Digital Converter
BIU	Bus Interface Unit
CGU	Clock Generation Unit
DFU	Device Firmware Upgrade
DMA	Direct Memory Access Controller
DRM	Digital Rights Management
ECC	Error Correction Code
I ² C M/S	Inter IC Communication Master/Slave Interface
I ² S	Inter-IC Sound
INTC	Interrupt Controller
IOCONFIG	Input Output Configuration
ROM	ROM Memory
IrDA	Infrared Data Association
ISRAM	Internal Static RAM Memory
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
PHY	Physical Layer
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RNG	Random Number Generator
SIR	Serial IrDA
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
Syscreg	System Control Registers
Timer	Timer module
UART	Universal Asynchronous Receiver Transmitter
USB 2.0 HS OTG	Universal Serial Bus 2.0 High Speed on the Go
WDT	WatchDog Timer

14. Revision history

Table 29: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC3130_3131_0.12	<td>	Preliminary data sheet		LPC3130_3131_0.08
Modifications:				
• SDRAM timing characteristics added. • SRAM dynamic characteristics of t_{su(DQ)} updated in Table 17. • Static characteristics of I/O pins added. • Table 8 "LPC3130/3131 boot modes" added.				
LPC3130_3131_0.08	<td>	Preliminary data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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