ERRATA SHEET

Date: 2008 November 26
Document Release: Version 1.0
Device Affected: LPC2478

This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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NXP Semiconductors

founded by Philips

Document revision history

Rev	Date	Description
1.0	November 26 2008	First version

Identification

The typical LPC2478 devices have the following top-side marking:

LPC2478xxx

xxxxxxx

xxYYWW R[x]

The last/second to last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC2478:

Revision Identifier (R)	Comment
‘C’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
Core.1	Incorrect update of the Abort Link register in Thumb state	C

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Device Revision the deviation occurs in
IRC.1	Accuracy of the Internal RC oscillator (IRC) frequency may be outside of the 4 MHz +/- 1 % specification only at extreme temperatures.	C

Errata Notes

Notes	Short Description	Device Revision the note applies to
Note 1	When the input voltage is Vi ≥ Vdd I/O + 0.5 v on each of the following port pins P0.23, P0.24. P0.25, P0.26, P1.30, P1.31, P0.12, and P0.13 (configured as general purpose input pin (s)), current must be limited to less than 4 mA by using a series limiting resistor.	C

Functional Problems of LPC2478

Core.1 **Incorrect update of the Abort Link register in Thumb state**

Introduction: If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem: In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work around: In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this is would have to be done manually.

AC/DC Deviations

IRC.1 **Accuracy of the Internal RC oscillator (IRC) frequency may be outside of the 4 MHz +/- 1 % specification only at extreme temperatures.**

Introduction: The device has a 4 MHz internal RC oscillator (IRC) which can be optionally used as the clock source for the Watch Dog Timer (WDT), and/or as the clock that drives the PLL and subsequently the CPU. The IRC frequency spec is 4 MHz +/- 1 % accuracy over the entire voltage and temperature range. During In-System Programming (ISP), the auto-baud routine is expecting the IRC frequency to be 4 MHz +/- 1 % and is used to synchronize with the host via serial port 0.

Problem: On the LPC2478 Rev C device only, the accuracy of internal RC oscillator (IRC) frequency meets 4 MHz +/- 1 % specification only at room temperature however, at extreme temperatures, the accuracy of internal RC oscillator (IRC) frequency may be 4 MHz +/- 10 %. As a result, at extreme temperatures, this may affect the auto-baud routine's ability to synchronize with the host via serial port 0 during In-System Programming (ISP) at higher baud rates.

Work around: None

Errata Notes

Note 1: On each of the following port pins P0.23, P0.24. P0.25, P0.26, P1.30, P1.31, P0.12, and P0.13 (when configured as general purpose input pin (s)), leakage current increases when the input voltage is Vi ≥ Vdd I/O + 0.5 v. Care must be taken to limit the current to less than 4 mA by using a series limiting resistor.