

LP5952 Evaluation Board

National Semiconductor
Application Note 1531
Klaus Scheitinger
April 3, 2008



Introduction

This evaluation board is designed to enable independent evaluation of the LP5952 electrical performance. Each board is pre-assembled and tested in the factory.

The evaluation kits are available in four output voltage options for the micro SMD package: LP5952TL-1.2EV, LP5952TL-1.3EV, LP5952TL-1.5EV and LP5952TL-1.8EV and one output voltage option for the COL LLP package: LP5952LC-1.5EV. For other voltage options, the device can be ordered from LP5952 product folder on National's website.

The board contains the LP5952 and input and output capacitors connected to GND.

General Description

The LP5952 converts higher input voltages connected to the power input voltage pin V_{IN} to lower output voltages while consuming low quiescent current. The bias input voltage V_{BATT} supplies internal circuitry.

The LP5952 is capable of operating with input voltage ranges from $0.7V \leq V_{IN} \leq 4.5V$ and $2.5V \leq V_{BATT} \leq 5.5V$ for fixed output voltage options from 0.5V to 2.0V. The LP5952 can supply a maximum output current of 350mA and is particularly suitable for portable, battery-powered systems. It also features internal protection against short-circuit and over-temperature conditions.

The power input voltage applied between V_{IN} and GND should be at least 0.2V above the output voltage and the bias input voltage applied between V_{BATT} and GND should be at least 1.5V above the output voltage (with a minimum of 2.5V) to operate the device within operating conditions. Input connections should be kept reasonably short (<20cm) to minimise input inductance and ensure optimum transient performance.

ON/OFF control of the LP5952 is realized by a logic signal applied to the EN pin. To simplify the enabling of the device, a three pin jumper is provided on the evaluation board. The middle pin is directly connected to the EN pin of the device. A logic signal with a minimum of 1.0V to enable the device or with a maximum of 0.4V to disable the device can be directly connected to this jumper pin in the middle. Alternatively the middle pin can be shorted to the pin next to it to the left or to the right marked ON or OFF.

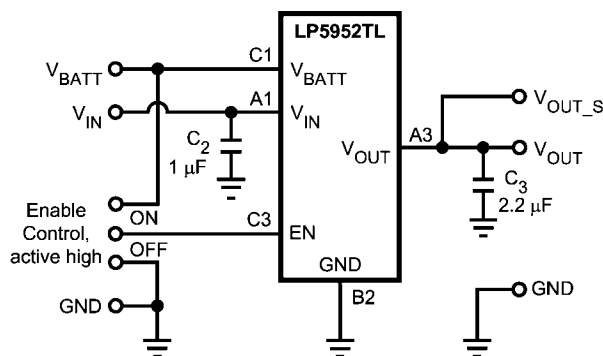
A load of up to 350mA maximum may be connected from the V_{OUT} pin to GND.

At the bottom of the board the output voltage option (1.2V, 1.3V, 1.5V, or 1.8V) is printed.

The V_{OUT_S} pin represents a sense path to the output voltage pin and can be used for more precise voltage measurements.

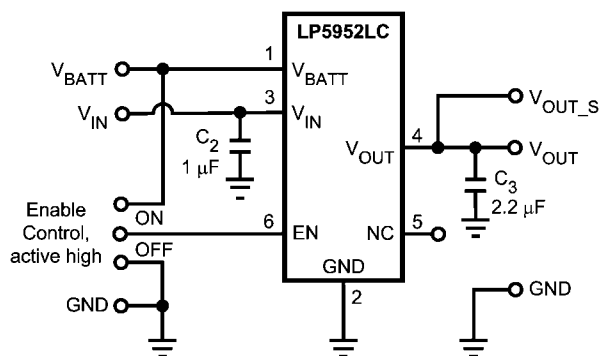
The schematic and board layout for both packages are shown below:

Schematic Diagram



Evaluation Board Schematic (TL Package)

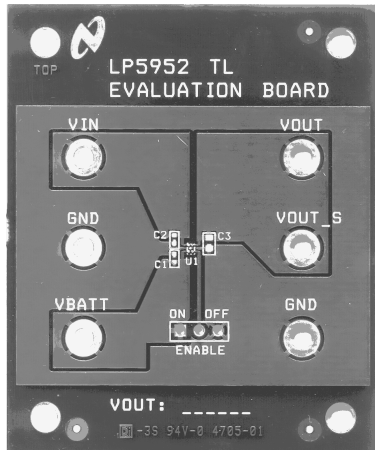
20210201



Evaluation Board Schematic (LC Package)

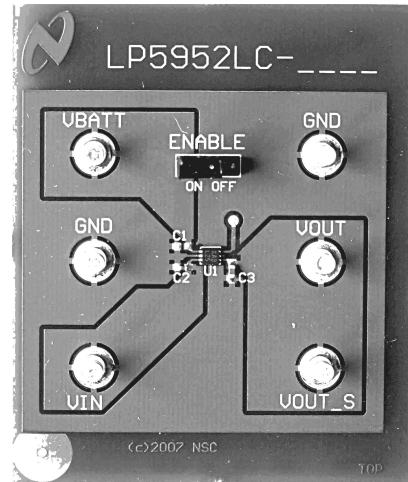
20210207

Evaluation Board Component and Pin Layout



LP5952TL: TOP Side
Board Size: 50mm x 60mm

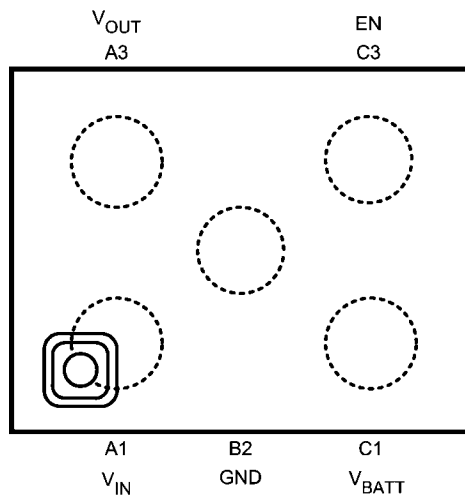
20210202



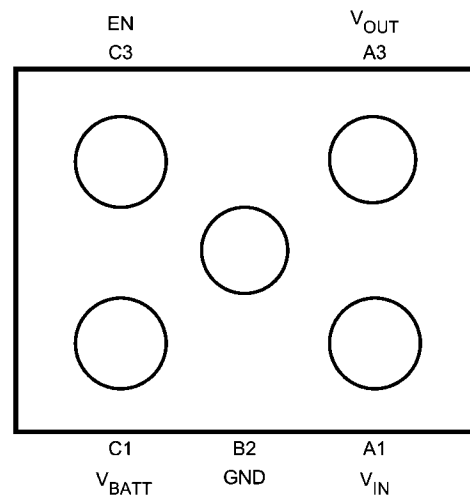
LP5952LC: TOP Side
Board Size: 50mm x 60mm

20210205

Connection Diagrams



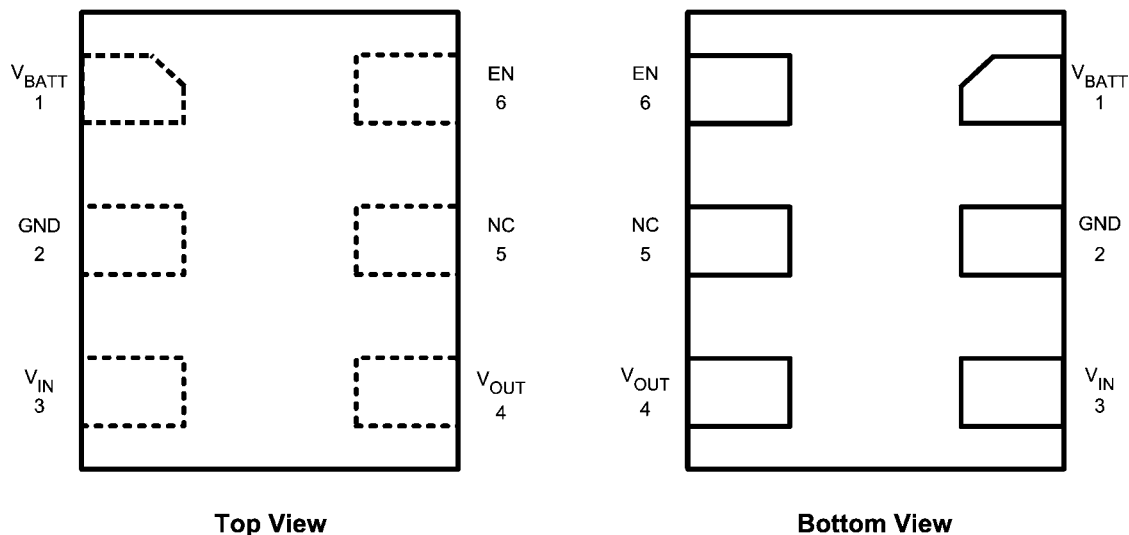
Top View



Bottom View

Connection Diagram 5-Bump Thin Micro SMD Package, Large Bump, 0.5mm Pitch

20210203



Connection Diagram 6-Pin Chip On Lead LLP Package, 0.5mm Pitch

20210212

Table 1: Pin Descriptions

Pin Number Micro SMD	Pin Number LLP	Name	Description
A1	3	V_{IN}	Power input voltage; input range: 0.7V to 4.5V, $V_{IN} \leq V_{BATT}$
A3	4	V_{OUT}	Regulated output voltage
B2	2	GND	Ground
C1	1	V_{BATT}	Bias input voltage; input range: 2.5V to 5.5V
C3	6	EN	Enable pin logic input: low = shutdown, high = active, normal operation. This pin should not be left floating. Short to V_{BATT} using attached jumper for normal operation.
	5	NC	No internal connection

Table 2: Bill of Materials

Item	Description	Amount	Footprint	Mfg., Part Number
C1	C_{BATT} , optional, not needed, capacitor at V_{BATT}	0	0402 / 0201	
C2	C_{IN} , ceramic capacitor, 1 μ F, X5R at V_{IN}	1	0402 / 0201	TDK, C1005X5R1A105K or Taiyo Yuden, LMK105BJ105KV-F
C3	C_{OUT} , ceramic capacitor, 2.2 μ F, X5R at V_{OUT}	1	0603 / 0402	TDK, C1608X5R0J225K or Taiyo Yuden, JMK105BJ225MV-F
U1	Linear Regulator LP5952TL or LP5952LC	1	5-bump micro SMD: TLA05Z1A or 6-pin COL LLP: LCA06B	National Semiconductor, LP5952TL-x.x or LP5952LC-1.5
V_{IN} , V_{BATT} , V_{OUT_S} , V_{OUT} , GND	Test pins	6		Cambion, 160-1026-02-05
ENABLE	3 pin jumper for enable function	1		

Application Hints

DUAL RAIL SUPPLY

The LP5952 requires two different supply voltages:

- V_{IN} , the power input voltage, is regulated to the fixed output voltage

- V_{BATT} , the bias input voltage, supplies internal circuitry.

It's important that V_{IN} does not exceed V_{BATT} at any time. If the device on the evaluation board is used in the typical post regulation application as shown in FIGURE 1 of the datasheet using a DC-DC converter to generate V_{IN} out of V_{BATT} , the sequencing of the two power supplies is not an issue as V_{BATT} supplies both, the DC-DC regulator and the LP5952. The output voltage of the DC-DC regulator will take some time to rise up and supply V_{IN} of LP5952. In this application V_{IN} will always ramp up more slowly than V_{BATT} .

In case V_{IN} is shorted to V_{BATT} , the voltages at the two supply pins will ramp up simultaneously causing no problem.

If the LP5952 evaluation board is used stand alone, two independent supplies are connected to the LP5952. Therefore special care must be taken to guarantee that **V_{IN} is always $\leq V_{BATT}$** .

POWER DISSIPATION AND DEVICE OPERATION

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die and ambient air.

The allowable power dissipation for the device in a given package can be calculated using the following equation:

$$P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$$

With a $\theta_{JA} = 95^\circ\text{C/W}$, the device in the 5 bump micro SMD package returns a value of 1053mW with a maximum junction temperature of 125°C at T_A of 25°C or 421mW at T_A of 85°C .

With a $\theta_{JA} = 150^\circ\text{C/W}$, the device in the 6-pin COL LLP package returns a value of 667mW with a maximum junction temperature of 125°C at T_A of 25°C or 267mW at T_A of 85°C .

The actual power dissipation across the device can be estimated by the following equation:

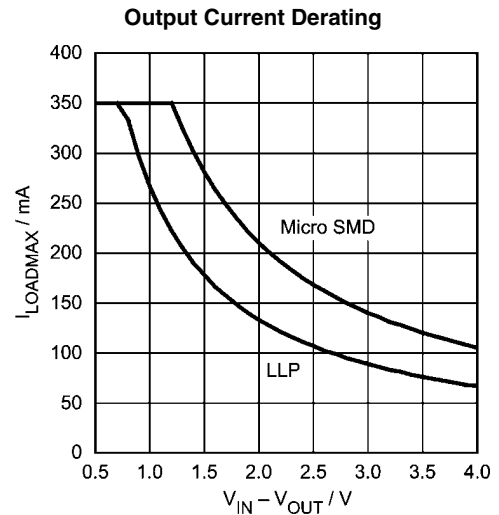
$$P_D \approx (V_{IN} - V_{OUT}) * I_{OUT}$$

This establishes the relationship between the power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application. As an example for the micro SMD package, to keep full load

current capability of 350mA for a 1.5V output voltage option at a high ambient temperature of 85°C , V_{IN} has to be kept $\leq 2.7\text{V}$:

$$V_{IN} \leq P_D / I_{OUT} + V_{OUT} = 421\text{mW} / 350\text{mA} + 1.5\text{V} = 2.7\text{V}.$$

The figure below shows the output current derating due to these considerations:



20210211

Maximum Load Current vs $V_{IN} - V_{OUT}$
 $T_A = 85^\circ\text{C}$, $\theta_{JA(\text{MICROSMD})} = 95^\circ\text{C/W}$, $\theta_{JA(\text{LLP})} = 150^\circ\text{C}$

The typical contribution of the bias input voltage supply V_{BATT} to the power dissipation can be neglected: $P_{D_VBATT} = V_{BATT} * I_{Q_VBATT} = 5.5\text{V} * 50\mu\text{A} = 0.275\text{mW}$ typical.

EXTERNAL CAPACITORS

If the LP5952 evaluation board is used stand alone (V_{IN} and V_{BATT} directly connected to a dual power supply), an input capacitor at V_{IN} (C2) is required for stability. A ceramic capacitor of $1.0\mu\text{F}$ is recommended and assembled at the power input pin V_{IN} .

A capacitor at V_{BATT} (C1) is not required if the distance to the supply does not exceed 5cm. Therefore no capacitor is assembled by default, but a footprint is provided on the evaluation board.

At the output (C3) a $2.2\mu\text{F}$ ceramic capacitor is recommended and assembled.

For further details on recommended capacitors and capacitor characteristics please see bill of materials above and the datasheet.

Notes

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
Wireless (PLL/VCO)	www.national.com/wireless		

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2008 National Semiconductor Corporation

For the most current product information visit us at www.national.com



**National Semiconductor
Americas Technical
Support Center**
Email:
new.feedback@nsc.com
Tel: 1-800-272-9959

**National Semiconductor Europe
Technical Support Center**
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

**National Semiconductor Asia
Pacific Technical Support Center**
Email: ap.support@nsc.com

**National Semiconductor Japan
Technical Support Center**
Email: jpn.feedback@nsc.com