

# LP38513S-1.8 Evaluation Board

National Semiconductor  
Application Note 1518  
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## Introduction

This board is designed to enable the evaluation of the LP38513S-1.8 Voltage Regulator. Each board is assembled and tested in the factory. This evaluation board has the TO-263 5-lead package mounted.

## General Description

The LP38513 is a linear regulator capable of supplying up to 3A of output current, and incorporates Enable and Error flag features.

The device has been designed to work with 10  $\mu\text{F}$  ceramic input and output capacitors. Footprints areas for  $C_{\text{IN}}$  and  $C_{\text{OUT}}$  will allow for a variety of sizes.

## Operation

The input voltage, applied between  $V_{\text{IN}}$  and GND, should be at least 2.25V, and no higher than 5.5V.

Loads can be connected to  $V_{\text{OUT}}$  with reference to GND.

Test points are provided on the board to allow monitoring of  $V_{\text{OUT}}$ ,  $V_{\text{IN}}$ , Enable, and ERROR signals during operation

If the application does not require the Enable function, the EN pin should be connected directly to the adjacent  $V_{\text{IN}}$  pin.

## Enable Operation

The Enable On/Off threshold is typically 850 mV, and has no hysteresis. The voltage signal must rise and fall cleanly, and promptly, through this threshold.

The Enable pin (EN) has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated either actively or passively.

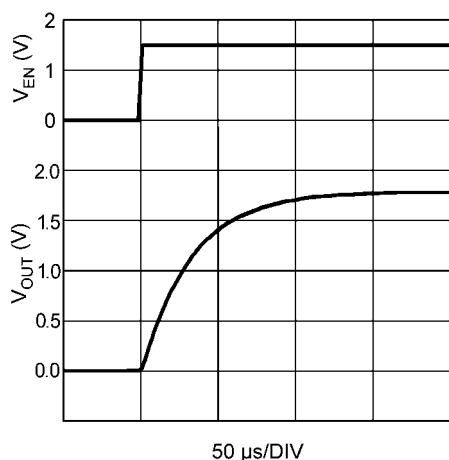


FIGURE 1.  $V_{\text{OUT}}$  vs.  $V_{\text{EN}}$

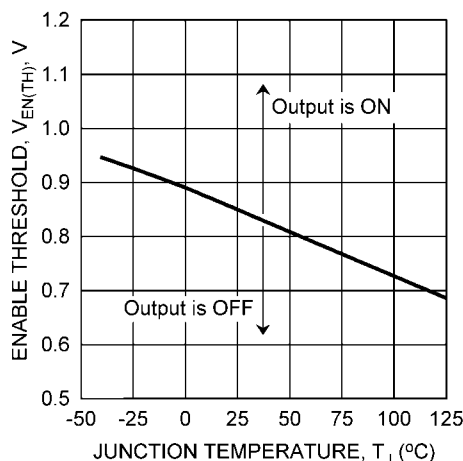
If the Enable pin is driven from a single ended device (such as the collector of a discrete transistor) a pull-up resistor to  $V_{\text{IN}}$ , or a pull-down resistor to ground, will be required for

proper operation. A 1 k $\Omega$  to 100 k $\Omega$  resistor can be used as the pull-up or pull-down resistor to establish default condition for the EN pin. The resistor value selected should be appropriate to swamp out any leakage in the external single ended device, as well as any stray capacitance.

If the Enable pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator output), the pull-up, or pull-down, resistor is not required.

If the application does not require the Enable function, the EN pin should be connected directly to the adjacent  $V_{\text{IN}}$  pin.

The status of the Enable pin also affects the behavior of the ERROR Flag. While the Enable pin is high the regulator control loop will be active and the ERROR Flag will report the status of the output voltage. When the Enable pin is taken low the regulator control loop is shutdown, the output is turned off, and the internal logic will immediately force the ERROR Flag pin low.



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FIGURE 2. Enable Threshold

## ERROR Flag

When the LP38513 Enable pin is high, the ERROR Flag pin will produce a logic low signal when the output drops by more than 10% (typical) from the nominal output voltage. The drop in output voltage may be due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The output voltage will need to rise to within 5% of the nominal output voltage for the ERROR Flag to return to a logic high state. It should also be noted that when the Enable pin is pulled low, the ERROR Flag pin is forced to be low as well.

The internal ERROR flag comparator has an open drain output stage. Hence, the ERROR pin requires an external pull-up resistor. The value of the pull-up resistor should be in the range of 2 k $\Omega$  to 100 k $\Omega$ , and should be connected to the LP38513 output voltage pin. The ERROR Flag pin should not be pulled-up to any voltage source higher than  $V_{\text{IN}}$  as current flow through an internal parasitic diode may cause unexpected behavior. When the input voltage is less than typically

1.25V the status of the  $\overline{\text{ERROR}}$  flag output will not be reliable. The  $\overline{\text{ERROR}}$  Flag pin must be connected to ground if this function is not used.

The timing diagram in Figure 4 shows the relationship between the  $\overline{\text{ERROR}}$  flag and the output voltage when the pull-up resistor is connected to the output voltage pin.

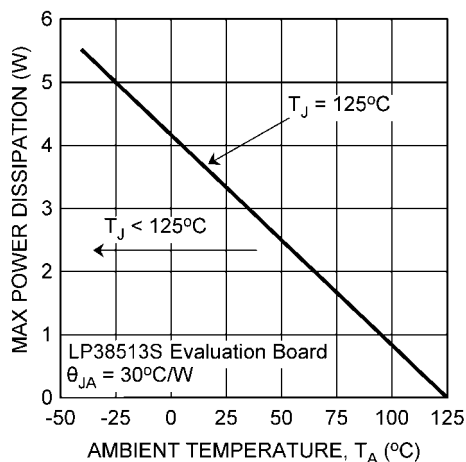
The timing diagram in Figure 5 shows the relationship between the  $\overline{\text{ERROR}}$  flag and the output voltage when the pull-up resistor is connected to the input voltage pin.

## Power Dissipation

The TO-263 package alone has a junction to ambient thermal resistance ( $\theta_{JA}$ ) rating of 60°C/W. When mounted on the LP38513S evaluation board the  $\theta_{JA}$  rating is approximately 30°C/W.

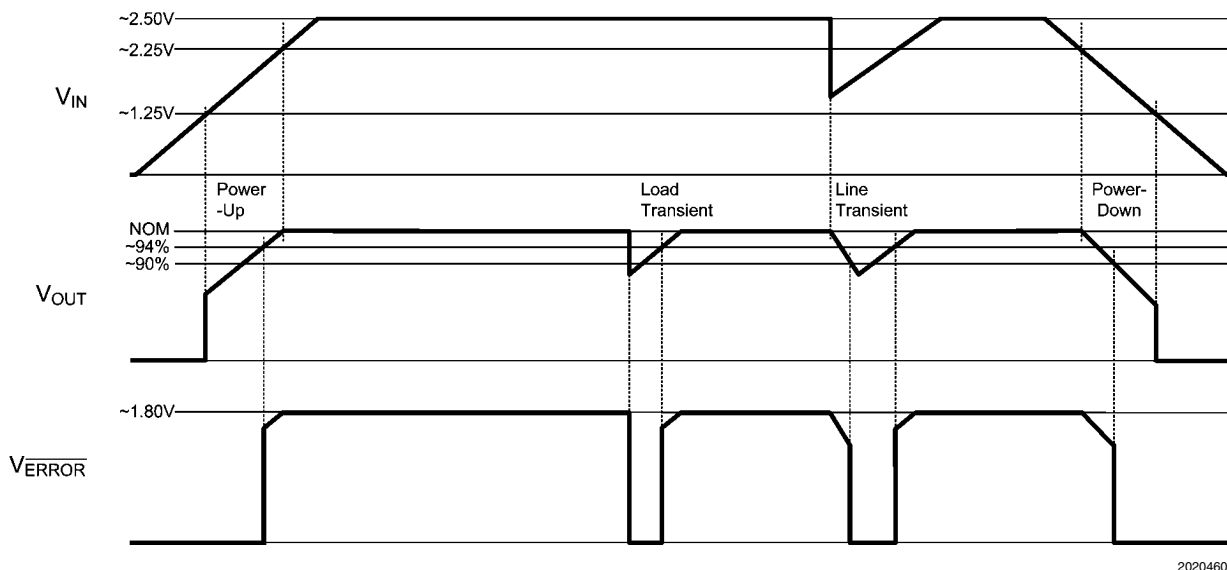
Although there is only approximately 0.28 square inches of 1 ounce copper area immediately under the tab, the top copper surface area is extended to an additional copper area, 1 square inch of 1 ounce copper, on the bottom of the board by the use of nine thermal vias.

With the 30°C/W thermal rating the LP38513S-1.8 evaluation board will deliver the rated 3A output current if  $V_{IN} = 2.5V$ ,  $V_{OUT} = 1.8V$ , and  $T_A \leq 25^\circ\text{C}$ .



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FIGURE 3. Maximum Power Dissipation vs. Ambient Temperature



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FIGURE 4.  $\overline{\text{ERROR}}$  Flag when Pull-Up is from  $V_{OUT}$

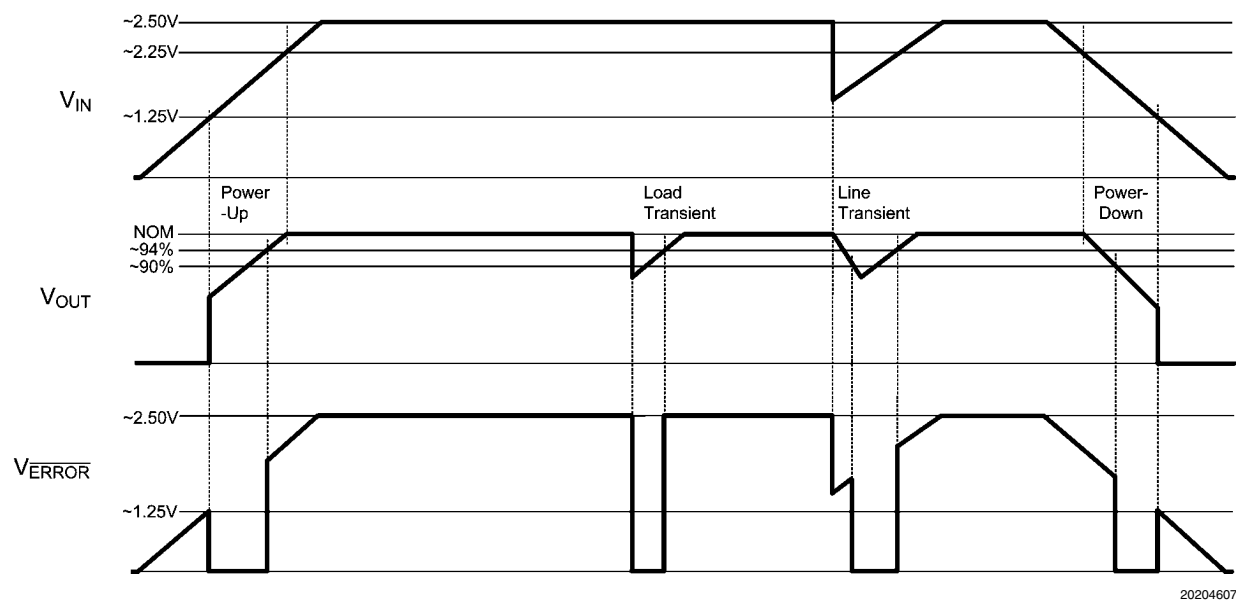
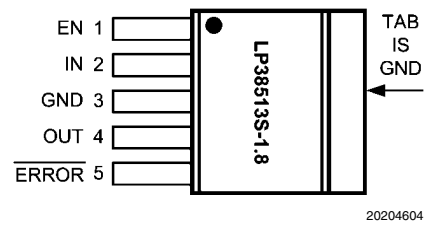
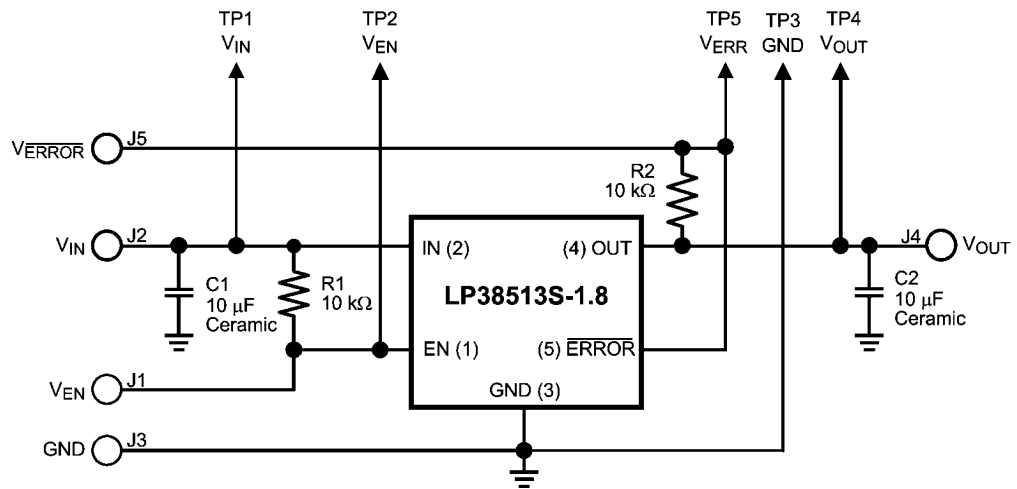


FIGURE 5.  $\overline{ERROR}$  Flag when Pull-Up is from  $V_{IN}$

## Connection Diagram

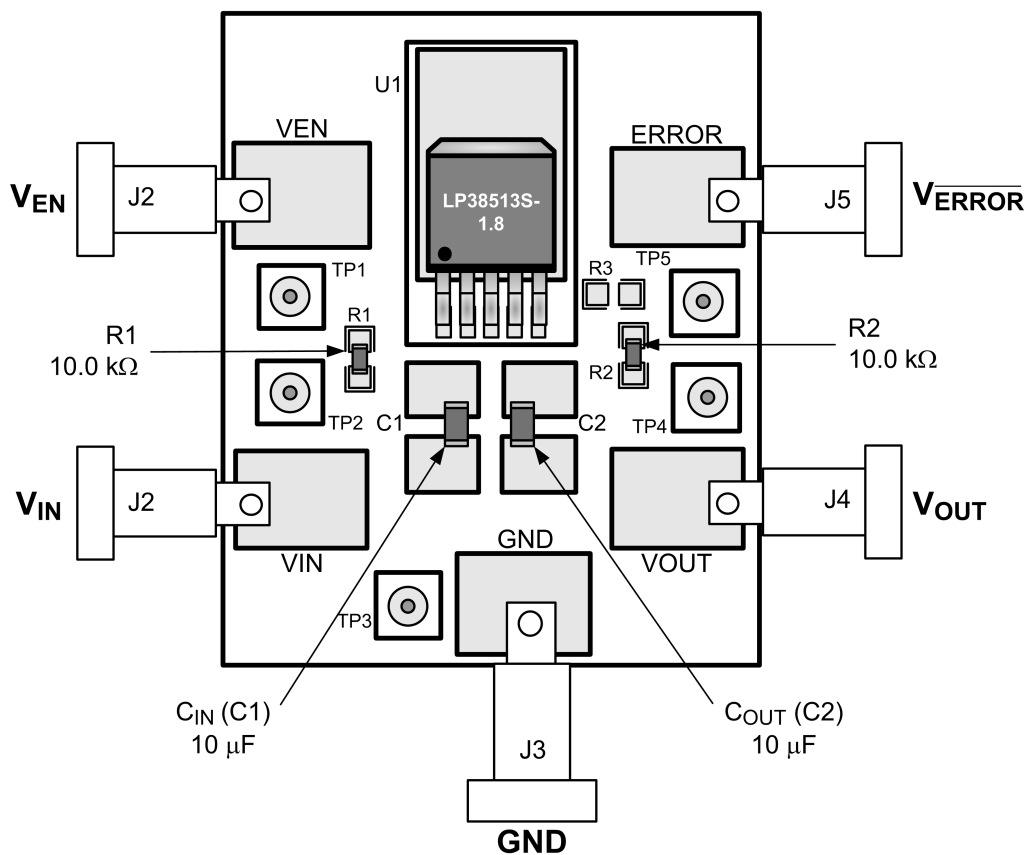


## Schematic Diagram



Evaluation Board Schematic

# PCB Layout



Evaluation Board Component and Pin Layout

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## Bill of Materials

ID	Name	Description	Manufacturer	Part Number
U1	U1	LP38513S-1.8 NOPB	National Semiconductor Corporation	LP38513S-1.8 NOPB
C1	C <sub>IN</sub>	10 $\mu$ F, 10%, MLCC, 10V, X7R, 1210	AVX	1210ZC106KAT2A
C2	C <sub>OUT</sub>	10 $\mu$ F, 10%, MLCC, 10V, X7R, 1210	AXV	1210ZC106KAT2A
J1	V <sub>EN</sub>	Banana Jack : Insulated Solder Terminal ; White	Johnson Components	108-0901-001
J2	V <sub>IN</sub>	Banana Jack : Insulated Solder Terminal ; Red		108-0902-001
J3	GND	Banana Jack : Insulated Solder Terminal ; Black		108-0903-001
J4	V <sub>OUT</sub>	Banana Jack : Insulated Solder Terminal ; Orange		108-0906-001
J5	V <sub>ERR</sub>	Banana Jack : Insulated Solder Terminal ; Blue		108-0910-001
R1	—	Resistor: 10 k $\Omega$ $\pm$ 1%; 0805	Vishay Dale	CRCW 0805 1002 F
R2	—	Resistor: 10 k $\Omega$ $\pm$ 1%; 0805	Vishay Dale	CRCW 0805 1002 F
R3	—	Not Installed	N/A	N/A
TP1	TP <sub>EN</sub>	Turret Terminal : Mounting Hole Diameter = 0.062"	Keystone	1593-2
TP2	TP <sub>IN</sub>			
TP3	TP <sub>GND</sub>			
TP4	TP <sub>OUT</sub>			
TP5	TP <sub>BIAS</sub>			

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