National Semiconductor

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LMX2531LQ1500E
High Performance Frequency Synthesizer System with Integrated VCO

General Description

The LMX2531LQ1500E is a low power, high performance frequency synthesizer system which includes a fully integrated delta-sigma PLL and VCO with fully integrated tank circuit. The third and fourth poles are also integrated and also adjustable. Also included are integrated ultra-low noise and high precision LDOs for the PLL and VCO which give higher supply noise immunity and also more consistent performance. When combined with a high quality reference oscillator, the LMX2531LQ1500E generates very stable, low noise local oscillator signals for up and down conversion in wireless communication devices. The LMX2531LQ1500E is a monolithic integrated circuit, fabricated in an advanced BiCMOS process. There are several different versions of this product in order to accomdate different frequency bands.

Device programming is facilitated using a three-wire MICROWIRE Interface that can operate down to 1.8 volts.

Supply voltage range is 2.8 to 3.2 Volts. The LMX2531LQ1500E is available in a 36 pin 6x6x0.8 mm Lead-Free Leadless Leadframe Package (LLP).

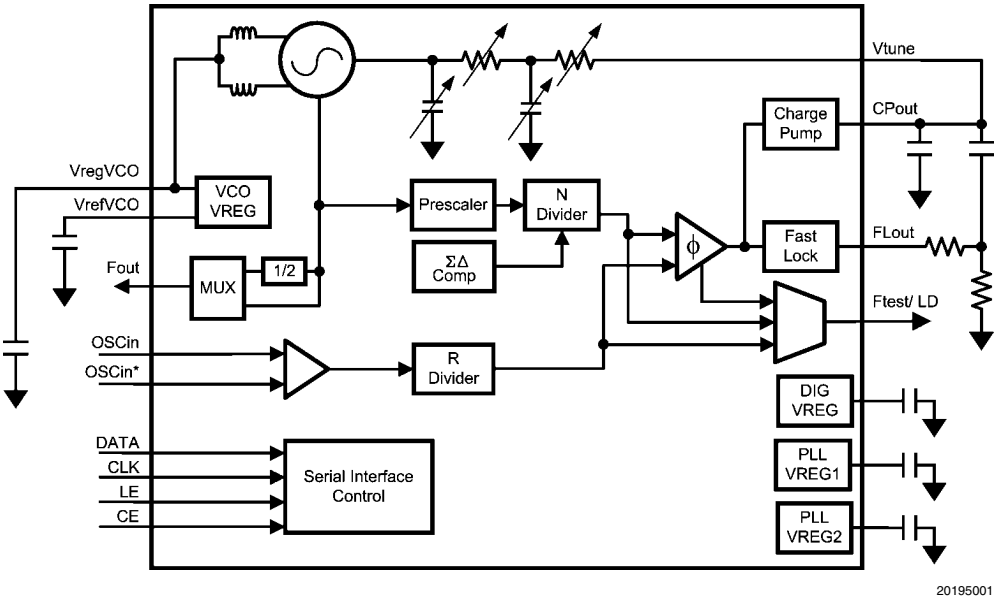
Features

- **PLL Features**
  - — Fractional-N Delta Sigma Modulator Order programmable up to 4th order
  - — FastLock/Cycle Slip Reduction with Timeout Counter
  - — Partially integrated, adjustable Loop Filter
  - — Very low phase noise and spurs
- **VCO Features**
  - — Integrated tank inductor
  - — Low phase noise
  - — 1499 - 1510 MHz Output Frequency
  - — 749.5 - 755 MHz Output Frequency (Divide by 2 Mode)
- **Other Features**
  - — 2.8 V to 3.2 V Operation
  - — Low Power-Down Current
  - — 1.8V MICROWIRE Support
  - — Package: 36 Lead LLP

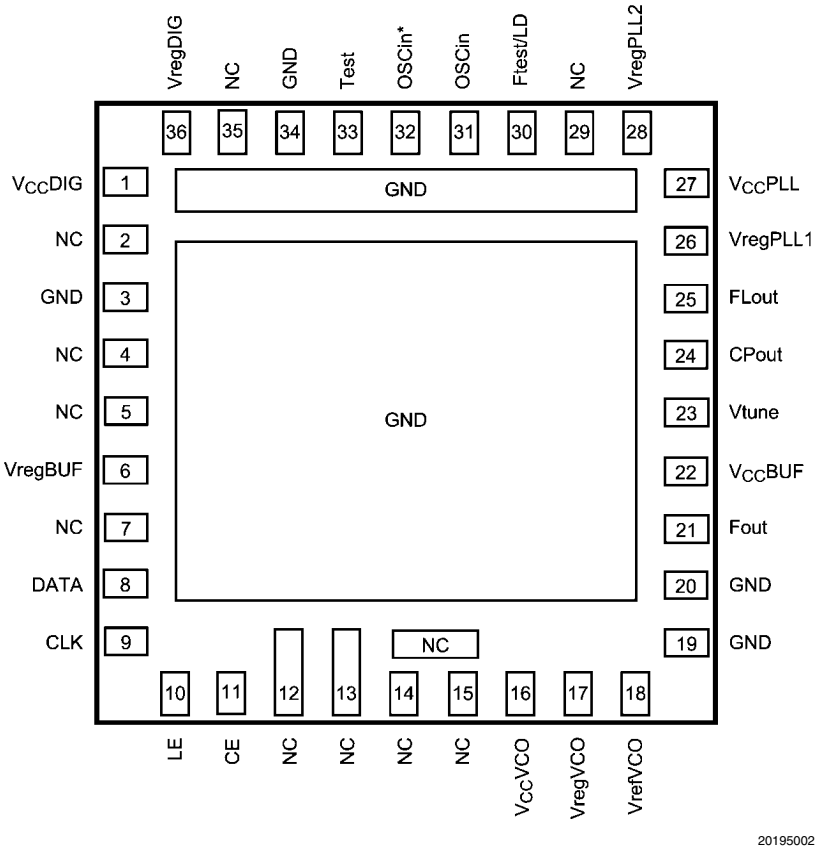
Target Applications

- Data Converting Clocking

Functional Block Diagram



Connection Diagram



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Pin Descriptions

Pin #	Pin Name	I/O	Description
1	VccDIG	-	Power Supply for digital LDO circuitry. Input may range from 2.8 - 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
3	GND	-	Ground
2,4,5,7, 12, 13, 29, 35	NC	-	No Connect.
6	VregBUF	-	Internally regulated voltage for the VCO buffer circuitry. Connect to ground with a capacitor.
8	DATA	I	MICROWIRE serial data input. High impedance CMOS input. This pin must not exceed 2.75V. Data is clocked in MSB first. The last bits clocked in form the control or register select bits.
9	CLK	I	MICROWIRE clock input. High impedance CMOS input. This pin must not exceed 2.75V. Data is clocked into the shift register on the rising edge.
10	LE	I	MICROWIRE Latch Enable input. High impedance CMOS input. This pin must not exceed 2.75V. Data stored in the shift register is loaded into the selected latch register when LE goes HIGH.
11	CE	I	Chip Enable Input. High impedance CMOS input. This pin must not exceed 2.75V. When CE is brought high the LMX2531LQ1500E is powered up corresponding to the internal power control bits. It is necessary to reprogram the R0 register to get the part to re-lock.
14, 15	NC	-	No Connect. Do NOT ground.
16	VccVCO	-	Power Supply for VCO regulator circuitry. Input may range from 2.8 - 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
17	VregVCO	-	Internally regulated voltage for VCO circuitry. Not intended to drive an external load. Connect to ground with a capacitor and some series resistance.

Pin #	Pin Name	I/O	Description
18	VrefVCO	-	Internal reference voltage for VCO LDO. Not intended to drive an external load. Connect to ground with a capacitor.
19	GND	-	Ground for the VCO circuitry.
20	GND	-	Ground for the VCO Output Buffer circuitry.
21	Fout	O	Buffered RF Output for the VCO.
22	VccBUF	-	Power Supply for the VCO Buffer circuitry. Input may range from 2.8 - 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
23	Vtune	I	Tuning voltage input for the VCO. For connection to the CPout Pin through an external passive loop filter.
24	CPout	O	Charge pump output for PLL. For connection to Vtune through an external passive loop filter.
25	FLout	O	An open drain NMOS output which is used for FastLock or a general purpose output.
26	VregPLL1	-	Internally regulated voltage for PLL charge pump. Not intended to drive an external load. Connect to ground with a capacitor.
27	VccPLL	-	Power Supply for the PLL. Input may range from 2.8 - 3.2 V. Bypass capacitors should be placed as close as possible to this pin and ground.
28	VregPLL2	-	Internally regulated voltage for RF digital circuitry. Not intended to drive an external load. Connect to ground with a capacitor.
30	Ftest/LD	O	Multiplexed CMOS output. Typically used to monitor PLL lock condition.
31	OSCin	I	Oscillator input.
32	OSCin*	I	Oscillator complimentary input. When a single ended source is used, then a bypass capacitor should be placed as close as possible to this pin and be connected to ground.
33	Test	O	This pin if for test purposes and should be grounded for normal operation.
34	GND	-	Ground
36	VregDIG	-	Internally regulated voltage for LDO digital circuitry.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Parameter	Symbol	Ratings	Units
Power Supply Voltage	V_{CC} (VccDIG, VccVCO, VccBUF, VccPLL)	-0.3 to 3.5	V
	All other pins (Except Ground)	-0.3 to 3.0	
Storage Temperature Range	T_{STG}	-65 to 150	°C
Lead Temperature (solder 4 sec.)	T_L	+ 260	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage (VccDig, VccVCO, VccBUF)	Vcc	2.8	3.0	3.2	V
Serial Interface and Power Control Voltage	V_i	0		2.75	V
Ambient Temperature (Note 3)	T_A	-40		+85	°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only to the test conditions listed.

Electrical Characteristics (V_{CC} = 3.0 V, -40°C ≤ T_A ≤ 85 °C; f_{Fout} = 1500 MHz, except as specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Current Consumption						
I_{CC}	Power Supply Current	Divider Disabled		34	41	mA
		Divider Enabled		37	46	
$I_{CC}PD$	Power Down Current	CE = 0 V, Part Initialized		7		µA
Oscillator						
$I_{IH}OSC$	Oscillator Input High Current	V_{IH} = 2.75 V			100	µA
$I_{IL}OSC$	Oscillator Input Low Current	V_{IL} = 0	-100			µA
f_{OSCin}	Frequency Range		5		80	MHz
v_{OSCin}	Oscillator Sensitivity		0.5		2.0	Vpp
PLL						
f_{COMP}	Phase Detector Frequency				32	MHz
I_{CPout}	Charge Pump Output Current Magnitude	ICP = 0		90		µA
		ICP = 1		180		µA
		ICP = 3		360		µA
		ICP = 15		1440		µA
$I_{CPout}TRI$	CP TRI-STATE Current	0.4 V < V_{CPout} < 2.0 V		2	10	nA
$I_{CPout}MM$	Charge Pump Sink vs. Source Mismatch	V_{CPout} = 1.2 V, T_A = 25°C		2	8	%
$I_{CPout}V$	Charge Pump Current vs. CP Voltage Variation	0.4 V < V_{CPout} < 2.0 V, T_A = 25°C		4		%
$I_{CPout}T$	CP Current vs. Temperature Variation	V_{CPout} = 1.2 V		8		%
LN(f)	Normalized Phase Noise Contribution (Note 2)	ICP = 1X Charge Pump Gain, 4 kHz Offset		-202		dBc/Hz
		ICP = 16X Charge Pump Gain, 4 kHz Offset		-212		

Symbol	Parameter	Conditions		Min	Typ	Max	Units
VCO Frequencies							
f_{Fout}	Operating Frequency Range			1499		1510	MHz
Other VCO Specifications							
p_{Fout}	Output Power to a 50Ω/5pF Load (Applies across entire tuning range.)	Divider Disabled		1.0	3.5	7.0	dBm
		Divider Enabled		1.0	3.0	6.0	dBm
K_{Vtune}	Fine Tuning Sensitivity (When a range is displayed in the typical column, indicates the lower sensitivity is typical at the lower end of the tuning range, and the higher tuning sensitivity is typical at the higher end of the tuning range.)				4-7		MHz/V
HS_{Fout}	Harmonic Suppression (Applies Across Entire Tuning Range)	2nd Harmonic, 50Ω / 5pF Load	Divider Disabled		-30	-25	dBc
			Divider Enabled		-20	-15	
		3rd Harmonic, 50Ω / 5pF Load	Divider Disabled		-40	-35	
			Divider Enabled		-25	-20	
$PUSH_{Fout}$	Frequency Pushing	Creg = 0.1uF, V_{DD} ± 100mV, Open Loop			300		kHz/V
$PULL_{Fout}$	Frequency Pulling	VSWR=2:1, Open Loop				±600	kHz
Z_{Fout}	Output Impedance				50		Ω
VCO Phase Noise (Note 4)							
$L(f)_{Fout}$	Phase Noise	f_{Fout} = 1500 MHz	10 kHz Offset		-97		dBc/Hz
			100 kHz Offset		-120		
			1 MHz Offset		-142		
			5 MHz Offset		-155		

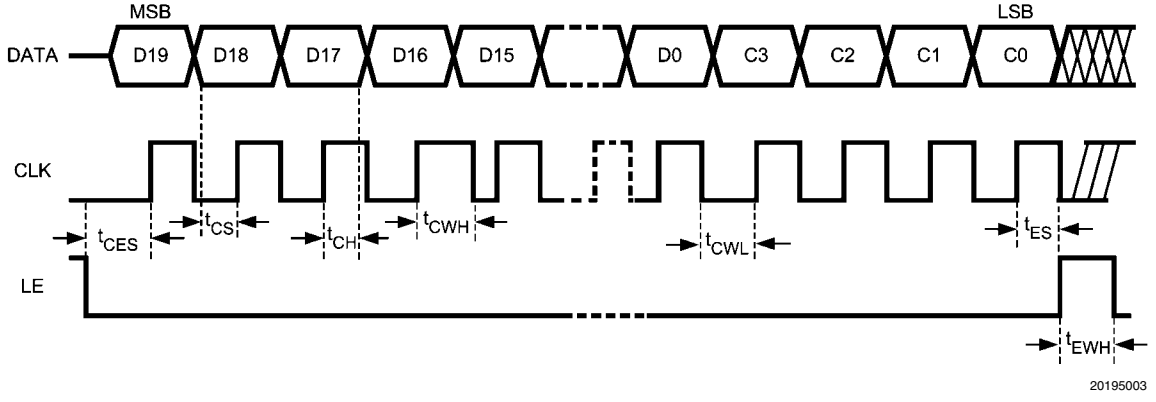
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital Interface (DATA, CLK, LE, CE, Ftest/LD, FLout)						
V_{IH}	High-Level Input Voltage		1.6		2.75	V
V_{IL}	Low-Level Input Voltage				0.4	V
I_{IH}	High-Level Input Current	V_{IH} = 1.75	-3.0		3.0	µA
I_{IL}	Low-Level Input Current	V_{IL} = 0 V	-3.0		3.0	µA
V_{OH}	High-Level Output Voltage	I_{OH} = 500 µA	2.0	2.65		V
V_{OL}	Low-Level Output Voltage	I_{OL} = -500 µA		0.0	0.4	V
MICROWIRE Timing						
t_{CS}	Data to Clock Set Up Time	See Data Input Timing	25			ns
t_{CH}	Data to Clock Hold Time	See Data Input Timing	20			ns
t_{CWH}	Clock Pulse Width High	See Data Input Timing	25			ns
t_{CWL}	Clock Pulse Width Low	See Data Input Timing	25			ns
t_{ES}	Clock to Enable Set Up Time	See Data Input Timing	25			ns
t_{CES}	Enable to Clock Set Up Time	See Data Input Timing	25			ns
t_{EWH}	Enable Pulse Width High	See Data Input Timing	25			ns

Note 2: Normalized Phase Noise Contribution is defined as: LN(f) = L(f) – 20log(N) – 10log(Fcomp) where L(f) is defined as the single side band phase noise measured at an offset frequency, f, in a 1 Hz Bandwidth and Fcomp is the comparison frequency of the synthesizer. The offset frequency, f, must be chosen sufficiently smaller then the loop bandwidth of the PLL, and large enough to avoid a substantial noise contribution from the reference.

Note 3: Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the R0 register was last programmed, and still have the part stay in lock. The action of programming the R0 register, even to the same value, activates a frequency calibration routine. This implies that the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the R0 register to ensure that it stays in lock. Regardless of what temperature the part was initially programmed at, the temperature can never drift outside the frequency range of -40°C $\leq T_A \leq$ 85°C without violating specifications.

Note 4: The VCO phase noise is measured assuming that the loop bandwidth is sufficiently narrow that the VCO noise dominates. The maximum limits apply only at center frequency and over temperature, assuming that the part is reloaded at each test frequency. Over frequency, the phase noise can vary 1-2 dB, with the worst case performance typically occurring at the highest frequency. Over temperature, the phase noise typically varies 1-2 dB, assuming the part is reloaded.

Serial Data Timing Diagram



The DATA is clocked into a shift register on each rising edge of the CLK signal. On the rising edge of the LE signal, the data is sent from the shift registers to an actual counter. A slew rate of at least 30 V/µs is recommended for these signals. After the programming is complete, the CLK, DATA, and LE signals should be returned to a low state. If the CLK and DATA lines are toggled while the in VCO is in lock , as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during the time of this programming.

1.0 Functional Description

The LMX2531LQ1500E is a low power, high performance frequency synthesizer system which includes the PLL, VCO, and partially integrated loop filter. Section 2.0 on programming describes the bits mentioned in this section in more detail.

1.1 REFERENCE OSCILLATOR INPUT

Because the VCO frequency calibration algorithm is based on clocks from the OSCin pin, there are certain bits that need to be set depending on the OSCin frequency. XTLSEL (R6[22:20]) and XTLDIV (R7[9:8]) are both need to be set based on the OSCin frequency.

1.2 R DIVIDER

The R divider divides the OSCin frequency down to the phase detector frequency. The only valid R counter values are 1, 2, 4, 8, 16, and 32. The R divider also has an impact on the fractional modulus that can be used, if it is greater than 8.

1.3 N DIVIDER AND FRACTIONAL CIRCUITRY

The N divider on the LMX2531LQ1500E is fractional and can achieve any fractional denominator between 1 and 4,194,303. The integer portion of the N counter value, $N_{Integer}$, is determined by the value of the N word. Because there is a 16/17/20/21 prescaler, there are restrictions on how small the $N_{Integer}$ value can be. This is because this value is actually formed by several different prescalers in the quadruple modulus prescaler in order to achieve the desired value. The fractional word, $N_{Fractional}$, is a fraction formed with the NUM and DEN words. The fractional denominator value, DEN, can be set from 2 to 4,194,303. The case of DEN=0 makes no sense, since this would cause an infinite N value, and the case of 1 makes no sense (but could be done), because integer mode should be used in these applications. All other values in this range, like 10, 32,734, or 4,000,000 are all valid. Once the fractional denominator, DEN, is determined, the fractional numerator, NUM, is intended to be varied from 0 to DEN-1. Sometimes, expressing the same fraction, like 1/10, in terms of larger fractions, like 100/10000, sometimes yields better fractional spurs, but other times it does not. This can be impacted by the fractional modulator order and the dithering mode selected, as well as the loop bandwidth, and other application specific criteria. So in general, the total N counter value is determined by:

$$N = N_{Integer} + N_{Fractional}$$

In order to calculate the minimum necessary fractional denominator, the R counter value needs to be chosen, so that the comparison frequency is known. The minimum necessary fractional denominator can be calculated by dividing the comparison frequency by the greatest common multiple of the comparison frequency and the OSCin frequency. For example, consider the case of a 10 MHz crystal and a 200 kHz channel spacing. If the R counter value is chosen to be 2, then the comparison frequency will be 5 MHz. The greatest common multiple of 200 kHz and 5 MHz is 200 kHz. If one takes 5 MHz divided by 200 kHz, this is 25. So a fractional denominator of 25, or any multiple of 25 would work in this situation. Now consider a second example where the channel spacing is changed to 30 kHz. If it is again assumed that the comparison frequency is 5 MHz, then the greatest common multiple of 30 kHz and 5 MHz is 10 kHz. 5 MHz divided by 10 kHz is 500. In this situation, a fractional denominator of 500, or any multiple of 500 would suffice. For a final example, consider an application with a fixed output frequency of 2110.8 MHz and a crystal frequency of 19.68 MHz. If the R counter is chosen to be 2, then the comparison frequency is 9.84 MHz. The greatest common multiple of 9.84 MHz and 2110.8 MHz is 240 kHz. 9.84 MHz / 240 kHz = 41. So the fractional denominator could be 41, or any multiple of 41. For this last example value, the entire N counter value would be 214 + 21/41.

The fractional value is achieved with a delta sigma architecture. In this architecture, an integer N counter is modulated between different values in order to achieve a fractional value. On this part, the modulator order can be zero (integer mode), two, three, or four. The higher the fractional modulator order is, the lower the spurs theoretically are. However, this is not always the case, and the higher order fractional modulator can sometimes give rise to additional spurious tones, but this is dependent on the application. This is why it is an advantage to have the modulator order selectable. Dithering also has an impact on the fractional spurs, but a lesser one.

1.4 PHASE DETECTOR

The phase detector compares the outputs of the R and N counters and puts out a correction current corresponding to the phase error. The choice of the phase detector frequency does have an impact on performance. When determining which phase detector frequency to use, the restrictions on the R counter values must be taken into consideration.

1.5 PARTIALLY INTEGRATED LOOP FILTER

The LMX2531LQ1500E integrates the third pole (formed by R3 and C3) and fourth pole (formed by R4 and C4) of the loop filter. This loop filter can be enabled or bypassed using the EN_LPFLTR (R6[15]). The values for C3, C4, R3, and R4 can also be programmed independently through the MICROWIRE interface . Also, the values for R3 and R4 can be changed during FastLock, for minimum lock time. It is recommended that the integrated loop filter be set to the maximum possible attenuation (R3=R4=40kΩ, C3=C4=100pF), the internal loop filter is more effective at reducing certain spurs than the external loop filter. However, if the attenuation of the internal loop filter is too high, it limits the maximum attainable loop bandwidth that can be achieved, which corresponds to the case where the shunt loop filter capacitor, C1, is zero. Increasing the charge pump current and/or the comparison frequency increases the maximum attainable loop bandwidth when designing with the integrated filter. Furthermore, this often allows the loop filter to be better optimized and have stronger attenuation. If the charge pump current and comparison frequency are already as high as they go, and the maximum attainable loop bandwidth is still too low, the resistor and capacitor values can be decreased or the internal loop filter can even be bypassed. Note that when the internal loop filter is bypassed, there is still a small amount of input capacitance on front of the VCO on the order of 200 pF. For design tools and more information on partially integrated loop filters, go to wireless.national.com.

1.6 LOW NOISE, FULLY INTEGRATED VCO

The LMX2531LQ1500E includes a fully integrated VCO, including the inductors. In order for optimum phase noise performance, this VCO has frequency and phase noise calibration algorithms. The frequency calibration algorithm is necessary because the VCO internally divides up the frequency range into several bands, in order to achieve a lower tuning gain, and therefore better phase noise performance. The frequency calibration routine is activated any time that the R0 register is programmed. If the temperature shifts considerably and the R0 register is not programmed, then it can not drift more than the maximum allowable drift for continuous lock, ΔT_{CL}, or else the VCO is not guaranteed to stay in lock.

The phase noise calibration algorithm is necessary in order to achieve the lowest possible phase noise. The VCO_ACI_SEL bit (R6[19:16]) needs to be set to the correct value to ensure the best possible phase noise.

The gain of the VCO can change considerably over frequency. It is lowest at the minimum frequency and highest at the maximum frequency. This range is specified in the datasheet. When designing the loop filter, the following method is recommended. First, take the geometric mean of the minimum and maximum frequencies that are to be used. Then use a linear approximation to extrapolate the VCO gain.

1.7 PROGRAMMABLE DIVIDE BY 2

All options of the LMX2531LQ1500E offer a divide by 2 option. This allows the user to get exactly half of the VCO frequency, by dividing the output of the VCO output by two. Because this divide by two is outside feedback path between the VCO and the PLL, the loop filter and counter values are set up for the VCO frequency before it is divide by two. Note that R0 register should be reprogrammed the first time after the DIV2 bit is enabled or disabled for optimal phase noise performance.

1.8 CHOOSING THE CHARGE PUMP CURRENT AND COMPARISON FREQUENCY

The LMX2531LQ1500E has 16 levels of charge pump currents and a highly flexible fractional modulus. This gives the user many degrees of freedom. This section discusses some of the design considerations. From the perspective of the PLL noise, choosing the charge pump current and comparison frequency as high as possible are best for optimal phase noise performance. The far out PLL noise improves 3 dB for every doubling of the comparison frequency, but at lower offsets, this effect is much less due to the PLL 1/f noise. Increasing the charge pump current improves the phase noise about 3 dB per doubling of the charge pump current, although there are small diminishing returns as the charge pump current goes higher.

From a loop filter design and PLL phase noise perspective, one might think to always design with the highest possible comparison frequency and charge pump current. However, if one considers the worst case fractional spurs that occur at an output frequency equal to 1 channel spacing away from a multiple of the OSCin frequency, then this gives reason to reconsider. If the comparison frequency or charge pump currents are too high, then these spurs could be degraded, and the loop filter may not be able to filter these spurs as well as theoretically predicted. For optimal spur performance, a comparison frequency in the ballpark of 2.5 MHz and a charge pump current of 1X are recommended.

2.0 General Programming Information

The LMX2531LQ1500E is programmed using 11 24-bit registers used to control the LMX2531LQ1500E operation. A 24-bit shift register is used as a temporary register to indirectly program the on-chip registers. The shift register consists of a data field and an address field. The last 4 register bits, CTRL[3:0] form the address field, which is used to decode the internal register address. The remaining 20 bits form the data field DATA[19:0]. While LE is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When LE goes high, data is transferred from the data field into the selected register bank.

Although there are actually 14 registers in this part, only a portion of them should be programmed, since the state of the other hidden registers (R13, R11, and R10) are set during the initialization sequence. Although it is possible to program these hidden registers, as well as a lot of bits that are defined to either '1' or '0', the user should not experiment with these hidden registers and bits, since doing will most likely degrade performance. Furthermore, this would be inconsistent to how these parts are tested.

DATA[19:0]																				CONTROL[3:0]			
MSB																							**LSB**
D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	C3	C2	C1	C0

2.01 Register Location Truth Table

C3	C2	C1	C0	Data Address
1	1	0	0	R12
1	0	0	1	R9
1	0	0	0	R8
0	1	1	1	R7
0	1	1	0	R6
0	1	0	1	R5
0	1	0	0	R4
0	0	1	1	R3
0	0	1	0	R2
0	0	0	1	R1
0	0	0	0	R0

2.02 Initialization Sequence

The initial loading sequence from a cold start is described below. The registers must be program in order shown.

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R5 INIT1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R5 INIT2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R5	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	1
R12	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	0
R9	See individual section for R9 programming information.																				1	0	0	1
R8	See individual section for Register R8 programming information. Register R8 only needs to be programmed for a few options of the LMX2531LQ1500E and and only in the case that the OSCin frequency is greater than 40 MHz.																				1	0	0	0
R7	See individual section for Register R7 programming information.																				0	1	1	1
R6	See individual section for Register R6 programming information.																				0	1	1	0
R4	See individual section for Register R4 programming information. Register R4 only needs to be programmed if FastLock is used.																				0	1	0	0
R3	See individual section for Register R3 programming information.																				0	0	1	1
R2	See individual section for Register R2 programming information.																				0	0	1	0
R1	See individual section for Register R1 programming information.																				0	0	0	1
R0	See individual section for Register R0 programming information.																				0	0	0	0

Note: There must be a minimum of 10 mS between the time when R5 is last loaded and when R1 is loaded to ensure time for the LDOs to power up properly.

2.03 Complete Register Content Map

This table shows all the programmable bits for the LMX2531LQ1500E. No programming order or initialization sequence is implied by this table, only the location of the programming information.

REGISTER	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DATA[19:0]																				C3	C2	C1	C0
R0	N [7:0]								NUM [11:0]												0	0	0	0
R1	0	0	1	ICP [3:0]				N [10:8]			NUM [21:12]										0	0	0	1
R2	0	1	DEN [11:0]												R [5:0]						0	0	1	0
R3	DIV2	FDM	DITHER [1:0]		ORDER [1:0]		FoLD [3:0]				DEN [21:12]										0	0	1	1
R4	0	0	ICPFL [3:0]				TOC [13:0]														0	1	0	0
R5	1	0	0	0	0	REG_RST	0	0	0	0	0	0	0	EN_DIGLDO	EN_PLLLDO2	EN_PLLLDO1	EN_VCOLD	EN_OSC	EN_VCO	EN_PLL	0	1	0	1
R6	0	XTLSEL [2:0]			VCO_ACI_SEL [3:0]				EN_LPFLTR	R4_ADJ [1:0]		R4_ADJ_FL [1:0]		R3_ADJ [1:0]		R3_ADJ_FL [1:0]		C3_4_ADJ [2:0]			0	1	1	0
R7	0	0	XTLMAN [11:0]												XTLDIV [1:0]		0	0	0	0	0	1	1	1
R8	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	XTLMAN2	1	0	0	0
R9	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	0	1	0	0	1
R12	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	0

2.1 REGISTER R0

The action of programming the R0 register activates a frequency calibration routine for the VCO. This calibration is necessary to get the VCO to center the tuning voltage for optimal performance. If the temperature drifts considerably, then the PLL should stay in lock, provided that the temperature drift specification is not violated.

2.1.1 NUM[10:0] and NUM[21:12] -- Fractional Numerator

The NUM word is split between the R0 register and R1 register. The Numerator bits determine the fractional numerator for the delta sigma PLL. This value can go from 0 to 4095 when the FDM bit (R3[22]) is 0 (the other bits in this register are ignored), or 0 to 4194303 when the FDM bit is 1.

	NUM[21:12]										**NUM[11:0]**											
Fractional Numerator																						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...																						
409503	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
...																						
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note that there are restrictions on the fractional numerator value depending on the R counter value if it is 16 or 32.

2.1.2 N[7:0] and N[10:8]

The N counter is 11 bits. 8 of these bits are located in the R0 register, and the remaining 3 (MSB bits) are located in the R1 register. The LMX2531LQ1500E consists of an A, B, and C counter, which work in conjunction with the 16/17/20/21 prescaler in order to form the final N counter value.

	N[10:8]			**N[7:0]**							
N Value	C							B		A	
<55	Values less than 55 are prohibited.										
55	0	0	0	0	0	1	1	0	1	1	1
...											
2039	1	1	1	1	1	1	1	0	1	1	1

2.2 REGISTER R1

2.2.1 NUM[21:12]

These are the MSB bits in for the fractional numerator that already have been described.

2.2.2 N[10:8] -- 3 MSB Bits for the N Counter

These are the 2 MSB bits for the N counter, which were discussed in the R0 register section.

2.2.3 ICP[3:0] -- Charge Pump Current

This bit programs the charge pump current when the charge pump gain. The current is programmable between 100uA and 1.6mA in 100uA steps. In general, higher charge pump currents yield better phase noise for the PLL, but also can cause higher spurs.

ICP	Charge Pump State	Typical Charge Pump Current at 3 Volts (µA)
0	1X	90
1	2X	180
2	3X	270
3	4X	360
4	5X	450
5	6X	540
6	7X	630
7	8X	720
8	9X	810
9	10X	900
10	11X	990
11	12X	1080
12	13X	1170
13	14X	1260
14	15X	1350
15	16X	1440

2.3 REGISTER R2

2.3.1 R[5:0] -- R Counter Value

These bits determine the phase detector frequency. The OSCin frequency is divided by this R counter value. Note that only the values of 1, 2, 4, 8, 16, and 32 are allowed.

R Value	Fractional Denominator Restrictions	R[5:0]					
0,3,5-7, 9-15,17-31, 33-63	n/a	These values are illegal.					
1	none	0	0	0	0	0	1
2	none	0	0	0	0	1	0
4	none	0	0	0	1	0	0
8	none	0	0	1	0	0	0
16	Must be divisible by 2	0	1	0	0	0	0
32	Must be divisible by 4	1	0	0	0	0	0

Note that the R counter value can put some restrictions on the fractional denominator. In the case that it is 16, the fractional denominator must be divisible by 2, which is equivalent to saying that the LSB of the fractional denominator word is zero. In the case that the R counter is 32, the two LSB bits of the fractional denominator word must also be zero, which is equivalent to saying that the fractional denominator must be divisible by 4. Because the fractional denominator can be very large, this should cause no issues. For instance, if one wanted to achieve a fractional word of 1/65, and the R counter value was 16, the fractional word could be changed t0 4/260 ,and the same resolution could be achieved.

2.3.2 DEN[21:12] and DEN[11:0]-- Fractional Denominator

These bits determine the fractional denominator. Note that the MSB bits for this word are in register R3. If the FDM bit is set to 0, DEN[21:12] are ignored. The fractional denominator should only be set to zero if the fractional circuitry is being disabled by setting ORDER=1. A value of one never makes sense to use. All other values could reasonably be used in fractional mode.

	DEN[21:12]										DEN[11:0]											
Fractional Denominator																						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
...																						
4095	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4096	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
...																						
4194303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

2.4 REGISTER R3

2.4.1 DEN[21:12] -- Extension for the Fractional Denominator

These are the MSB bits of the DEN word, which have already been discussed.

2.4.2 FoLD[3:0] -- Multiplexed Output for Ftest/LD Pin

The FoLD[3:0] word is used to program the output of the Ftest/LD Pin. This pin can be used for a general purpose I/O pin, a lock detect pin, and for diagnostic purposes. When programmed to the digital lock detect state, the output of the Ftest/LD pin will be high when the part is in lock, and low otherwise. Lock is determined by comparing the input phases to the phase detector. The analog lock detect modes put out a high signal with very fast negative pulses, that correspond to when the charge pump comes on. This output can be low pass filtered with an RC filter in order to determine the lock detect state. If the open drain state is used, a pull-up resistor that is much larger than the resistance in the RC filter, to increase the sensitivity of the circuit. For diagnostic purposes, the options that allow one to view the output of the R counter or the N counter can be very useful. Be aware that the output voltage level of the Ftest/LD is not equal to the supply voltage of the part, but rather is given by V_{OH} and V_{OL} in the electrical characteristics specification.

FoLD	Output Type	Function
0	High Impedance	Disabled
1	Push-Pull	Logical High State
2	Push-Pull	Logical Low State
3	Push-Pull	Digital Lock Detect
4	N/A	Reserved
5	Push-Pull	N Counter Output Divided by 2
6	Open-Drain	Analog Lock Detect
7	Push-Pull	Analog Lock Detect
8	N/A	Reserved
9	N/A	Reserved
10	N/A	Reserved
11	N/A	Reserved
12	N/A	Reserved
13	N/A	Reserved
14	Push-Pull	R Counter Output
15	N/A	Reserved

2.4.3 ORDER -- Order of Delta Sigma Modulator

This bit determines the order of the delta sigma modulator in the PLL. In general, higher order fractional modulators tend to reduce the primary fractional spurs that occur at increments of the channel spacing, but can also create spurs that are at a fraction of the channel spacing, if there is not sufficient filtering. The optimal choice of modulator order is very application specific, however, a third order modulator is a good starting point if not sure what to try first.

ORDER	Delta Sigma Modulator Order
0	Fourth
1	Reset Modulator (Integer Mode - all fractions are ignored)
2	Second
3	Third

2.4.4 DITHER -- Dithering

Dithering is useful in reducing fractional spurs, especially those that occur a a fraction of the channel spacing. The only exception is when the fractional numerator is zero. In this case, dithering usually is not a benefit. Dithering also can sometimes increase the PLL phase noise by a fraction of a dB. In general, if dithering is disabled, phase noise may be slightly better inside the loop bandwidth of the system, but spurs are likely to be worse too.

DITHER	Dithering Mode
0	Weak Dithering
1	Reserved
2	Strong Dithering
3	Dithering Disabled

2.4.5 FDM -- Fractional Denominator Mode

When this bit is set to 1, the 10 MSB bits for the fractional numerator and denominator are considered. This allows the fractional denominator to range from 1 to 4,194,303. If this bit is set to zero, only the 12 LSB bits of the fractional numerator and denominator are considered, and this allows a fractional denominator from 1 to 4095. When this bit is disabled, the current consumption is about 0.5 mA lower.

2.4.6 -- DIV2

When this bit is enabled on the appropriate option, the output of the VCO is divided by 2 on options that offer this feature. This has a small impact on harmonic content and output power.

DIV2	VCO Output Frequency
0	Not Divided by 2
1	Divided by 2

2.5 REGISTER R4

2.5.1 TOC[13:0] -- Time Out Counter for FastLock

When the value of this word is 3 or less, then FastLock is disabled, and this pin can only be used for general purpose I/O. When this value is 4 or greater, the time out counter is engaged for the amount of phase detector cycles shown in the table below.

TOC Value	FLout Pin State	Timeout Count
0	High Impedance	0
1	Low	Always Enabled
2	Low	0
3	High	0
4	Low	4 X 2 Phase Detector
.	.	.
16383	Low	16383 X 2 Phase Detector

When this count is active, the FLout Pin is grounded, the FastLock current is engaged, and the resistors R3 and R4 are also potentially changed. The table below summarizes the bits that control various values in and out of FastLock differences.

FastLock State	FLout	Charge Pump Current	R3	R4
Steady State	High Impedance	ICP	R3_ADJ	R4_ADJ
Fastlock	Grounded	ICPFL	R3_ADJ_FL	R4_ADJ_FL

2.5.2 ICPFL[3:0] -- Charge Pump Current for Fastlock

When FastLock is enabled, this is the charge pump current that is used for faster lock time.

ICPFL	Fastlock Charge Pump State	Typical Fastlock Charge Pump Current at 3 Volts (µA)
0	1X	90
1	2X	180
2	3X	270
3	4X	360
4	5X	450
5	6X	540
6	7X	630
7	8X	720
8	9X	810
9	10X	900
10	11X	990
11	12X	1080
12	13X	1170
13	14X	1260
14	15X	1350
15	16X	1440

2.6 REGISTER R5

2.6.1 EN_PLL -- Enable Bit for PLL

When this bit is set to 1, the PLL is powered up, otherwise, it is powered down.

2.6.2 EN_VCO -- Enable Bit for the VCO

When this bit is set to 1, the VCO is powered up, otherwise, it is powered down.

2.6.3 EN_OSC -- Enable Bit for the Oscillator Inverter

When this bit is set to 1 (default), the reference oscillator is powered up, otherwise it is powered down.

2.6.4 EN_VCOLDO -- ENABLE BIT FOR THE VCO LDO

When this bit is set to 1 (default), the VCO LDO is powered up, otherwise it is powered down.

2.6.5 EN_PLLLDO1 -- ENABLE BIT FOR THE PLL LDO 1

When this bit is set to 1 (default), the PLL LDO 1 is powered up, otherwise it is powered down.

2.6.6 EN_PLLLDO2 -- ENABLE BIT FOR THE PLL LDO 2

When this bit is set to 1 (default), the PLL LDO 2 is powered up, otherwise it is powered down.

2.6.7 EN_DIGLDO -- ENABLE BIT FOR THE DIGITAL LDO

When this bit is set to 1 (default), the Digital LDO is powered up, otherwise it is powered down.

2.6.8 REG_RST -- RESETS ALL REGISTERS TO DEFAULT SETTINGS

This bit needs to be programmed three times to initialize the part. When this bit is set to one, all registers are set to default mode, and the part is powered down. The second time the R5 register is programmed with REG_RST=0, the register reset is released and the default states are still in the registers. However, since the default states for the blocks and LDOs is powered off, it is therefore necessary to program R5 a third time so that all the LDOs and blocks can be programmed to a power up state. When this bit is set to 1, all registers are set to the default modes, but part is powered down. For normal operation, this bit is set to 0. Note that once this initialization is done, it is not necessary to initialize the part any more.

2.7 REGISTER R6

2.7.1 C3_C4_ADJ[2:0] -- VALUE FOR C3 AND C4 IN THE INTERNAL LOOP FILTER

C3_C4_ADJ	C3 (pF)	C4 (pF)
0	50	50
1	50	100
2	50	150
3	100	50
4	150	50
5	100	100
6	50	150
7	50	150

2.7.2 R3_ADJ_FL[1:0] -- Value for Internal Loop Filter Resistor R3 During Fastlock

R3_ADJ_FL Value	R3 Resistor During Fastlock (kΩ)
0	10
1	20
2	30
3	40

2.7.3 R3_ADJ[1:0] -- Value for Internal Loop Filter Resistor R3

R3_ADJ	R3 Value (kΩ)
0	10
1	20
2	30
3	40

2.7.4 R4_ADJ_FL[1:0] -- Value for Internal Loop Filter Resistor R4 During Fastlock

R4_ADJ_FL	R4 Value during Fast Lock (kΩ)
0	10
1	20
2	30
3	40

2.7.5 R4_ADJ[1:0] -- Value for Internal Loop Filter Resistor R4

R4_ADJ	R4 Value (kΩ)
0	10
1	20
2	30
3	40

2.7.6 EN_LPFLTR-- Enable for Partially Integrated Internal Loop Filter

The Enable Loop Filter bit is used to enable/disable the 3rd and 4th pole on-chip loop filters.

EN_LPFLTR	3rd and 4th Poles of Loop Filter
0	disabled (R3 = R4 = 0 ohms and C3 + C4 = 200pF)
1	enabled

2.7.7 VCO_ACI_SEL

This bit is used to optimize the VCO phase noise. The recommended values are what are used for all testing purposes, and this bit should be set as the table below instructs.

Part	VCO_ACI_SEL
LMX2531LQ1500E	8

2.7.8 XTLSEL[2:0] -- Crystal Select

XTLSEL	Crystal Frequency
0	<25 MHz
1	25 - 50 MHz
2	50 - 70 MHz
3	>70 MHz
4	Manual Mode
5	Reserved
6	Reserved
7	Reserved

The value of this word needs to be changed based on the frequency presented to the OSCin pin in accordance to the table above.

2.8 REGISTER R7

2.8.1 XTLDIV[1:0] -- Division Ratio for the Crystal Frequency

The frequency provided to the VCO frequency calibration circuitry is based on the OSCin frequency divided down by a factor, determined by the XTLDIV word. Note that this division ratio is independent of the R counter value or the comparison frequency. The necessary division ratio depends on the OSCin frequency and is shown in the table below:

XTLDIV	Crystal Division Ratio	Crystal Range
0	Reserved	Reserved
1	Divide by 2	< 20 MHz
2	Divide by 4	20-40 MHz
3	Divide by 8	> 40 MHz

2.8.2 XTLMAN[11:0] -- Manual Crystal Mode

Program all these bits to zero.

2.9 REGISTER R8

2.9.1 XTLMAN2 -- MANUAL CRYSTAL MODE SECOND ADJUSTMENT

Set all these bits to zero.

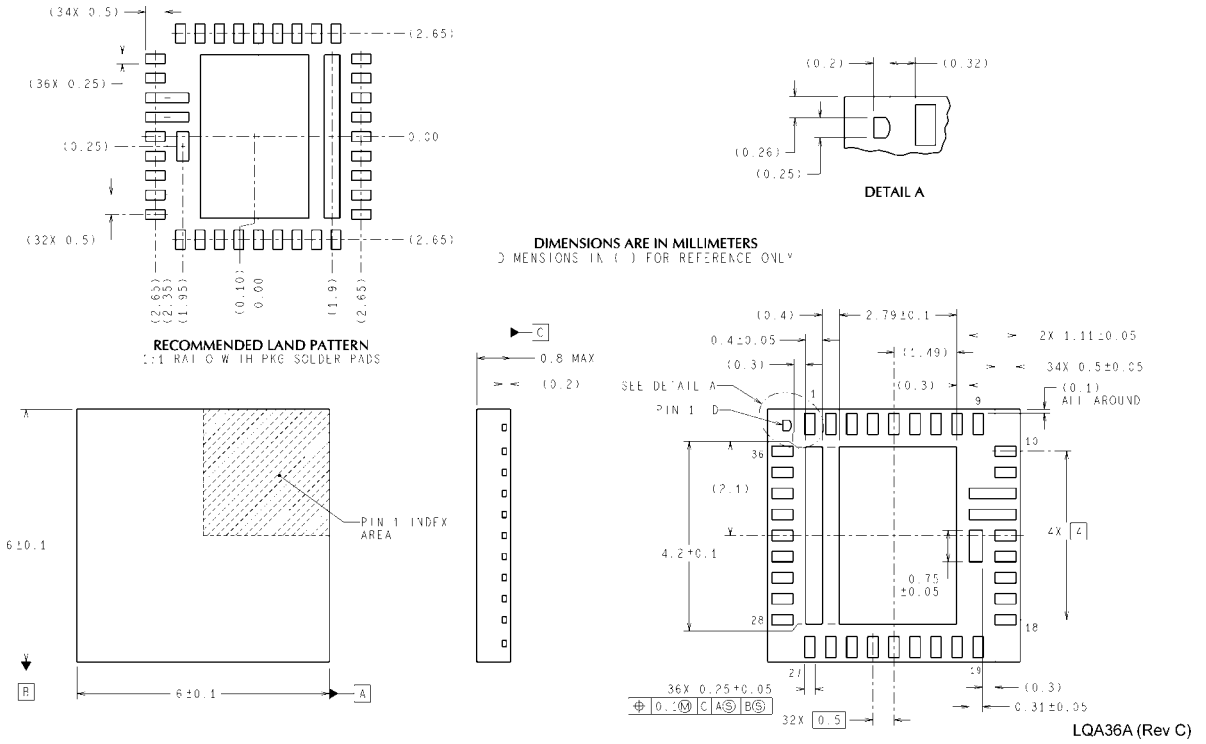
2.10 REGISTER R9

All the bits in this register should be programmed as shown in the programming table.

2.11 REGISTER R12

Even though this register does not have user selectable bits, it still needs to be programmed. This register should be loaded as shown in section 2.02 Complete Register Content Map.

Physical Dimensions inches (millimeters) unless otherwise noted



LQA36A (Rev C)

Leadless Leadframe Package (Bottom View)
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Notes

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