LM5034 Evaluation Board

National Semiconductor
Application Note 1370
Dennis Morgan
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Introduction

The LM5034EVAL evaluation board provides the power supply design engineer with a fully functional 200W dual interleaved DC-DC power switching regulator using forward/active clamp topology. A single LM5034 dual current mode PWM controller is employed to control the two converter channels. Jumpers on the board permit configuring the board as two independent regulators (3.3V and 2.5V outputs), or as a single high current regulator providing 3.3V. The two controller channels operate 180˚ out of phase thereby reducing input ripple current. Power dissipation in the primary side switches is minimized through the use of high speed, high current compound gate drivers in the LM5034 capable of sourcing 1.5A and sinking 2.5A. Power dissipation associated with the transformer reset is minimized through the use of active clamps. Synchronous rectifiers reduce rectification losses in the secondaries.

Features of the LM5034 which can be investigated on this board include:

- Switching frequency can be changed with a single resistor (R8)
- Switching frequency can be synchronized to an external source
- Dead time between main switches and active clamp switches can be adjusted (R7)
- Maximum allowed duty cycle limit can be changed with a single resistor (R3)
- Hiccup mode timing during extended overload conditions can be adjusted (C8)
- Under-voltage lockout threshold can be adjusted (R4, R5)
- Soft-start timing can be changed separately on each channel (C10, C11)

Other features of the LM5034 include an integrated high voltage start-up regulator, cycle-by-cycle current limit, maximum duty cycle fold back at high input voltage, integrated slope compensation, direct interface with opto-coupler transistor, and thermal shutdown.

The evaluation board's specifications are as follows:

- Input voltage: 36V to 78V
- Output voltages: 3.3V, ±2.5% and 2.5V, ±1.5%, or a single 3.3V, ±2.5% high current output
- Output current: 30A from each separate output, or 60A when configured for a single output
- Measured efficiency: 94% (Vin = 48V, Iout = 20A, single 3.3V output)
- Switching frequency: 200 kHz
- Current limit: ≈31.5A at each output
- Input voltage UVLO: ≈34.3V increasing, and ≈32.3V decreasing
- On/Off (shutdown) input
- Synchronizing input
- Size: 3.4 x 2.4 x 0.48 in.

Schematic

Referring to the schematic in *Figure 14* , the circuit is comprised of the LM5034 dual controller, and two almost identical forward converter channels. Channel 2 is along the top half of the schematic providing the 3.3V output. Current sensing transformer T1 provides primary side current information to the LM5034's CS2 pin for current mode PWM control, and for over-current detection. Q1 is the main switch for the power transformer (T3), and Q2 is the active clamp switch. Q5-Q8 are the self-driven synchronous rectifiers for the secondary. The output filter is made up of L2 and C28-C32. In addition, L2 has an auxiliary winding to power the LM5034's VCC pin when this channel is enabled. Error amplifier U3, along with reference U5, provide the voltage feedback signal to the LM5034's COMP2 pin via the opto-coupler.

Schematic (Continued)

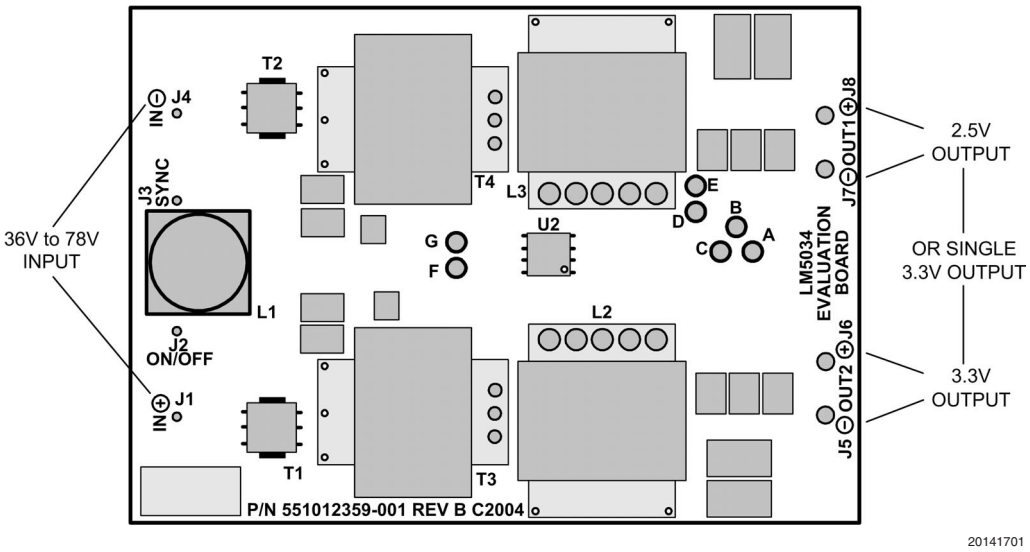


FIGURE 1. Evaluation Board - Top Side

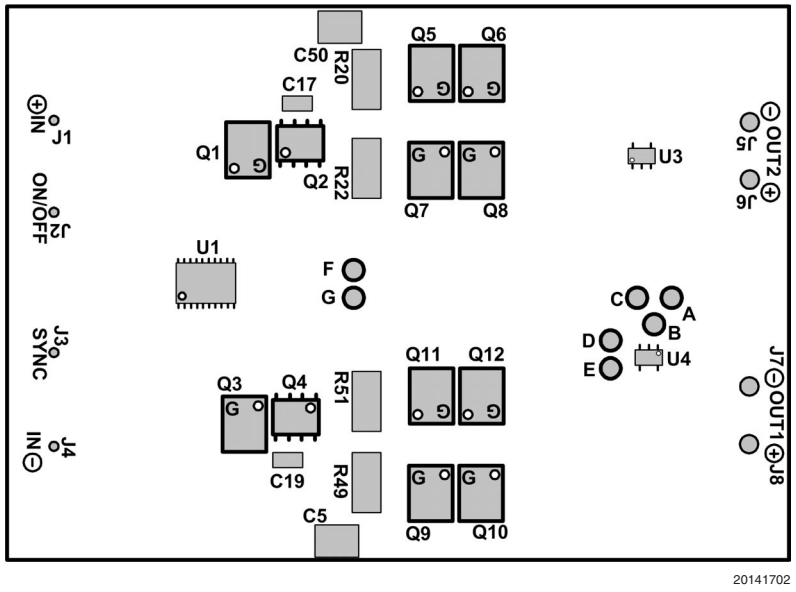


FIGURE 2. Evaluation Board - Bottom Side

Layout and Probing

The pictorials in *Figure 1* and *Figure 2* show the placement of the significant components which may be probed in evaluating the circuit's operation. The following should be kept in mind when the board is powered:

1. The board has two circuit grounds - one associated with the input power, and one associated with the output power. The ground plane on the primary side is shared by the two channels, as is the ground plane on the secondary side. The primary and secondary grounds are DC isolated, but are AC coupled by high voltage capacitors C5 and C50.
2. The power train components (L1, T3, T4, L2, L3, and Q1 - Q12) may get hot to the touch at high load currents. USE CAUTION. When operating either channel at a load current in excess of 15A, the use of a fan to provide forced air flow IS NECESSARY.
3. Use care when probing the primary side at maximum input voltage. 78V is enough to produce a shock or sparks, and cause component damage through accidental contact.
4. At maximum load current the size and length of the wires used to connect the load become important. Ensure there is not a significant drop in the wires. A minimum of 12 gauge wire is recommended for 30A. When configured for a single high current output, it is recommended that equal length 12 gauge wires be used from each output pin to the load. See *Figure 3*.
5. The input wires will carry up to 6A (average) at maximum load current. Ensure these wires are adequately sized.

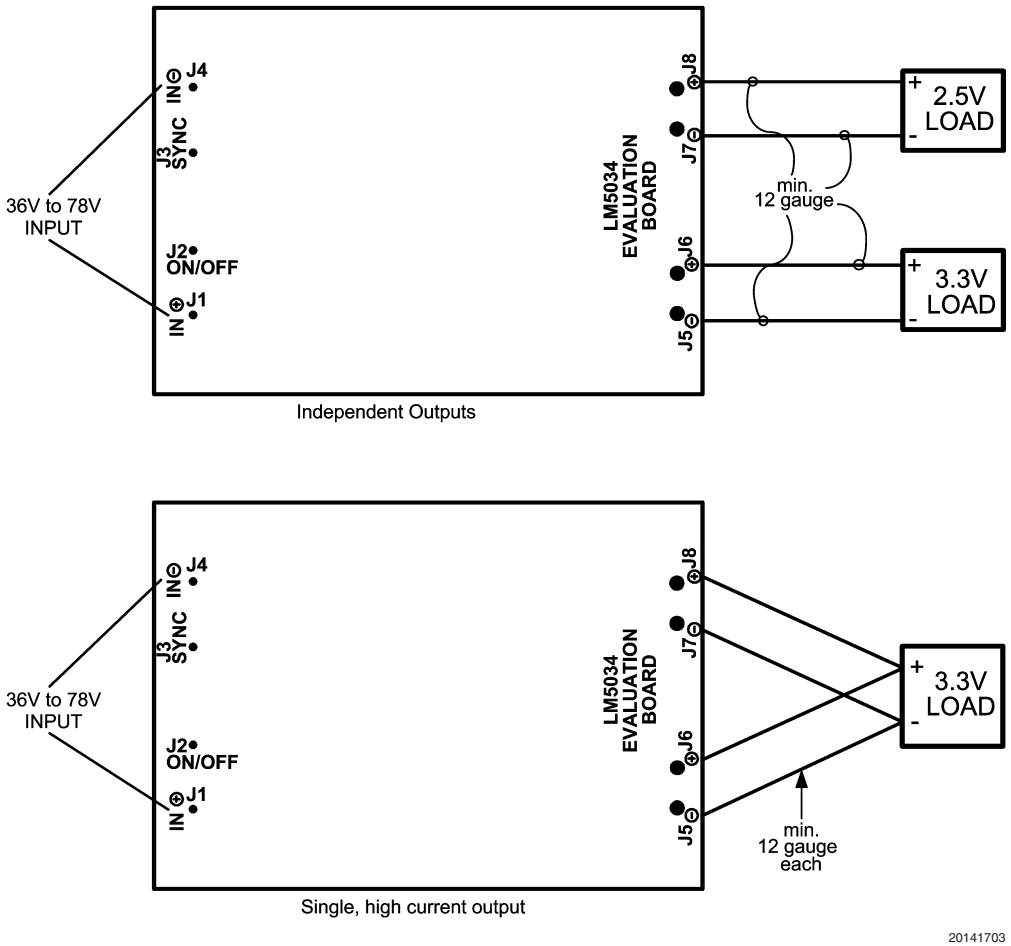


FIGURE 3. Connecting the Load(s)

Output Configuration

Prior to applying power, the jumpers must be set for the desired output configuration. The board is initially shipped with jumper A-B in place, which configures the board for independent outputs - i.e., 2.5V at OUT1 and 3.3V at OUT2. To configure the board for a single 3.3V high current output, it is necessary to remove jumper A-B, and install jumpers in locations B-C, D-E, and F-G. Output pins J6 and J8 must be connected together at the load, as well as output pins J5 and J7, as shown in *Figure 3*. See *Figure 1* for the jumper locations.

Connections/Start-Up

When operating at load currents in excess of 15A from either channel, forced air flow is **NECESSARY**. The input connections are made to terminals J1 (+) and J4 (-). The power source must be capable of supplying the input current as shown in *Figure 8* or *Figure 9*. Upon turn-on, the input current increases with little or no overshoot, due to the LM5034's soft-start function.

When configured for separate outputs, the 3.3V load is connected to J6 (+) and J5 (-) and the 2.5V load is connected to J8 (+) and J7 (-). When configured for a single 3.3V high current output, output pins J6 and J8 (+) are connected together at the load, as are J5 and J7 (-). See *Figure 3*. A minimum of 12 gauge wire should be used for the 30A load currents.

Before start-up a voltmeter should be connected to the input terminals, and to each output. The input current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually until the under-voltage lockout threshold (≈34.3V) is reached, at which time the outputs become active. At this point the meters should be checked immediately to ensure they indicate nominal values.

Performance

When configured for separate outputs, the output impedance is <5 mΩ at each output. When configured as a single high current output, the output impedance is <2.5 mΩ. Line regulation is <0.01% (4 mV) over the input range of 36V to 78V at all load currents. The power conversion efficiency, which peaks at 94% is shown in *Figure 10*- 12.

Waveforms

Figure 7 shows some of the significant waveforms for various input/output combinations. REMEMBER when viewing waveforms there are two circuit grounds, and scope probe grounds must be connected appropriately.

1. The primary side switch for the 3.3V channel (Q1) is on during time t1. The duty cycle (t1/5µs) is determined by the input and output voltages and the transformer's 12:2 turns ratio. The active clamp switch (Q2) is off during t1, and on during Q1's off-time.
2. Current level I2 is the average input current to the board, and I1 is the ripple value of that input current.
3. CS2 is the current information provided by T1, and its associated components, to the CS2 pin. Its amplitude V3 is determined by the primary side current, a reflection of the load current. When viewing the signal at CS2 (or CS1) the scope probe and its ground must be directly across C20 (or C21).
4. The voltages at T3's secondary are shown as V5 and V6. At L2's input, V5's average value is 3.3V, the output voltage.
5. The primary side switch for the 2.5V channel (Q3) is on during time t2. Q3's duty cycle is less than Q1's duty cycle since the output voltage is lower. The start of Q3's on-time occurs 2.5 µs after the start of Q1's on-time since the two signals are 180° out of phase.

Primary Side Operation

In the 3.3V channel, primary side switch (Q1) is driven by the LM5034's OUT2 pin with a duty cycle determined by the input and output voltages and the transformer's 12:2 turns ratio. Duty cycle control is provided by the voltage feedback at COMP2 and the current information at CS2. The active clamp switch (Q2) is off during Q1's on-time, and vice-versa, controlled by the AC2 pin. The overlap time between OUT2 and AC2, which ensures a deadtime between Q1's on-time and Q2's on-time, is set to 45 ns by R7 at Pin 1.

The voltage feedback at COMP2 from the opto-coupler U2 is discussed in more detail in the Feedback Circuit section. The current information at CS2 is provided by the current sense transformer T1, which has a 100:1 turns ratio. The current in T1's primary generates a voltage signal across R15 which is filtered by R16 and C20.

The 2.5V channel operates in the same manner with components Q3, Q4, T2, R18, R19, C21, and pins OUT1, AC1, COMP1, and CS1.

Input filtering is provided by L1 and C1-C4. R1 provides damping for any oscillation tendencies in this filter. R2 and C6 filter transients from the input voltage provided to the LM5034's VIN pin. The input UVLO levels are set by R4 and R5. The internal oscillator frequency is set to ≈400 kHz by R8.

Secondary Side Operation

In the 3.3V channel, during Q1's on-time, T3's pin 4 is positive with respect to pin 3. Q5 and Q6 are on, taking pin 3 to ground, forcing Q7 and Q8 to be off. Current flow is out of T3's pin 4 through L2, through the load to ground, and back through Q5 and Q6 to T3's pin 3. During Q1's off-time, T3's pin 3 is positive with respect to pin 4, turning on Q7 and Q8 which takes pin 4 to ground. Q5 and Q6 are off, blocking current flow in T3's secondary winding. The current in L2 is uninterrupted as it flows through the load to ground, and through Q7 and Q8 back to L2.

Feedback Circuit

The voltage feedback circuit for the single 3.3V channel is shown in *Figure 4*. The 4.096V, ±0.5% reference voltage

Feedback Circuit (Continued)

provided by U5 is divided down to 2.5V by R28 and R29, and provided to error amplifier U3. The 3.3V output voltage is divided down (R31, R34) to 2.5V and provided to U3's inverting input. The error amplifier's output controls the opto-coupler's LED current to control the voltage at the LM5034's COMP2 input. A ramping signal representative of the primary side current is generated by T1, D1, and R15, and provided to the CS2 pin through the R16/C20 filter. Internally, the signals at CS2 and COMP2 are combined at the PWM comparator to generate the appropriate duty cycle at OUT2, and to the power transformer (T3).

Power for U3, U5 and the opto-coupler's LED is provided from T3's secondary through D9. Frequency compensation is provided by the components across U3, R32/C33, C51, R10/C14 and the output filter. The bode plot is shown in *Figure 13*.

When configured for separate outputs (jumper A-B installed), the 2.5V channel's feedback circuit is effectively the same as described above, and it operates independent of the 3.3V channel. When configured for a single high current output, jumpers B-C, D-E, and F-G are installed and A-B is removed, as shown in *Figure 5*. Output terminals J8 and J6 are connected together at the load, as well as the ground terminals J5 and J7. In this mode U4 is a follower to error amplifier U3, and the opto-coupler outputs are connected together to provide the same voltage to COMP1 and COMP2.

Since bandwidth optimization is application dependent, this circuit was not optimized for speed.

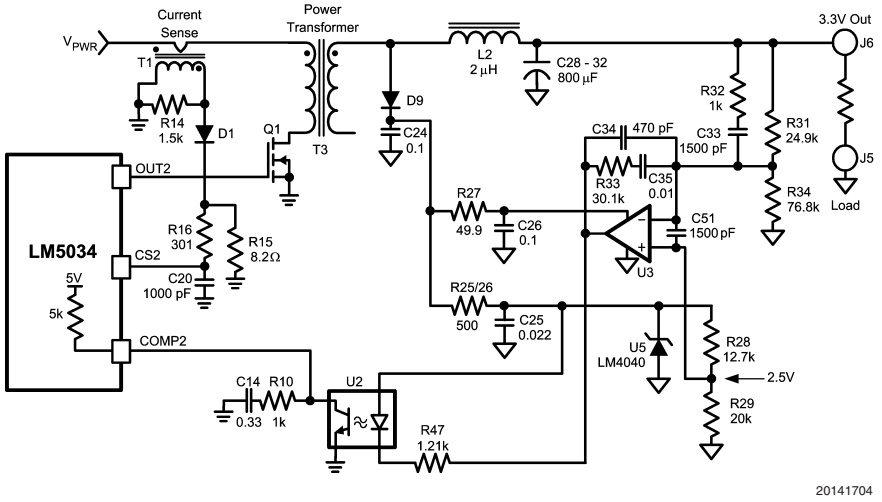


FIGURE 4. Single Channel Feedback Circuit

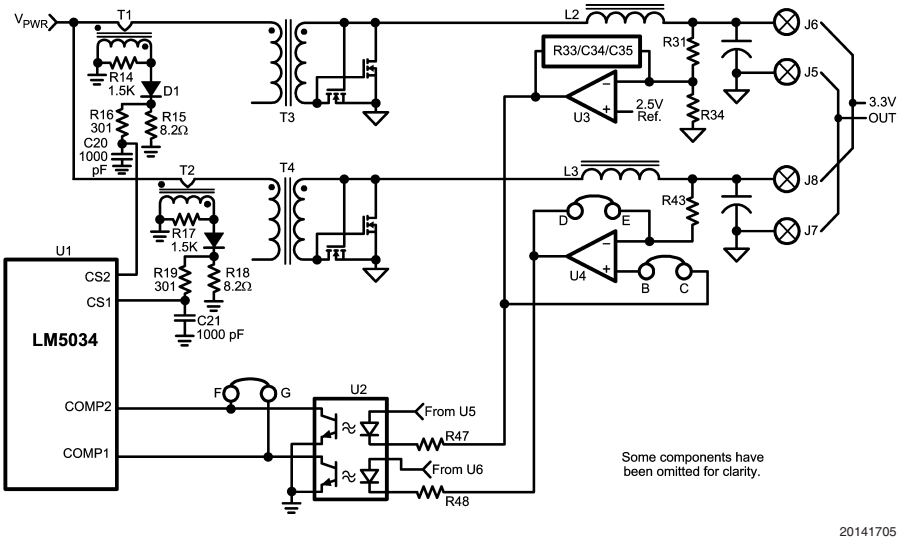


FIGURE 5. Feedback Configuration for Single High Current Output

Current Limit Operation

If the load current exceeds the current limit value, that is sensed at the appropriate CS pin, and the main driver output pulse (at OUT1 or OUT2) is terminated immediately. If the high current fault persists, the controller operates with constant peak switch current in a cycle-by-cycle current limit mode.

When the LM5034 detects repeated current limit events, the voltage at the RES pin increases as shown in *Figure 6*. When the voltage on this pin reaches 2.55V, the Current Limit Restart circuit activates to disable both regulators by taking the soft-start pins to ground. After a short propagation delay, the soft-start pins are charged up by internal 1 µA current sources (t2 in *Figure 6*). When the soft-start pins allow the COMP pins to reach ≈1.5V the output drivers are enabled, and the soft-start current sources increase to 50 µA (t3 in *Figure 6*). If the current fault has been cleared, the output duty cycles increases to the values required for regulation, and the soft-start pins saturate at 5V. If the current fault is still present, the above cycle repeats. The time t2 provides a periodic dwell time for the converters in the event of a sustained overload or short circuit. This results in lower average input current and lower power dissipated within the circuit components.

On this evaluation board, the time t1 in *Figure 6*is ≈13 ms if the current fault exists in both channels, and is ≈51 ms if the current fault exists in one channel only. Time t1 is set by capacitor C8 at pin 15. Time t2 is ≈15 ms, and time t3 is ≈700 µs. Times t2 and t3 are set by the smaller of capacitors C10 and C11, at pins 5 and 16. Although they are listed as the same value, normal tolerances make them slightly different.

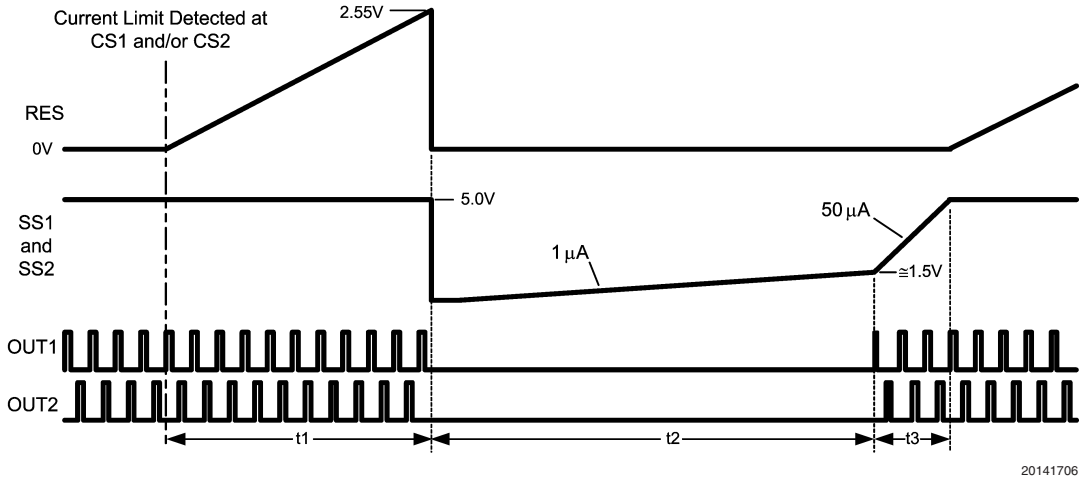


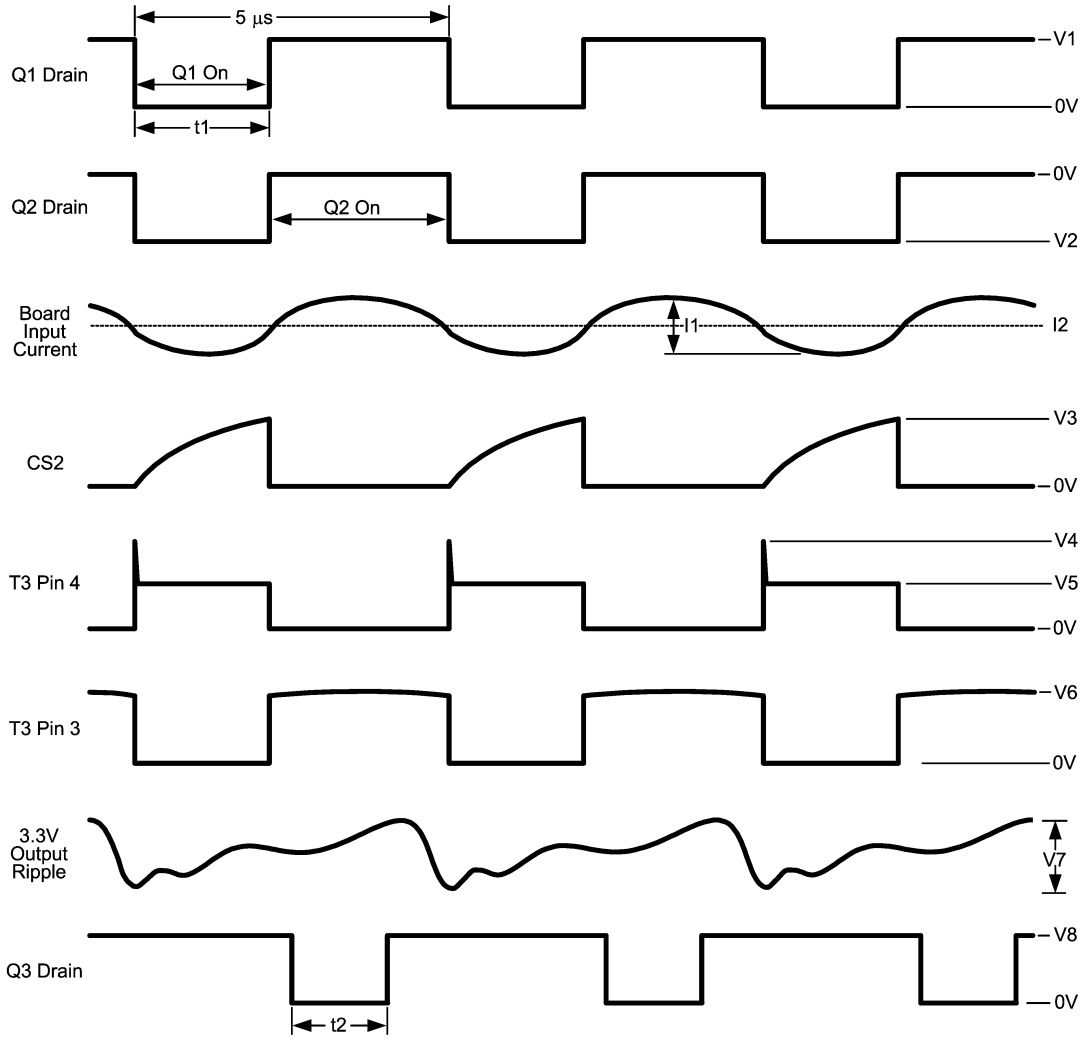
FIGURE 6. Current Limit Restart Operation

On/Off Input

Forcing the On/Off input (J2) below 1.25V shuts down the LM5034, and both switching regulators. In this mode the outputs are disabled, along with the VCC regulator, and the entire circuit consumes ≈1 mA. Upon releasing the On/Off input pin both regulators power up through a normal soft-start sequence.

Synchronizing Input

The LM5034 can be synchronized to an external frequency by applying that frequency to the SYNC input pin (J3). The synchronizing frequency must be at least 4% higher than the oscillator's free running frequency set with the RT resistor (400 kHz, R8 at pin 20), but less than twice the free running frequency. The externally applied pulses must be between 15 and 150 ns wide, with an amplitude between 1.8V and 3.0V with respect to the input ground (J4). R8 must be left in place in this mode.



Vin, Io	t1	V1	V2	V3	V4	V5	V6	V7	t2	V8	I1	I2
36V, 5A	2.8 µs	83V	-82V	95 mV	14V	5.8V	7.7V	39 mVp-p	2.1 µs	62V	30 mAp-p	530 mA
48V, 5A	2.1 µs	83V	-83.4V	95 mV	16.8V	7.8V	5.8V	47 mVp-p	1.56 µs	71V	32 mAp-p	410 mA
48V, 25A	2.23 µs	87V	-85.1V	360 mV	9.8V	7.7V	6.4V	41 mVp-p	1.56 µs	71V	160 mAp-p	1890 mA
78V, 5A	1.29 µs	105V	-105V	95 mV	21.8V	12.8V	4.6V	50 mVp-p	0.96 µs	96V	36 mAp-p	290 mA

Notes: 3.3V output loaded as indicated, 2.5V output unloaded.
All waveforms are in the 3.3V channel except Q3 Drain and Board Input Current.

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FIGURE 7. Representative Waveforms

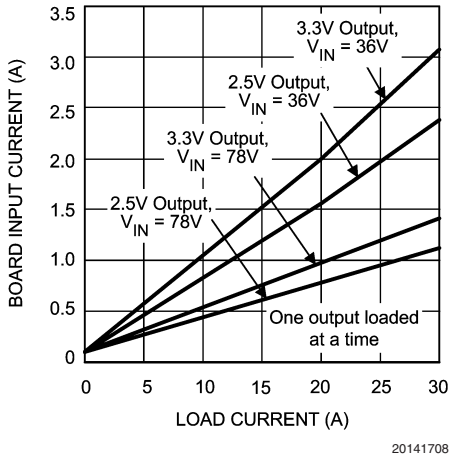


FIGURE 8. Input Current for Separate Output Configuration

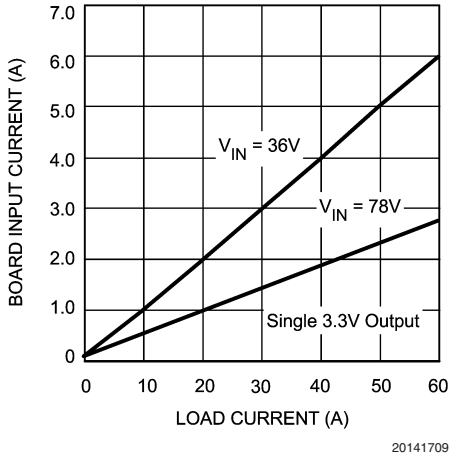


FIGURE 9. Input Current for Single Output Configuration

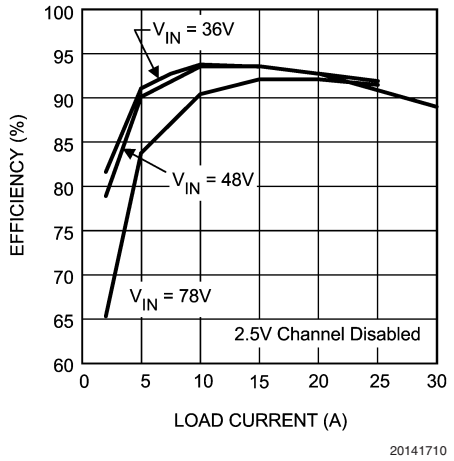


FIGURE 10. 3.3V Channel Efficiency (Separate Output Configuration)

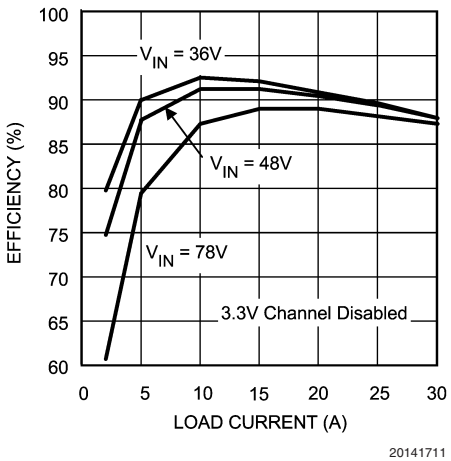


FIGURE 11. 2.5V Channel Efficiency (Separate Output Configuration)

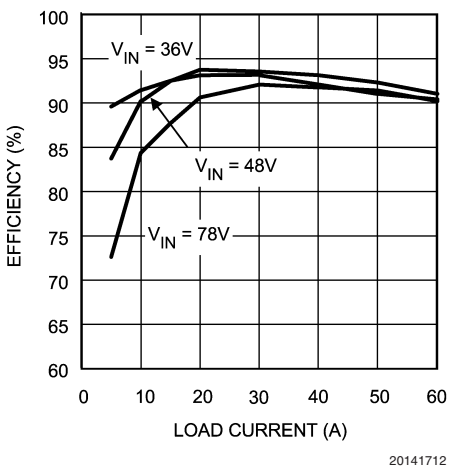


FIGURE 12. 3.3V Efficiency (Single Output Configuration)

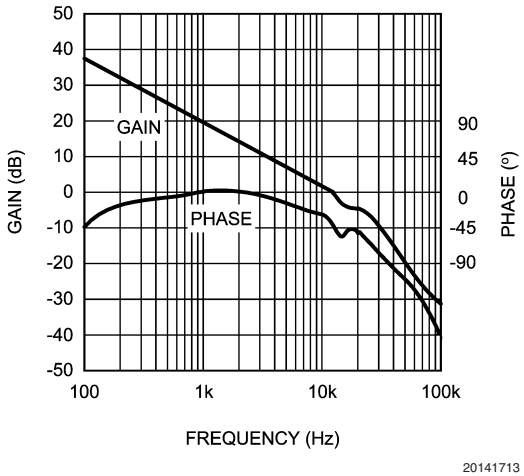


FIGURE 13. Bode Plot

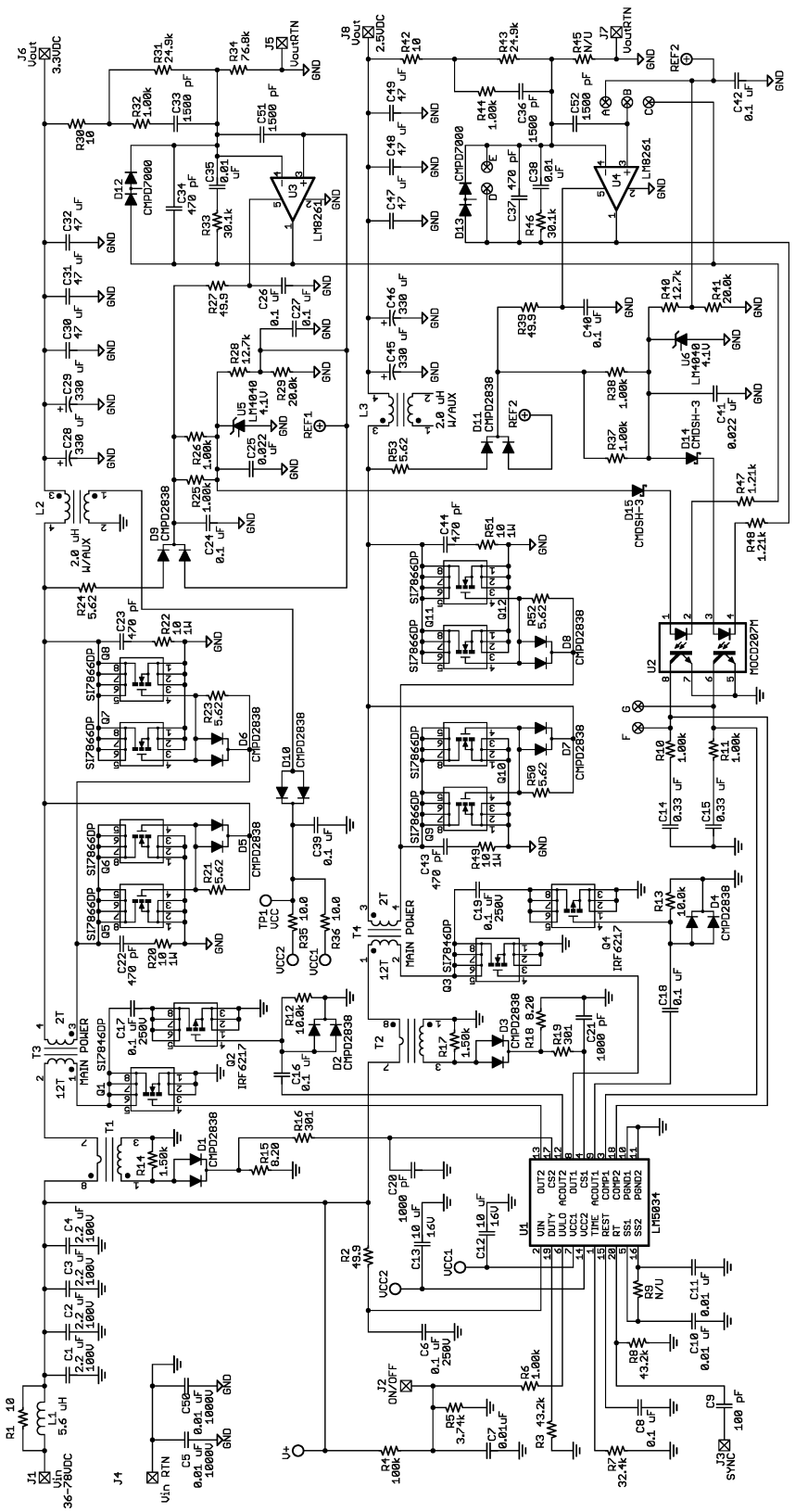


FIGURE 14. Evaluation Board Schematic

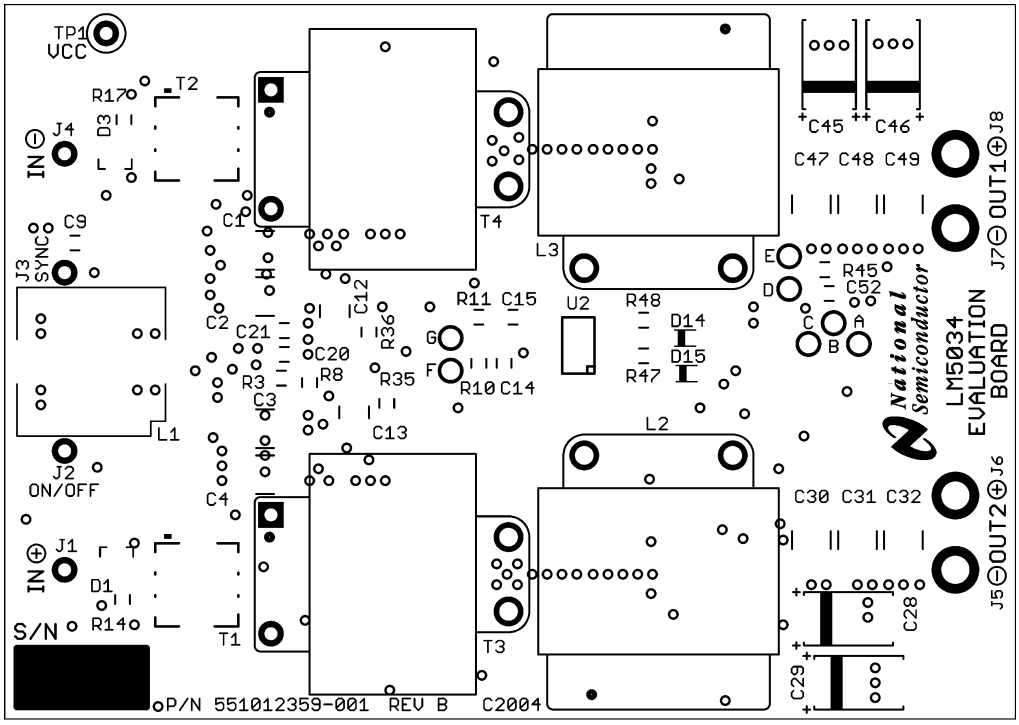
Bill of Materials

Item	Description	Package	Value	Mfg. & Part No.
C1-4	Ceramic Capacitor	1812	2.2 µF, 100V	TDK, Vishay or Kemet
C5, 50	Ceramic Capacitor	1812	0.01 µF, 1000V	TDK, Vishay or Kemet
C6, 17, 19	Ceramic Capacitor	1206	0.1 µF, 250V	TDK, Vishay or Kemet
C7, 10, 11, 35, 38	Ceramic Capacitor	0805	0.01 µF, 50V	TDK, Vishay or Kemet
C8, 16, 18, 24, 26, 27, 39, 40, 42	Ceramic Capacitor	0805	0.1 µF, 50V	TDK, Vishay or Kemet
C9	Ceramic Capacitor	0805	100 pF	TDK, Vishay or Kemet
C12, 13	Ceramic Capacitor	1210	10 µF, 16V	TDK, Vishay or Kemet
C14, 15	Ceramic Capacitor	0805	0.33 µF	TDK, Vishay or Kemet
C20, 21	Ceramic Capacitor	0805	1000 pF	TDK, Vishay or Kemet
C22, 23, 34, 37, 43, 44	Ceramic Capacitor	0805	470 pF	TDK, Vishay or Kemet
C25, 41	Ceramic Capacitor	0805	0.022 µF	TDK, Vishay or Kemet
C28, 29, 45, 46	Tantalum Capacitor	3018	330 µF, 6.3V	TDK, Vishay or Kemet
C30-32, 47-49	Ceramic Capacitor	1812	47 µF	TDK, Vishay or Kemet
C33, 36, 51, 52	Ceramic Capacitor	0805	1500 pF	TDK, Vishay or Kemet
D1-D11	Dual Diode	SOT-23	75V, 200 mA	Central Semi CMPD2838
D12, 13	Dual Diode	SOT-23	100V, 200 mA	Central Semi CMPD7000
D14, 15	Schottky diode	SOD-323	30V, 100 mA	Central Semi CMDSH-3
L1	Inductor	12.5 x 12.5	5.6 µH, 6A	TDK SLF12575-5R6N6R3
L2, 3	Inductor w/ aux out	0.92 x 0.81	2 µH, 30A	Coilcraft B0358-C
Q1, 3	N-MOSFET	SO8	150V, 4A	Vishay Si7846DP
Q2, 4	P-MOSFET	SO8	150V, 0.7A	Int'l Rect. IRF6217
Q5-12	N-MOSFET	SO8	20V, 25A	Vishay Si7866DP
R1	Resistor	1206	10Ω, 1/8W	Vishay
R2	Resistor	1206	49.9Ω, 1/8W	Vishay
R3, 8	Resistor	0805	43.2kΩ	Vishay
R4	Resistor	0805	100kΩ	Vishay
R5	Resistor	0805	3.74kΩ	Vishay
R6, 10, 11, 25, 26, 32, 37, 38, 44	Resistor	0805	1.0kΩ	Vishay
R7	Resistor	0805	32.4kΩ	Vishay
R9, 45	Resistor	0805	Open	
R12, 13	Resistor	0805	10kΩ	Vishay
R14, 17	Resistor	0805	1.5kΩ	Vishay
R15, 18	Resistor	0805	8.2Ω	Vishay
R16, 19	Resistor	0805	301Ω	Vishay
R20, 22, 49, 51	Resistor	2512	10Ω, 1W	Vishay
R21, 23, 24, 50, 52, 53	Resistor	0805	5.62Ω	Vishay
R27, 39	Resistor	0805	49.9Ω	Vishay
R28, 40	Resistor	0805	12.7kΩ	Vishay
R29, 41	Resistor	0805	20kΩ	Vishay
R30, 35, 36, 42	Resistor	0805	10Ω	Vishay
R31, 43	Resistor	0805	24.9kΩ	Vishay
R33, 46	Resistor	0805	30.1kΩ	Vishay
R34	Resistor	0805	76.8kΩ	Vishay
R47, 48	Resistor	0805	1.21kΩ	Vishay
T1, 2	Transformer	0.33 x 0.28	100:1, 6A	Pulse Eng. P8208T
T3, 4	Transformer	0.92 x 0.81	12:2, 30A	Coilcraft B0357-B
U1	PWM dual controller	TSSOP-20		Nat'l Semi LM5034MTC
U2	Dual Opto-coupler	SO8		Fairchild MOCD207M

Bill of Materials (Continued)

Item	Description	Package	Value	Mfg. & Part No.
U3, 4	Op Amp	SOT23-5		Nat'l Semi LM8261M5
U5, 6	Reference	SOT23		Nat'l Semi LM4040CIM3-4.1

PCB Layouts



TOP SILKSCREEN (.PLC) LAYER AS VIEWED FROM TOP

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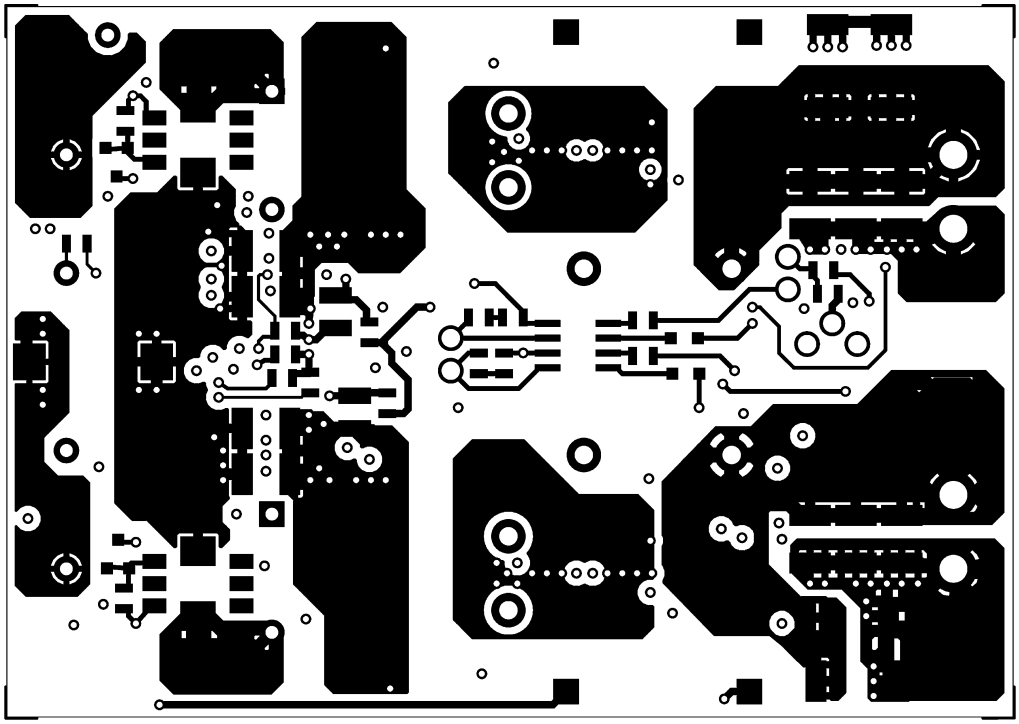
FIGURE 15. Top Silk Screen Layer



TOP (.CMP) LAYER AS VIEWED FROM TOP

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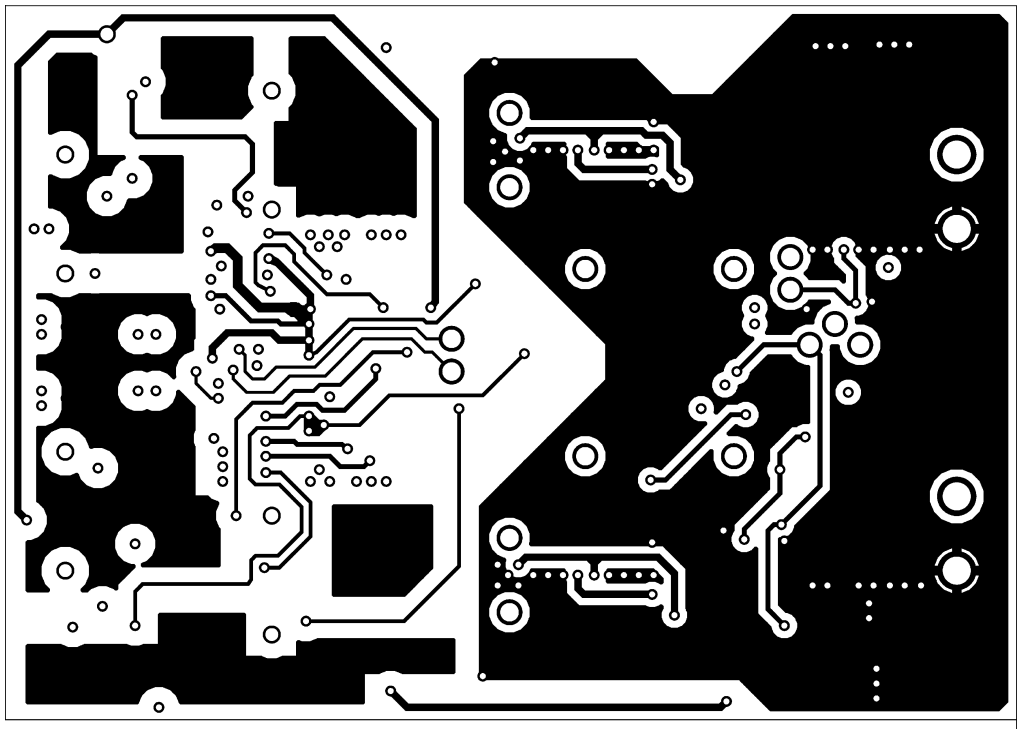
FIGURE 16. Top Layer

PCB Layouts (Continued)



LAYER 2 (.LY2) AS VIEWED FROM TOP

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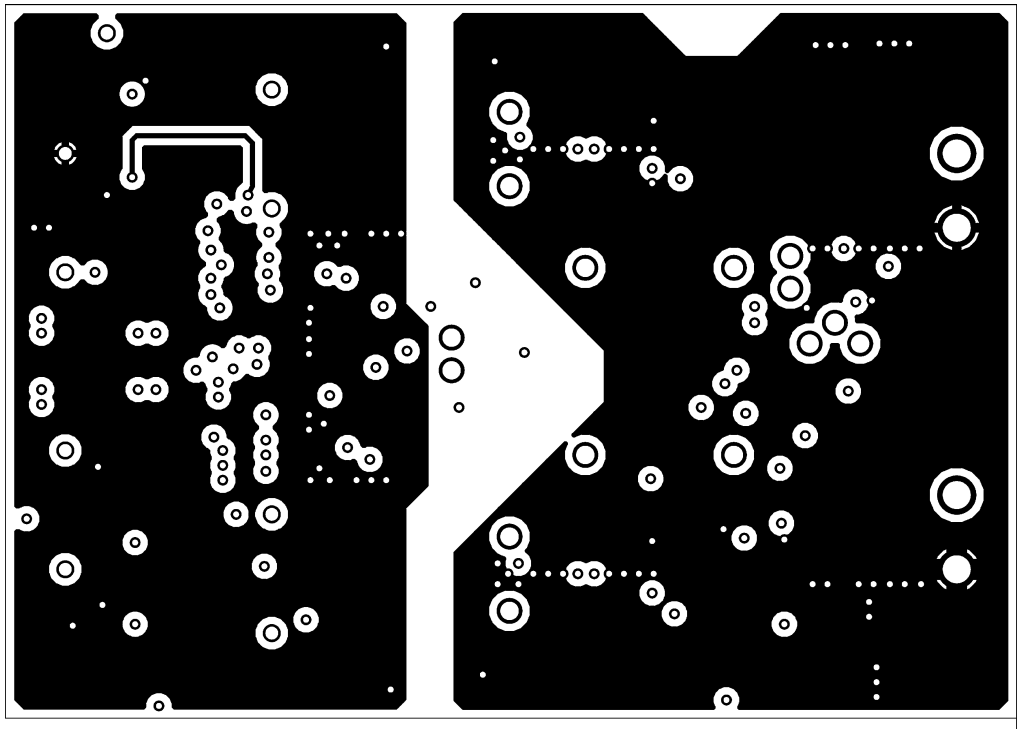
FIGURE 17. Layer 2



LAYER 3 (.LY3) AS VIEWED FROM TOP

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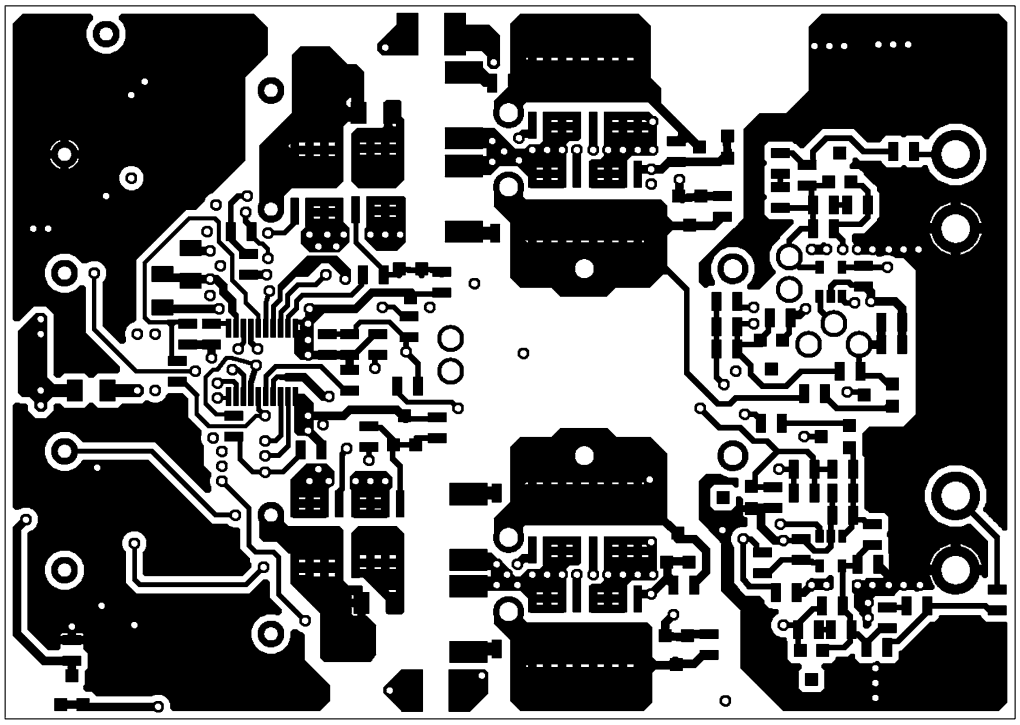
FIGURE 18. Layer 3

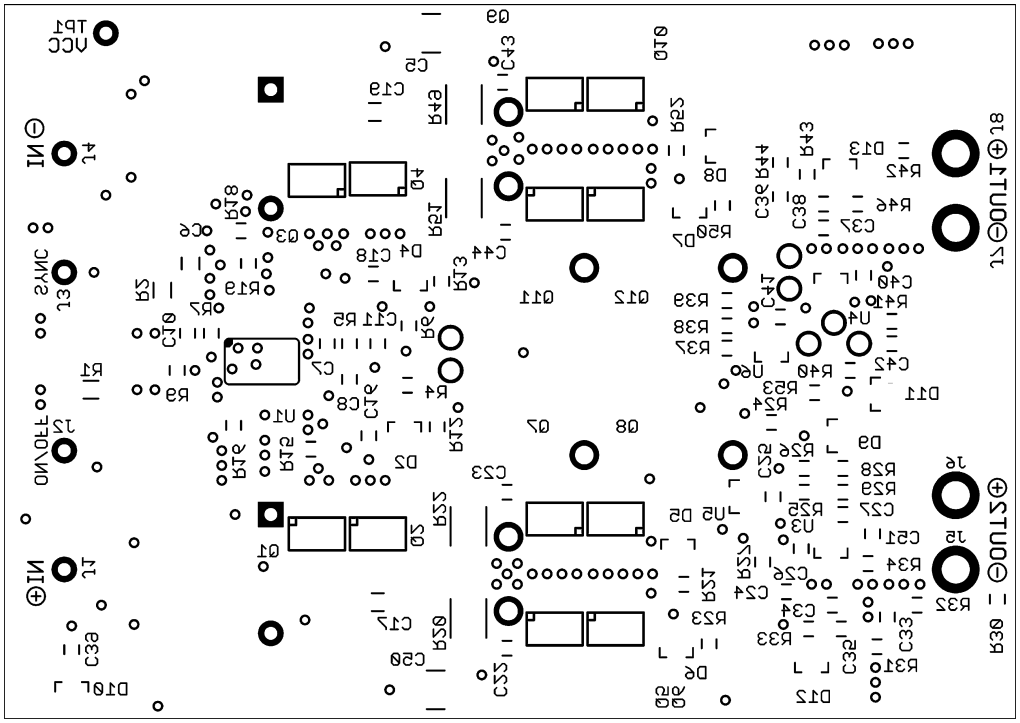
PCB Layouts (Continued)



BOTTOM (.S0L) LAYER AS VIEWED FROM TOP

20141719

FIGURE 19. Bottom Layer (as viewed from top)



BOTTOM SILKSCREEN (.BPL) LAYER AS VIEWED FROM TOP

20141720

FIGURE 20. Bottom Silk Screen Layer (as viewed from top)

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