LM3280 Evaluation Board

National Semiconductor
Application Note 1539
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January 2007

Introduction

The LM3280 evaluation board is designed to demonstrate the capability of the LM3280 power management device, which incorporates a step down DC-DC (buck) converter and three LDOs. This application note contains information about the evaluation board. For further information on buck converter topology, device electrical characteristics, and component selection please refer to the datasheet.

General Description

The buck converter coverts high input voltages to lower output voltages with high efficiency through an inductor-based switching topology. It has three operating modes. Fixed-frequency (2MHz) PWM mode operation offers regulated output at high efficiency. Bypass mode operation uses an internal FET switch to connect the input supply voltage directly to the load. Shutdown mode turns the device off and reduces the input supply consumption. The mode selection between PWM and Bypass can be fixed by the BYP pin setting.

The LDO provides a nominal output voltage of 2.85V with a maximum load current capability of 20mA. It has a separate enable pin for each LDO.

Operating Conditions

The evaluation board will operate under the recommended conditions below.

V_{IN} :		2.7V to 5.5V
V_{CON} :		0.267V to 1.20V
V_{OUT} equation :		V_{OUT} = 3 x V_{CON}
I_{OUT_BUCK}	@PWM mode :	0mA to 300mA
	@Bypass mode :	0mA to 500mA
I_{OUT_LDO} :		0mA to 20mA
Ambient temperature (T_A) :		-30°C to +85°C

Powering Up

The EN_{BUCK} pin should be set low to turn off the LM3280 during power-up and under voltage conditions when the V_{IN} is less than the 2.7V minimum operating voltage.

The LDO can be enabled only after the buck converter is activated. Single LDO must be turned on at the same time.

Schematic Diagram

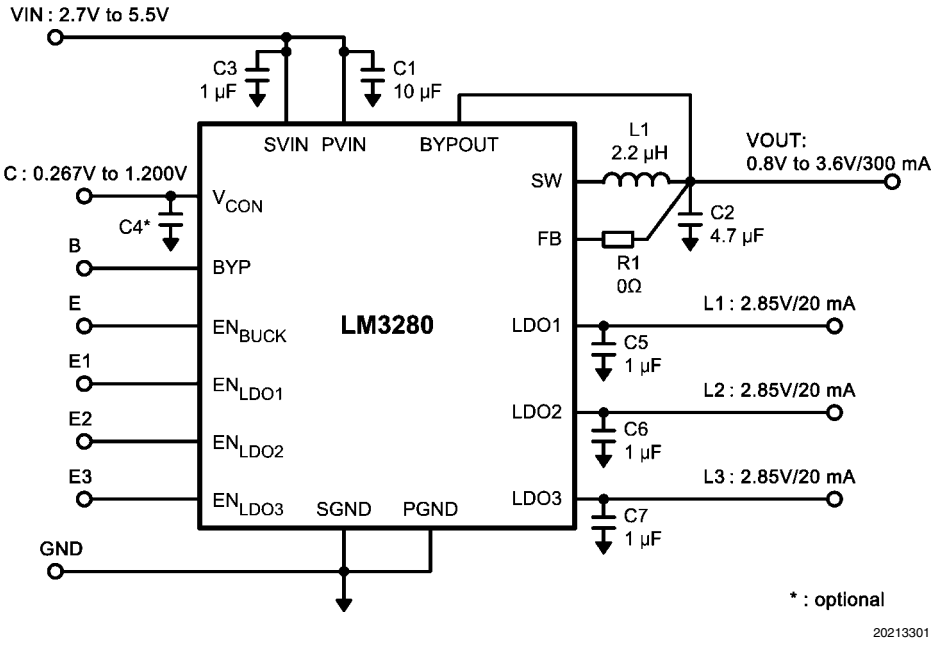


FIGURE 1. Evaluation Board Schematic

BOM for Common Configurations

Designator	Manufacture	Model	Description
C1	TDK	C2012X5R0J106M	10µF, 6.3V, 0805 (2012)
C2	TDK	C1608X5R0J475M	4.7µF, 6.3V, 0603 (1608)
C3	TDK	C1608JB1C105K	1.0µF, 16V , 0603 (1608)
C4			0.1µF, 6.3V, 0603 (1608), * optional: filter for V_{CON}. C4 is recommended for a better noise performance.
C5	TDK	C1608JB1C105K	1.0µF, 16V , 0603 (1608)
C6	TDK	C1608JB1C105K	1.0µF, 16V , 0603 (1608)
C7	TDK	C1608JB1C105K	1.0µF, 16V , 0603 (1608)
L1	Coilcraft	DO3314-222MLC	2.2 µH, Irms = 1.3A, Rdc = 0.2Ω, 3.5×3.5×1.4 mm
R1			0Ω, 0603 (1608)
VIN	Keystone	1502-1	test terminal
VOUT	Keystone	1502-1	test terminal
GND	Keystone	1502-1	test terminal

Component Selection Considerations

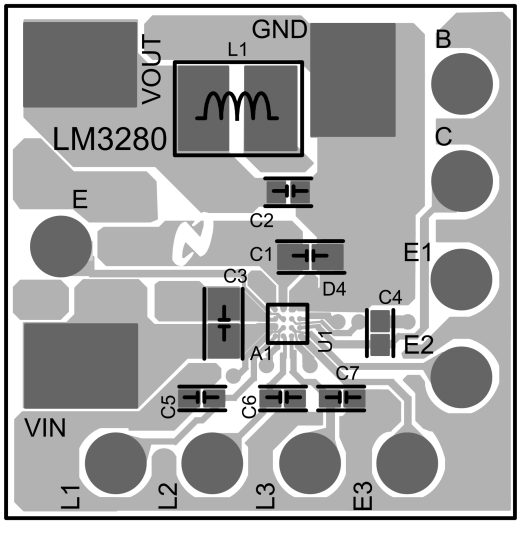
INDUCTOR

1. A 2.2µH inductor with a saturation current rating of over 940mA is recommended.
2. The inductor resistance should be less than 0.2Ω for better efficiency.
3. The acceptable inductance tolerance is 1.55µH to 3.1µH over the operating temperature range.

CAPACITOR

1. The DC bias and temperature characteristics of the capacitor must be considered.
2. The lower limit of acceptable C2 capacitance for stable performance is 3µF.
3. The lower limit of acceptable LDO caps, C5, C6, and C7, is 0.5µF.
4. A 10µF capacitor for PVIN and a 1µF capacitor for SVIN are recommended. Smaller capacitance may be acceptable if the VIN line is sufficiently clean. Sufficient evaluation must be done before making a decision to use smaller capacitance.

Evaluation Board Layout



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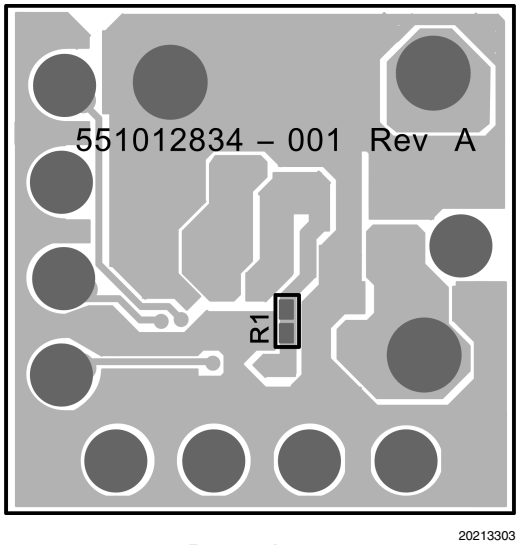
Top Layer



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Bottom Layer

FIGURE 2. Board Layout

Board Layout Consideration

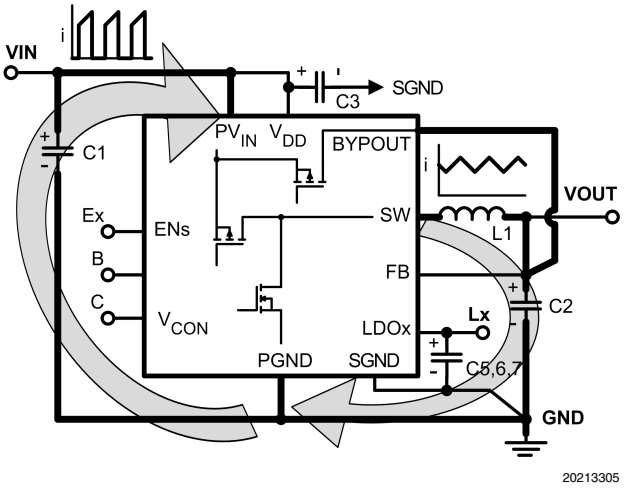

FIGURE 3. Current Loop

The LM3280 converts higher input voltage to lower output voltage with high efficiency. This is achieved with an inductor-based switching topology. During the first half of the switching cycle, the internal PFET switch turns on, the input voltage is applied to the inductor, and the current flows from PVIN line to the output capacitor (C2) through the inductor. During the second half cycle, the PFET turns off and the internal NFET turns on. The inductor current continues to flow via the inductor from the device PGND line to the output capacitor (C2).

Referring to Figure, the LM3280 in PWM mode has two major current loops where pulse and ripple current flow. The loop shown in the left had side is important because pulse current flows in the path. In the loop on the right hand side, the current waveform in this path is triangular. Pulse current has many high-frequency components due to fast di/dt. Triangular ripple current also has wide high-frequency components. Board layout and circuit pattern design of these two loops are key factors for reducing noise radiation and achieving stable operation. Other lines, such as input and output terminals are DC current, Therefore pattern width (current capability) and DCR drop considerations are needed.

BOARD LAYOUT GUIDELINES

1. Minimize C1, PVIN, and PGND loop. These traces should be as wide and short as possible.
2. Minimize L1, C2, SW and PGND loop. These traces also should be wide and short.
3. Above layout patterns should be placed on the component side of the PCB to minimize parasitic inductance and resistance due to via-holes. It may be a good idea that the SW to L1 path is routed between C2 (+) and C2(-) land patterns. If vias are used in these large current paths, multiple via-holes should be used if possible.
4. Connect C1(-), C2(-), and PGND with side GND pattern. This pattern should be short, so C1(-), C2(-), and PGND should be as close as possible. Then connect to a PCB common GND pattern with as many via-holes as possible.
5. SGND should not connect directly to PGND. Connecting these pins under the device should be avoided. (If possible, connect SGND to the common port of C1(-), C2 (-), and PGND.)
6. Place C3 as close to SVIN as possible to avoid noise.
7. FB line should be protected from noise. It is a good idea to use an inner GND layer (if available) as a shield.
8. It is recommended to connect BYPOUT to VOUT at C2 (+) using a separate trace, instead of connecting it directly to the FB for better noise immunity.
9. The LDO caps, C5, C6, and C7, should be placed as far away from the buck convertor as possible to suppress high frequency switching noise.

Connection Diagram and Package Mark Information

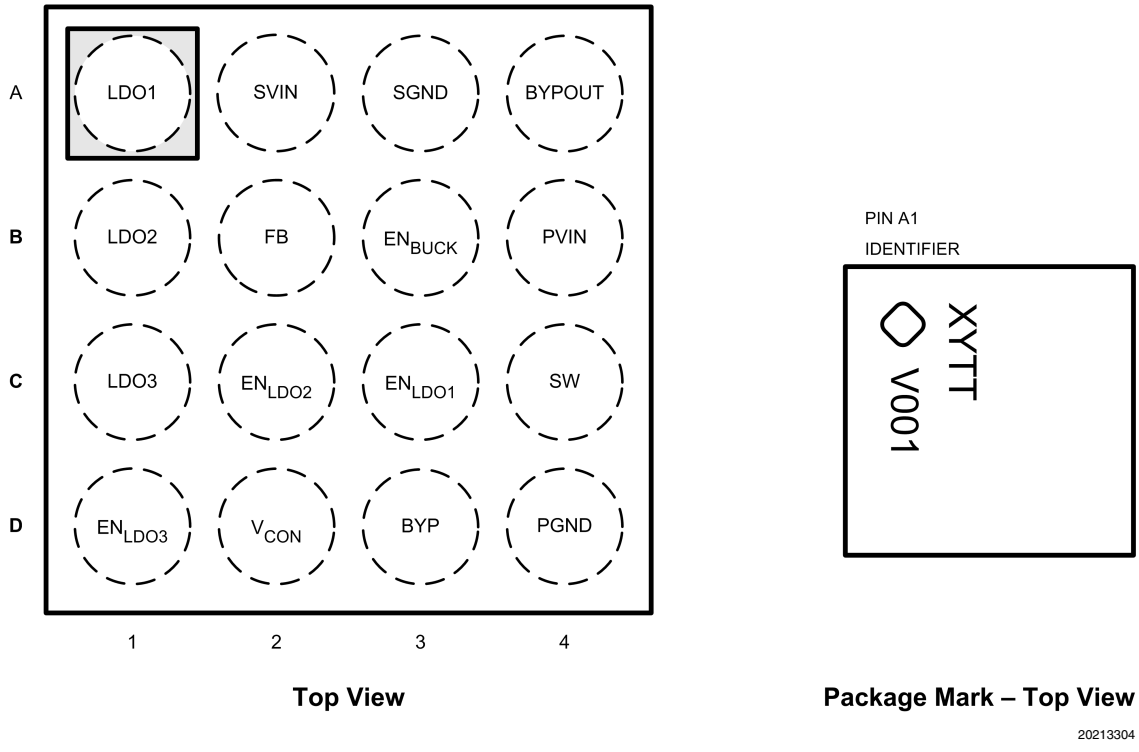

FIGURE 4. 16–Bump Thin Micro SMD Package

Pin Descriptions

Pin #	Name	Description
A1	LDO1	LDO1 Output.
B1	LDO2	LDO2 Output.
C1	LDO3	LDO3 Output.
D1	EN_{LDO3}	LDO3 Enable Input. Set this digital input high to turn on LDO3. (EN_{BUCK} pin must be also set high.) For turning LDO3 off, set low.
A2	SVIN	Analog, Signal and LDO Supply Input.
B2	FB	Buck Converter Feedback Analog Input. Connect to the output at the output filter capacitor.
C2	EN_{LDO2}	LDO2 Enable Input. Set this digital input high to turn on LDO2. (EN_{BUCK} pin must be also set high.) For turning LDO2 off, set low.
D2	V_{CON}	Buck Converter Voltage Control Analog Input. This pin controls V_{OUT} in PWM mode. Set: $V_{OUT} = 3 \times V_{CON}$. Do not leave floating.
A3	SGND	Analog, Signal, and LDO Ground.
B3	EN_{BUCK}	Buck Converter Enable Input. Set this digital input high after $V_{IN} > 2.7V$ for normal operation. For shutdown, set low.
C3	EN_{LDO1}	LDO1 Enable Input. Set this digital input high to turn on LDO1. (EN_{BUCK} pin must be also set high.) For turning LDO1 off, set low.
D3	BYP	Forced Bypass Input. Use this digital input to command operation in Bypass mode. Set BYP low for normal operation.
A4	BYPOUT	Bypass FET Drain. Connect to the output capacitor. Do not leave floating.
B4	PVIN	Buck Converter Power Supply Voltage Input to the internal P-FET switch and Bypass FET.
C4	SW	Buck Converter Switch Node connection to the internal P-FET switch and N-FET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit of the PWM Buck Converter.
D4	PGND	Buck Converter Power Ground.

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