LM3207 Evaluation Board

National Semiconductor
Application Note 1505
Jeffrey Colwell
July 2007

Introduction

The LM3207 evaluation board is a working demonstration of a step down DC-DC converter. This application note contains information about the evaluation board and board layout considerations. For further information on buck converter topology, device electrical characteristics, and component selection please refer to the LM3207 datasheet.

General Description

The LM3207 is a DC-DC converter optimized for powering RF power amplifiers (RFPAs) from a single Lithium-Ion cell, however the device may be used in many other applications. The LM3207 steps down an input voltage range from 2.7V to 5.5V to a variable output voltage range from 0.8V to 3.6V. Output voltage is set using a V_{CON} analog input for controlling power levels and efficiency of the RF PA.

The LM3207 also provides a regulated reference voltage (Vref) required by linear RF power amplifiers through an integrated LDO with a nominal has a maximum Iref of 10 mA. See Ordering Information table on page 2 for Voltage Options.

The LM3207 offers superior performance for powering WCMDA / CDMA RF power amplifiers and similar applications. Fixed-frequency PWM operation minimizes RF interference. Shutdown function turns the device off and reduces battery consumption to 0.01 µA (typ).

The LM3207 is available in a 9-pin lead free micro SMD package. A high switching frequency (2 MHz) allows use of tiny surface-mount components. Only four small external components are required, an inductor and three ceramic capacitors.

Operating Conditions

- V_{IN} range: 2.7V ≤ V_{IN} ≤ 5.5V
- V_{CON} range: 0.32V ≤ V_{CON} ≤ 1.44V
- V_{OUT} equation: V_{OUT} = 2.5 x V_{CON}
- I_{OUT} range: 0 mA≤ I_{OUT} ≤ 650 mA

Typical Application

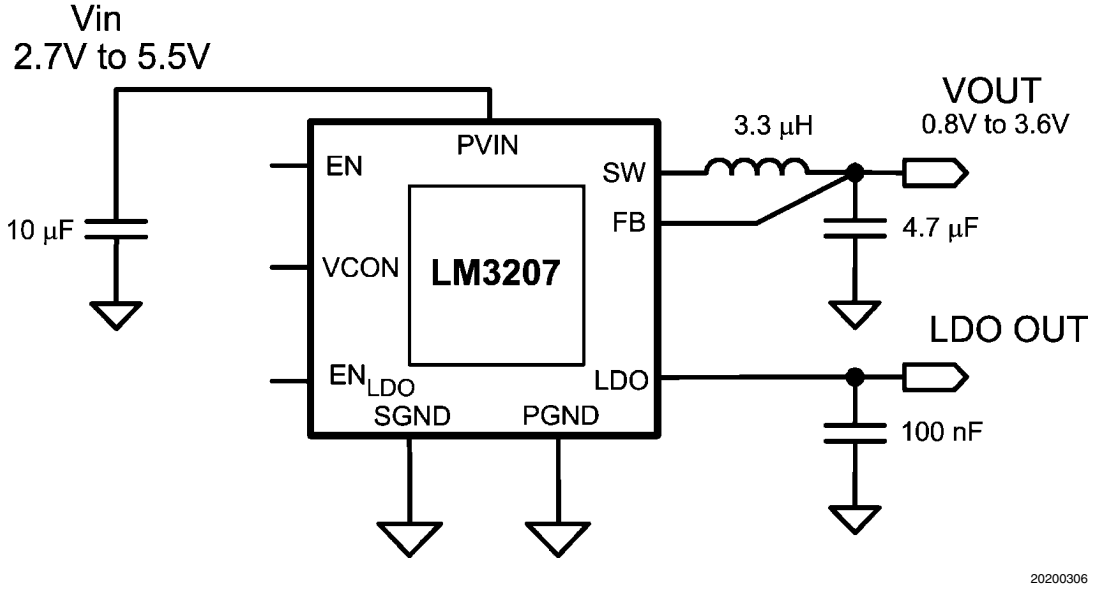
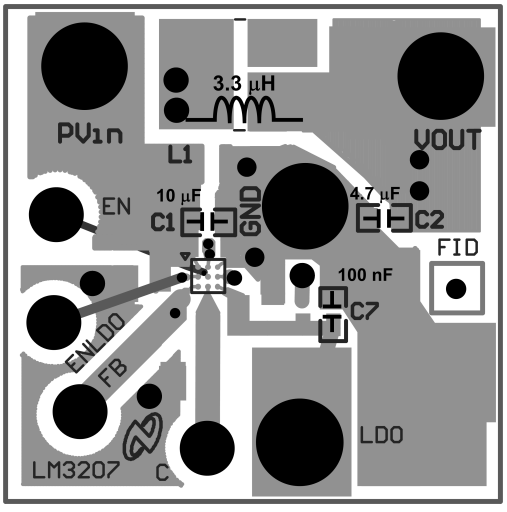


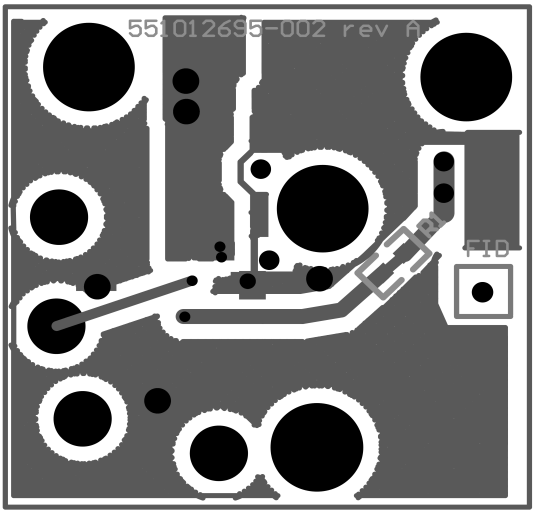
FIGURE 1. Typical Application Circuit

Evaluation Board Layout



20200307

FIGURE 2. Top Layer



20200311

FIGURE 3. Bottom Layer

Order Information

LDO Voltage Option	Order Number	Part Marking (Note)	Supplied As
2.875	LM3207TL	XVS/34	250 units, Tape-and-Reel
	LM3207TLX	XVS/34	3000 units, Tape-and-Reel
2.53	LM3207TL-2.53	XVS/43	250 units, Tape-and-Reel
	LM3207TLX-2.53	XVS/43	3000 units, Tape-and-Reel

Note: The actual physical placement of the package marking will vary from part to part. The package marking "X" designates the date code. "V" is a NSC internal code for die traceability. Both will vary considerably. "S" designates the device type as switcher device. "34" identifies the device part number/option.

Connection Diagram and Package Mark Information

Top View **Package Mark - Top View**

20200305

FIGURE 4.
9–Bump Thin Micro SMD Package, Large Bump
NS Package Number TLA09TTA

Pin Descriptions

Pin #	Name	Description
A1	PV_{IN}	Power Supply Voltage Input to the internal PFET switch.
B1	EN_{LDO}	LDO Enable Input. Set this digital input high to turn on LDO (EN pin must also be set high). For shutdown, set low.
C1	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.
C2	V_{CON}	Voltage Control Analog input. V_{CON} controls V_{OUT} in PWM mode.
C3	LDO	LDO Output Voltage.
B3	SGND	Analog and Control Ground
A3	PGND	Power Ground
A2	SW	Switch node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the LM3207.
B2	EN	PWM enable Input. Set this digital input high for normal operation. For shutdown, set low.

BOM For Common Configurations

	Manufacture	Manufacture #	Description
C1 (input C)	TDK	C1608X5R0J106M	10 µF,6.3V,10%,0603
C2 (output C)	TDK	C1608X5R0J475M	4.7 µF,6.3V,10%,0603
C3 (optional, input C)			0.1 µF,25V , 0402(Note 1)
C4 (optional, filter for V_{CON})			10 - 100 pF, 25V , 0402(Note 1)
C7 (LDO Cap)	TDK	C1005X5R1A104KT	100nF,10V, 0402
L1 (inductor)	Taiyo-Yuden	NR3015T3R3M	3.3 µH, 1210mA, 3×3×1.5 mm
V_{IN} banana jack - red	Johnson Components	108-0902-001	connector, insulated banana jack (red)
V_{out} banana jack - yellow	Johnson Components	108-0907-001	connector, insulated banana jack (yellow)

	Manufacture	Manufacture #	Description
GND banana jack - black	Johnson Components	108-0903-001	connector, insulated banana jack (black)
LDO Out banana jack - yellow	Johnson Components	108-0907-001	connector, insulated banana jack (yellow)

Note 1: C3 and C4 are recommended for a better noise performance.

Board Layout Considerations

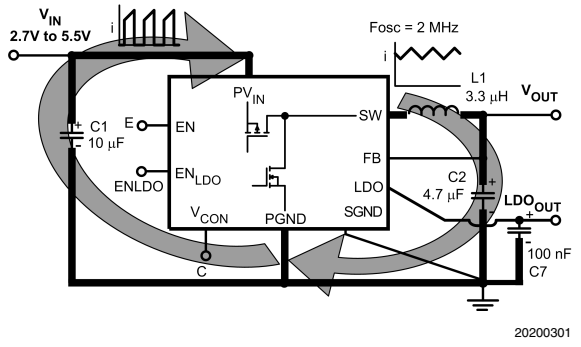


FIGURE 5. Current Loop

The LM3207 converts higher input voltage to lower output voltage with high efficiency. This is achieved with an inductor-based switching topology. During the first half of the switching cycle, the internal PMOS switch turns on, the input voltage is applied to the inductor, and the current flows from P_{VIN} line to the output capacitor (C2) through the inductor. During the second half cycle, the PMOS turns off and the internal NMOS turns on. The inductor current continues to flow via the inductor from the device PGND line to the output capacitor (C2). The inductor current continues to flow via the inductor from the device PGND line to the output capacitor (C2) .

Referring to *Figure 5*, the LM3207 has two major current loops where pulse and ripple current flow. The loop shown in the left hand side is important because pulse current flows in this path. In the loop on the right hand side, the current waveform in this path is triangular. Pulse current has many high-frequency components due to fast di/dt. Triangular ripple current also has wide high-frequency components. Board layout and circuit pattern design of these two loops are key factors for reducing noise radiation and achieving stable operation. Other lines, such as input and output terminals are DC current, therefore pattern width (current capability) and DCR drop considerations are needed.

BOARD LAYOUT FLOW

1. Minimize C1, PV_{IN}, and PGND loop. These traces should be as wide and short as possible. This is most important.
2. Minimize L1, C2, SW and PGND loop. These traces also should be wide and short. This is the second priority.
3. Above layout patterns should be placed on the component side of the PCB to minimize parasitic inductance and resistance due to via-holes. It may be a good idea that the SW to L1 path is routed between C2 (+) and C2(-) land patterns. If vias are used in these large current paths, multiple via-holes should be used if possible.
4. Connect C1(-), C2(-) and PGND with wide GND pattern. This pattern should be short, so C1(-), C2(-), and PGND should be as close as possible. Then connect to a PCB common GND pattern with as many via-holes as possible.
5. SGND should not connect directly to PGND. Connecting these pins under the device should be avoided. (If possible, connect SGND to the common port of C1(-), C2 (-) and PGND.)
6. FB line should be protected from noise. It is a good idea to use an inner GND layer (if available) as a shield.
7. The LDO Cap C7 should be placed as close to the PA as possible and as far away from the switcher to suppress high frequency switch noises.

Note: The evaluation board shown in *Figure 2* and *Figure 3* for the LM3207 was designed with the considerations mentioned above, and it shows good performance. However some aspects have not been optimized because of limitations due to evaluation-specific requirements. The board can be used as a reference. For specific questions, please refer to a National representative.

Notes

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530-85-86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +49 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560