National Semiconductor

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LM2716
Dual (Step-Up and Step-Down) PWM DC/DC Converter

General Description

The LM2716 is composed of two PWM DC/DC converters. A buck (step-down) converter is used to generate a fixed output voltage of 3.3V. A boost (step-up) converter is used to generate an adjustable output voltage. Both converters feature low R_{DSON} (0.16Ω and 0.12Ω) internal switches for maximum efficiency. Operating frequency can be adjusted anywhere between 300kHz and 600kHz allowing the use of small external components. External soft-start pins for each enables the user to tailor the soft-start times to a specific application. Each converter may also be shut down independently with its own shutdown pin. The LM2716 is available in a low profile 24-lead TSSOP package.

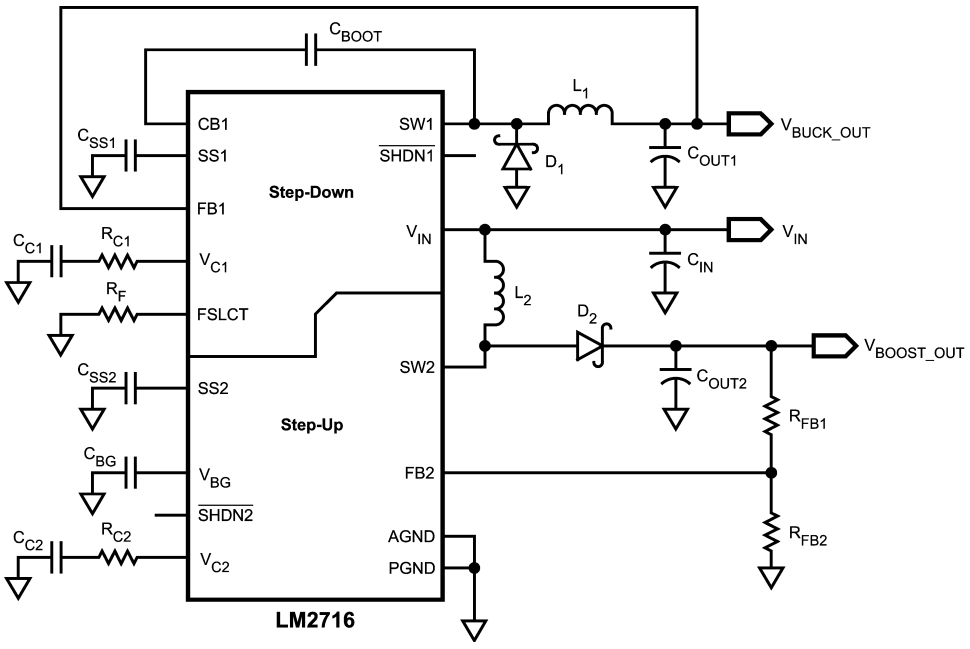
Features

- Fixed 3.3V buck converter with a 1.8A, 0.16Ω, internal switch
- Adjustable boost converter with a 3.6A, 0.12Ω, internal switch
- Adjustable boost output voltage up to 20V
- Operating input voltage range of 4V to 20V
- Input undervoltage protection
- 300kHz to 600kHz pin adjustable operating frequency
- Over temperature protection
- Small 24-Lead TSSOP package
- Patented current limit circuitry

Applications

- TFT-LCD Displays
- Handheld Devices
- Portable Applications
- Cellular Phones/Digital Camers

Typical Application Circuit



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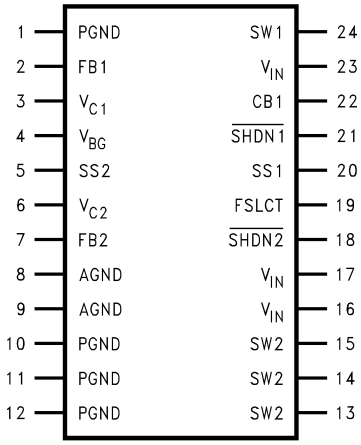
Connection Diagram

Top View



TSSOP 24 Package

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24-Lead TSSOP

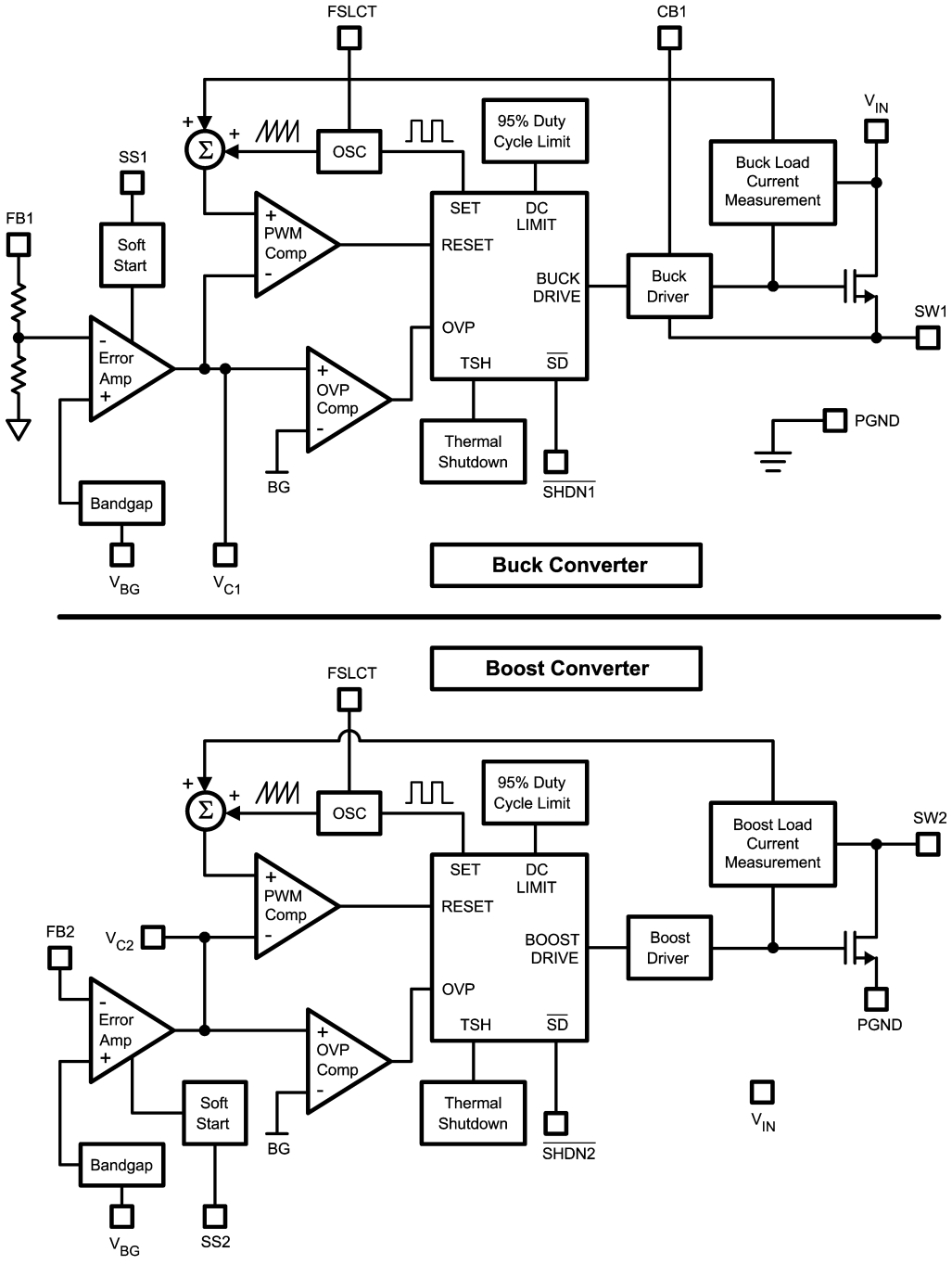
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2716MT	TSSOP-24	MTC24	61 Units, Rail
LM2716MTX	TSSOP-24	MTC24	2500 Units, Tape and Reel

Pin Descriptions

Pin	Name	Function
1	PGND	Power ground. AGND and PGND pins must be connected together directly at the part.
2	FB1	Buck output voltage feedback input.
3	V_{C1}	Buck compensation network connection. Connected to the output of the voltage error amplifier.
4	V_{BG}	Bandgap connection.
5	SS2	Boost soft start pin.
6	V_{C2}	Boost compensation network connection. Connected to the output of the voltage error amplifier.
7	FB2	Boost output voltage feedback input.
8	AGND	Analog ground. AGND and PGND pins must be connected together directly at the part.
9	AGND	Analog ground. AGND and PGND pins must be connected together directly at the part.
10	PGND	Power ground. AGND and PGND pins must be connected together directly at the part.
11	PGND	Power ground. AGND and PGND pins must be connected together directly at the part.
12	PGND	Power ground. AGND and PGND pins must be connected together directly at the part.
13	SW2	Boost power switch input. Switch connected between SW2 pins and PGND pins. SW2 pins should be connected directly together at the device.
14	SW2	Boost power switch input. Switch connected between SW2 pins and PGND pins. SW2 pins should be connected directly together at the device.
15	SW2	Boost power switch input. Switch connected between SW2 pins and PGND pins. SW2 pins should be connected directly together at the device.
16	V_{IN}	Analog power input. V_{IN} pins must be connected together directly at the DUT.
17	V_{IN}	Analog power input. V_{IN} pins must be connected together directly at the DUT.
18	$\overline{SHDN2}$	Shutdown pin for Boost converter. Active low.
19	FSLCT	Switching frequency select input. Use a resistor to set the frequency anywhere between 300kHz and 600kHz.
20	SS1	Buck soft start pin.
21	$\overline{SHDN1}$	Shutdown pin for Buck converter. Active low.
22	CB1	Buck converter bootstrap capacitor connection.
23	V_{IN}	Analog power input. V_{IN} pins must be connected together directly at the DUT.
24	SW1	Buck power switch input. Switch connected between V_{IN} pins and SW1 pin.

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}	−0.3V to 22V
SW1 Voltage	−0.3V to 22V
SW2 Voltage	−0.3V to 22V
FB1 Voltage	−0.3V to 7V
FB2 Voltage	−0.3V to 7V
V_{C1} Voltage	$1.75V \le V_{C1} \le 2.25V$
V_{C2} Voltage	$0.965V \le V_{C2} \le 1.565V$
$\overline{SHDN1}$ Voltage	−0.3V to 7.5V
$\overline{SHDN2}$ Voltage	−0.3V to 7.5V
SS1 Voltage	−0.3V to 2.1V
SS2 Voltage	−0.3V to 0.6V
FSLCT Voltage	AGND to 5V
CB1 Voltage	V_{IN} + 7V ($V_{IN} = V_{SW}$)
Maximum Junction Temperature	150˚C
Power Dissipation(Note 2)	Internally Limited
Lead Temperature	300˚C
Vapor Phase (60 sec.)	215˚C
Infrared (15 sec.)	220˚C
ESD Susceptibility (Note 3)	
Human Body Model	2kV
Machine Model	200V

Operating Conditions

Operating Junction Temperature Range (Note 4)	−40˚C to +125˚C
Storage Temperature	−65˚C to +150˚C
Supply Voltage	4V to 20V
SW1 Voltage	20V
SW2 Voltage	20V

Electrical Characteristics

Specifications in standard type face are for T_J = 25˚C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40˚C to +125˚C) Unless otherwise specified. V_{IN} = 5V and I_L = 0A, unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
I_Q	Total Quiescent Current (both switchers)	Not Switching		2.8	**3.5**	mA
		Switching, switch open		4	**4.5**	mA
		$V_{\overline{SHDN}}$ = 0V		9	**15**	µA
V_{BG}	Bandgap Voltage		**1.235**	1.26	**1.285**	V
I_{CL1}(Note 6)	Buck Switch Current Limit	95% Duty Cycle (Note 7)		1.8		A
I_{CL2}(Note 6)	Boost Switch Current Limit	95% Duty Cycle (Note 7)		3.6		A
I_{FB1}	Buck FB Pin Bias Current (Note 8)	V_{FB1} = 3.3V		65	75	µA
I_{FB2}	Boost FB Pin Bias Current (Note 8)	V_{FB2} = 1.265V		27	55	nA
V_{IN}	Input Voltage Range		**4**		**20**	V
g_{m1}	Buck Error Amp Transconductance	ΔI = 20µA		1200		µmho
g_{m2}	Boost Error Amp Transconductance	ΔI = 5µA		175		µmho
A_{V1}	Buck Error Amp Voltage Gain			100		V/V
A_{V2}	Boost Error Amp Voltage Gain			135		V/V
D_{MAX}	Maximum Duty Cycle		**90**	95	**98**	%
F_{SW}	Switching Frequency	R_F = 47.5kΩ	250	300	350	kHz
		R_F = 22.6kΩ	500	600	700	kHz
$I_{\overline{SHDN1}}$	Buck Shutdown Pin Current	$0V < V_{\overline{SHDN1}} < 7.5V$	**−5**		**5**	µA
$I_{\overline{SHDN2}}$	Boost Shutdown Pin Current	$0V < V_{\overline{SHDN2}} < 7.5V$	**−5**		**5**	µA
I_{L1}	Buck Switch Leakage Current	V_{DS} = 20V		0.2	5	µA
I_{L2}	Boost Switch Leakage Current	V_{DS} = 20V		0.2	3	µA
R_{DSON1}	Buck Switch R_{DSON}			160		mΩ
R_{DSON2}	Boost Switch R_{DSON}			120		mΩ

Electrical Characteristics (Continued)

Specifications in standard type face are for T_J = 25˚C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40˚C to +125˚C) Unless otherwise specified. V_{IN} = 5V and I_L = 0A, unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 5)	Max (Note 4)	Units
$Th_{\overline{SHDN1}}$	Buck $\overline{SHDN}$ Threshold	Output High		1.37	**2**	V
		Output Low	**0.8**	1.35		
$Th_{\overline{SHDN2}}$	Boost $\overline{SHDN}$ Threshold	Output High		1.37	**2**	V
		Output Low	**0.8**	1.35		
I_{SS1}	Buck Soft Start Pin Current		**6**	9.5	**12**	µA
I_{SS2}	Boost Soft Start Pin Current		**15**	19	**22**	µA
UVP	On Threshold		**3.35**	3.8	**4.0**	V
	Off Threshold		**3.10**	3.6	**3.9**	
θ_{JA}	Thermal Resistance (Note 9)	TSSOP, package only		115		˚C/W

Note 1: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = ($T_{J(MAX)}$ – T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 4: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested or guaranteed through statistical analysis. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 5: Typical numbers are at 25˚C and represent the most likely norm.

Note 6: Duty cycle affects current limit due to ramp generator.

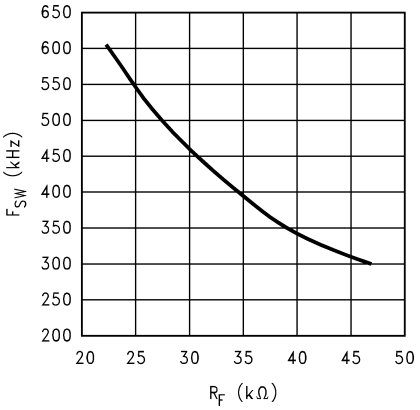
Note 7: Current limit at 95% duty cycle.

Note 8: Bias current flows into FB pin.

Note 9: Refer to National's packaging website for more detailed thermal information and mounting techniques for the TSSOP package.

Typical Performance Characteristics

Switching Frequency vs. R_F Resistor



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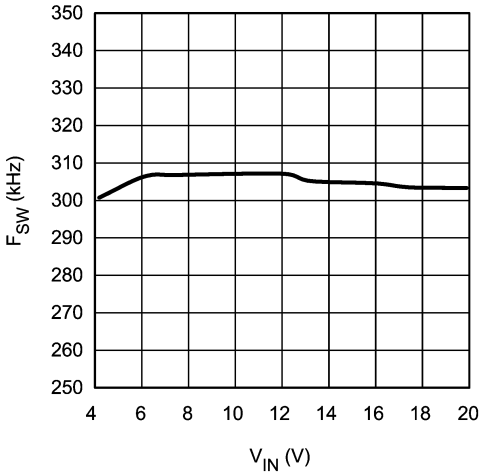
Switching Frequency vs. Input Voltage (F_{SW} = 300kHz)



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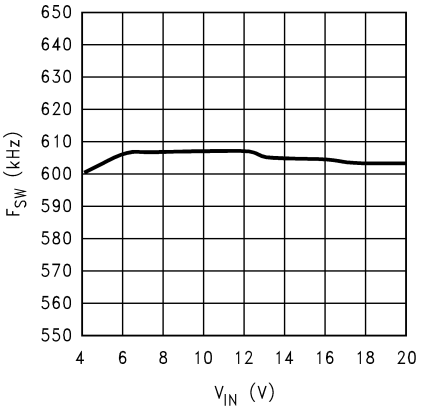
Switching Frequency vs. Input Voltage (F_{SW} = 600kHz)



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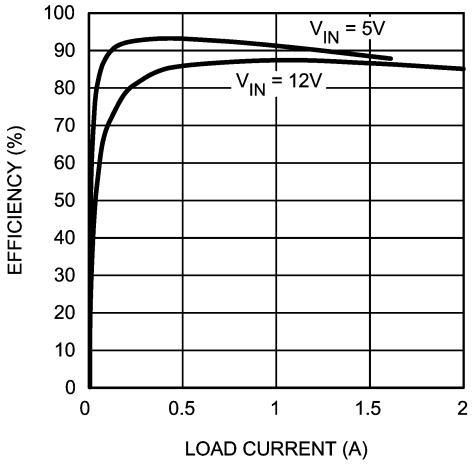
Buck Efficiency vs. Load Current (F_{SW} = 300kHz)



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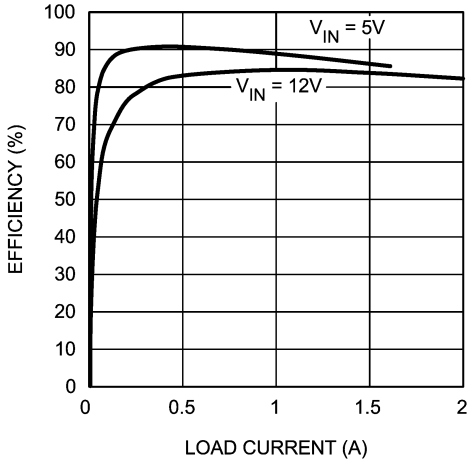
Buck Efficiency vs. Load Current (F_{SW} = 600kHz)



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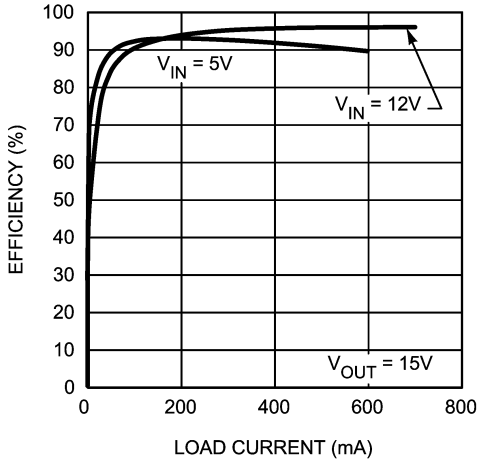
Boost Efficiency vs. Load Current (F_{SW} = 300kHz)



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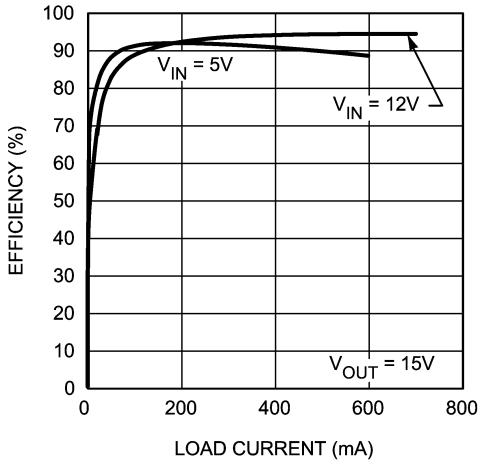
Typical Performance Characteristics (Continued)

Boost Efficiency vs. Load Current (F_{SW} = 600kHz)



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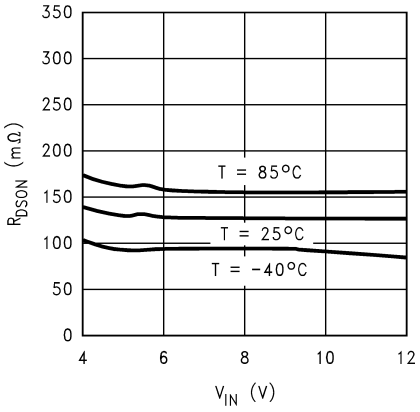
Boost Switch R_{DSON} vs. Input Voltage



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Buck Operation

PROTECTION (BOTH REGULATORS)

The LM2716 has dedicated protection circuitry running during normal operation to protect the IC. The Thermal Shutdown circuitry turns off the power devices when the die temperature reaches excessive levels. The UVP comparator protects the power devices during supply power startup and shutdown to prevent operation at voltages less than the minimum input voltage. The OVP comparator is used to prevent the output voltage from rising at no loads allowing full PWM operation over all load conditions. The LM2716 also features a shutdown mode for each converter decreasing the supply current to 9µA (both in shutdown mode).

CONTINUOUS CONDUCTION MODE

The LM2716 contains a current-mode, PWM buck regulator. A buck regulator steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the buck regulator operates in two cycles. The power switch is connected between V_{IN} and SW1.

In the first cycle of operation the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT} and the rising current through the inductor.

During the second cycle the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$D = \frac{V_{OUT}}{V_{IN}}, \; D' = (1\text{-}D)$$

where D is the duty cycle of the switch, D and D' will be required for design calculations.

DESIGN PROCEDURE

This section presents guidelines for selecting external components.

INPUT CAPACITOR

A low ESR aluminum, tantalum, or ceramic capacitor is needed betwen the input pin and power ground. This capacitor prevents large voltage transients from appearing at the input. The capacitor is selected based on the RMS current and voltage requirements. The RMS current is given by:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

The RMS current reaches its maximum ($I_{OUT}/2$) when V_{IN} equals $2V_{OUT}$. This value should be increased by 50% to account for the ripple current increase due to the boost regulator. For an aluminum or ceramic capacitor, the voltage rating should be at least 25% higher than the maximum input voltage. If a tantalum capacitor is used, the voltage rating required is about twice the maximum input voltage. The tantalum capacitor should be surge current tested by the manufacturer to prevent being shorted by the inrush current. The minimum capacitor value should be 47µF for lower output load current applications and less dynamic (quickly changing) load conditions. For higher output current applications or dynamic load conditions a 68µF to 100µF low ESR capacitor is recommended. It is also recommended to put a small ceramic capacitor (0.1 µF) between the input pin and ground pin to reduce high frequency spikes.

INDUCTOR SELECTION

The most critical parameters for the inductor are the inductance, peak current and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input and the output voltages:

$$L = \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN} \times I_{RIPPLE} \times 300\ kHz}$$

A higher value of ripple current reduces inductance, but increases the conductance loss, core loss, current stress for the inductor and switch devices. It also requires a bigger output capacitor for the same output voltage ripple requirement. A reasonable value is setting the ripple current to be 30% of the DC output current. Since the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. The DC resistance of the inductor is a key parameter for the efficiency. Lower DC resistance is available with a bigger winding area. A good tradeoff between the efficiency and the core size is letting the inductor copper loss equal 2% of the output power.

OUTPUT CAPACITOR

The selection of C_{OUT} is driven by the maximum allowable output voltage ripple. The output ripple in the constant frequency, PWM mode is approximated by:

$$V_{RIPPLE} = I_{RIPPLE}\left(ESR + \frac{1}{8F_S C_{OUT}}\right)$$

The ESR term usually plays the dominant role in determining the voltage ripple. A low ESR aluminum electrolytic or tantalum capacitor (such as Nichicon PL series, Sanyo OS-CON, Sprague 593D, 594D, AVX TPS, and CDE polymer aluminum) is recommended. An electrolytic capacitor is not recommended for temperatures below –25˚C since its ESR rises dramatically at cold temperature. A tantalum capacitor has a much better ESR specification at cold temperature and is preferred for low temperature applications.

BOOT CAPACITOR

A 3.3 nF or larger ceramic capacitor is recommended for the bootstrap capacitor.

SOFT-START CAPACITOR (BOTH REGULATORS)

The SS pins are used to tailor the soft-start for a specific application. A current source charges the external soft-start capacitor, C_{SS}. The soft-start time can be estimated as:

$$T_{SS} = C_{SS}*0.6V/I_{SS}$$

Soft-start times may be implemented using the SS pin and a capacitor C_{SS}.

When programming the softstart time, simply use the equation given in the *Soft-Start Capacitor* section above. This equation uses the typical room temperature value of the soft start current to set the soft start time.

Buck Operation (Continued)

COMPENSATION COMPONENTS

In the control to output transfer function, the first pole F_{P1} can be estimated as $1/(2\pi R_{OUT}C_{OUT})$; The ESR zero F_{Z1} of the output capacitor is $1/(2\pi ESRC_{OUT})$; Also, there is a high frequency pole F_{P2} in the range of 45kHz to 150kHz:

$$F_{P2} = F_{SW}/(\pi n(1-D))$$

where $D = V_{OUT}/V_{IN}$, $n = 1+0.348L/(V_{IN}-V_{OUT})$ (L is in µHs and V_{IN} and V_{OUT} in volts).

The total loop gain G is approximately $500/I_{OUT}$ where I_{OUT} is in amperes.

A Gm amplifier is used inside the LM2716. The output resistor R_o of the Gm amplifier is about 85kΩ. C_{C1} and R_{C1} together with R_o give a lag compensation to roll off the gain:

$$F_{PC1} = 1/(2\pi C_{C1}(R_o+R_{C1})),\ F_{ZC1} = 1/2\pi C_{C1}R_{C1}.$$

In some applications, the ESR zero F_{Z1} can not be cancelled by F_{P2}. Then, C_{C3} is needed to introduce F_{PC2} to cancel the ESR zero, $F_{P2} = 1/(2\pi C_{C3}R_o \| R_{C1})$.

The rule of thumb is to have more than 45˚ phase margin at the crossover frequency (G=1).

SCHOTTKY DIODE

The breakdown voltage rating of D_1 is preferred to be 25% higher than the maximum input voltage. Since D1 is only on for a short period of time, the average current rating for D1 only requires being higher than 30% of the maximum output current.

Boost Operation

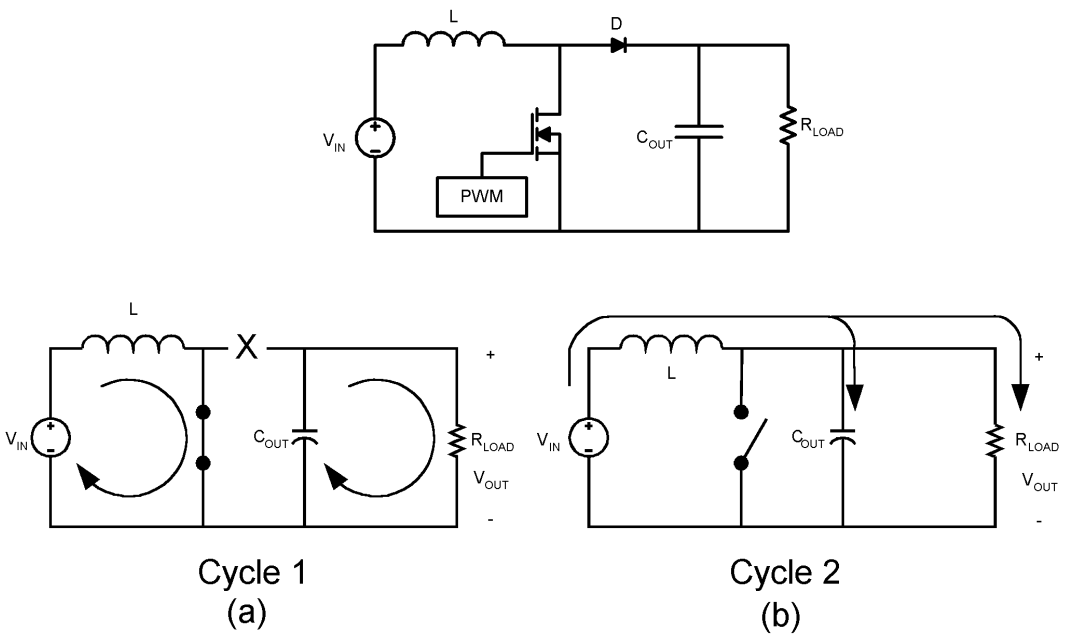

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FIGURE 1. Simplified Boost Converter Diagram
(a) First Cycle of Operation (b) Second Cycle Of Operation

CONTINUOUS CONDUCTION MODE

The LM2716 contains a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in *Figure 1* (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT}.

The second cycle is shown in *Figure 1* (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1-D},\ D' = (1-D) = \frac{V_{IN}}{V_{OUT}}$$

where D is the duty cycle of the switch, D and D' will be required for design calculations.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in *Figure 3*. The feedback pin voltage is 1.26V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 1.26}{1.26}\ \Omega$$

INTRODUCTION TO COMPENSATION

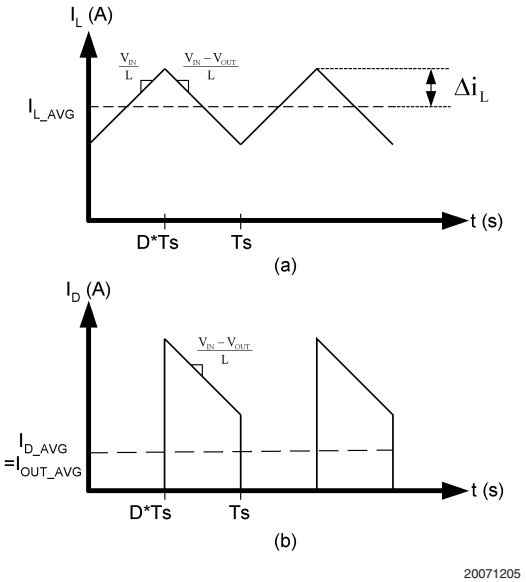

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FIGURE 2. (a) Inductor current. (b) Diode current.

Boost Operation (Continued)

The LM2716 has a current mode PWM boost converter. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see *Figure 2* (a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%. If the duty cycle is approaching near 85% up to the maximum of 95%, it may be necessary to increase the inductance by as much as 2X. See *Inductor and Diode Selection* for more detailed inductor sizing.

The LM2716 provides a compensation pin (V_{C2}) to customize the voltage loop feedback. It is recommended that a series combination of R_{C2} and C_{C2} be used for the compensation network, as shown in *Figure 3*. For any given application, there exists a unique combination of R_{C2} and C_{C2} that will optimize the performance of the LM2716 circuit in terms of its transient response. The series combination of R_{C2} and C_{C2} introduces a pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi R_{C2} C_{C2}} \text{ Hz}$$

$$f_{PC} = \frac{1}{2\pi (R_{C2} + R_O) C_{C2}} \text{ Hz}$$

where R_O is the output impedance of the error amplifier, approximately 850kΩ. For most applications, performance can be optimized by choosing values within the range 5kΩ ≤ R_{C2} ≤ 20kΩ (R_{C2} can be up to 200kΩ if C_{C4} is used, see *High Output Capacitor ESR Compensation*) and 680pF ≤ C_{C2} ≤ 4.7nF. Refer to the *Applications Information* section for recommended values for specific circuits and conditions. Refer to the *Compensation* section for other design requirement.

COMPENSATION

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation (loads greater than approximately 100mA), in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

INDUCTOR AND DIODE SELECTION

Although the inductor sizes mentioned earlier are fine for most applications, a more exact value can be calculated. To ensure stability at duty cycles above 50%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

$$L > \frac{V_{IN} R_{DSON}}{0.144\, F_{SW}} \left[\frac{\left(\frac{D}{D'}\right)^2 - 1}{\left(\frac{D}{D'}\right) + 1} \right] \text{ (in H)}$$

where F_{SW} is the switching frequency, D is the duty cycle, and R_{DSON} is the ON resistance of the internal switch taken from the graph "Boost Switch R_{DSON} vs. Input Voltage" in the *Typical Performance Characteristics* section. This equation is only good for duty cycles greater than 50% (D>0.5), for duty cycles less than 50% the recommended values may be used. The corresponding inductor current ripple as shown in *Figure 2* (a) is given by:

$$\Delta i_L = \frac{V_{IN} D}{2 L F_{SW}} \text{ (in Amps)}$$

The inductor ripple current is important for a few reasons. One reason is because the peak switch current will be the average inductor current (input current or I_{LOAD}/D') plus Δi_L. As a side note, discontinuous operation occurs when the inductor current falls to zero during a switching cycle, or Δi_L is greater than the average inductor current. Therefore, continuous conduction mode occurs when Δi_L is less than the average inductor current. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The typical current waveform for the diode in continuous conduction mode is shown in *Figure 2* (b). The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45˚) is desired for the best stability and transient response. For the purpose of stabilizing the LM2716, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin. A discussion of the right half plane zero and checking the crossover using the DC gain will follow.

OUTPUT CAPACITOR SELECTION

The choice of output capacitors is somewhat arbitrary and depends on the design requirements for output voltage ripple. It is recommended that low ESR (Equivalent Series

Boost Operation (Continued)

Resistance, denoted R_{ESR}) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the peak to peak output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \cong 2\Delta i_L R_{ESR} \text{ (in Volts)}$$

A minimum value of 10µF is recommended and may be increased to a larger value. After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi(R_{ESR} + R_L)C_{OUT}} \text{ (in Hz)}$$

$$f_{Z1} = \frac{1}{2\pi R_{ESR} C_{OUT}} \text{ (in Hz)}$$

Where R_L is the minimum load resistance corresponding to the maximum load current. The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the *High Output Capacitor ESR Compensation* section.

RIGHT HALF PLANE ZERO

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90˚ in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

$$\text{RHPzero} = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD} L} \text{ (in Hz)}$$

where I_{LOAD} is the maximum load current and D' corresponds to the minimum input voltage.

SELECTING THE COMPENSATION COMPONENTS

The first step in selecting the compensation components R_{C2} and C_{C2} is to set a dominant low frequency pole in the control loop. Simply choose values for R_{C2} and C_{C2} within the ranges given in the *Introduction to Compensation* section to set this pole in the area of 10Hz to 500Hz. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi(R_{C2} + R_O)C_{C2}} \text{(in Hz)}$$

where R_O is the output impedance of the error amplifier, approximately 850kΩ. Since R_{C2} is generally much less than R_O, it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero f_{ZC}. f_{ZC} is created to cancel out the pole created by the output capacitor, f_{P1}. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of f_{P1} over the expected loads and then set the zero f_{ZC} to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi C_{C2} R_{C2}} \text{(in Hz)}$$

Now R_{C2} can be chosen with the selected value for C_{C2}. Check to make sure that the pole f_{PC} is still in the 10Hz to 500Hz range, change each value slightly if needed to ensure both component values are in the recommended range. After checking the design at the end of this section, these values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance circuit. For improved transient response, higher values of R_{C2} should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimal performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

HIGH OUTPUT CAPACITOR ESR COMPENSATION

When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, C_{C4}, directly from the compensation pin V_{C2} to ground, in parallel with the series combination of R_{C2} and C_{C2}. The pole should be placed at the same frequency as f_{Z1}, the ESR zero. The equation for this pole follows:

$$f_{PC4} = \frac{1}{2\pi C_{C4}(R_{C2} || R_O)} \text{ (in Hz)}$$

To ensure this equation is valid, and that C_{C4} can be used without negatively impacting the effects of R_{C2} and C_{C2}, f_{PC4} must be greater than $10f_{ZC}$.

CHECKING THE DESIGN

The final step is to check the design. This is to ensure a bandwidth of ½ or less of the frequency of the RHP zero. This is done by calculating the open-loop DC gain, A_{DC}. After this value is known, you can calculate the crossover visually by placing a –20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than ½ the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved by adding C_{C4} as discussed earlier in the section. The equation for A_{DC} is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left\langle\left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right)\frac{g_m R_O D'}{R_{DSON}}\{[(\omega c \text{Leff}) // R_L] // R_L\}\right\rangle \text{ (in dB)}$$

$$\omega c \cong \frac{2F_{SW}}{nD'} \text{ (in rad/s)}$$

Boost Operation (Continued)

$$Leff = \frac{L}{(D')^2}$$

$$n = 1 + \frac{2mc}{m1} \text{ (no unit)}$$

$$mc \cong 0.072F_{SW} \text{ (in V/s)}$$

$$m1 \cong \frac{V_{IN}R_{DSON}}{L} \text{ (in V/s)}$$

where R_L is the minimum load resistance, V_{IN} is the minimum input voltage, g_m is the error amplifier transconductance found in the *Electrical Characteristics* table, and R_{DSON} is the value chosen from the graph "R_{DSON2} vs. V_{IN} " in the *Typical Performance Characteristics* section.

LAYOUT CONSIDERATIONS

The LM2716 uses two separate ground connections, PGND for the drivers and boost NMOS power device and AGND for the sensitive analog control circuitry. The AGND and PGND pins should be tied directly together at the package. The feedback and compensation networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the AGND pin. If no analog ground plane is available then the ground connections of the feedback and compensation networks must tie directly to the AGND pin. Connecting these networks to the PGND can inject noise into the system and effect performance.

The input bypass capacitor C_{IN}, as shown in *Figure 3*, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN}, close to the V_{IN} pin, to shunt any high frequency noise to ground. The output capacitors, C_{OUT1} and C_{OUT2}, should also be placed close to the IC. Any copper trace connections for the C_{OUTX} capacitors can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors R_{FB1} and R_{FB2}, should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. Trace connections made to the inductors and schottky diodes should be minimized to reduce power dissipation and increase overall efficiency. See *Figure 3*, *Figure 4*, and *Figure 5* for a good example of proper layout. For more detail on switching power supply layout considerations see Application Note AN-1149: *Layout Guidelines for Switching Power Supplies*.

Application Information

Some Recommended Inductors (others may be used)

Manufacturer	Inductor	Contact Information
Coilcraft	DO3316 and DO5022 series	www.coilcraft.com
Coiltronics	DRQ73 and CD1 series	www.cooperet.com
Pulse	P0751 and P0762 series	www.pulseeng.com
Sumida	CDRH8D28 and CDRH8D43 series	www.sumida.com

Some Recommended Input and Output Capacitors (others may be used)

Manufacturer	Capacitor	Contact Information
Vishay Sprague	293D, 592D, and 595D series tantalum	www.vishay.com
Taiyo Yuden	High capacitance MLCC ceramic	www.t-yuden.com
Cornell Dubilier	ESRD seriec Polymer Aluminum Electrolytic SPV and AFK series V-chip series	www.cde.com
Panasonic	High capacitance MLCC ceramic EEJ-L series tantalum	www.panasonic.com

Application Information (Continued)

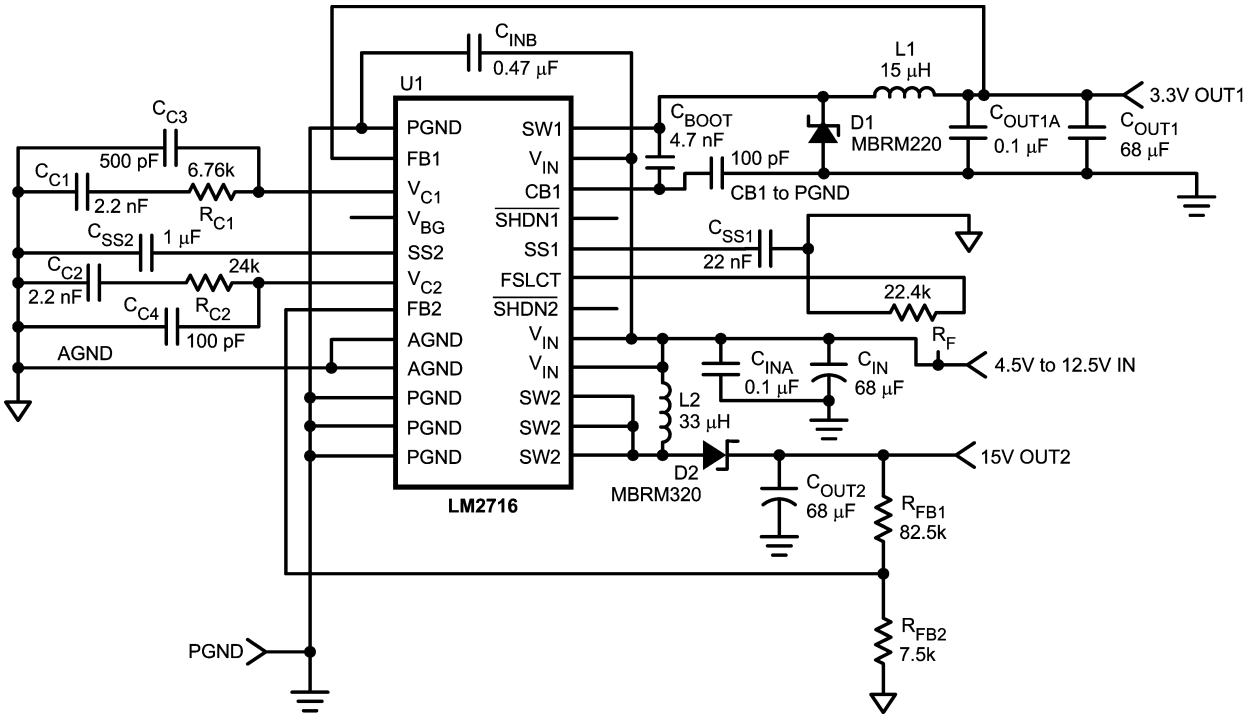

FIGURE 3. 15V, 3.3V Output Application

Application Information (Continued)

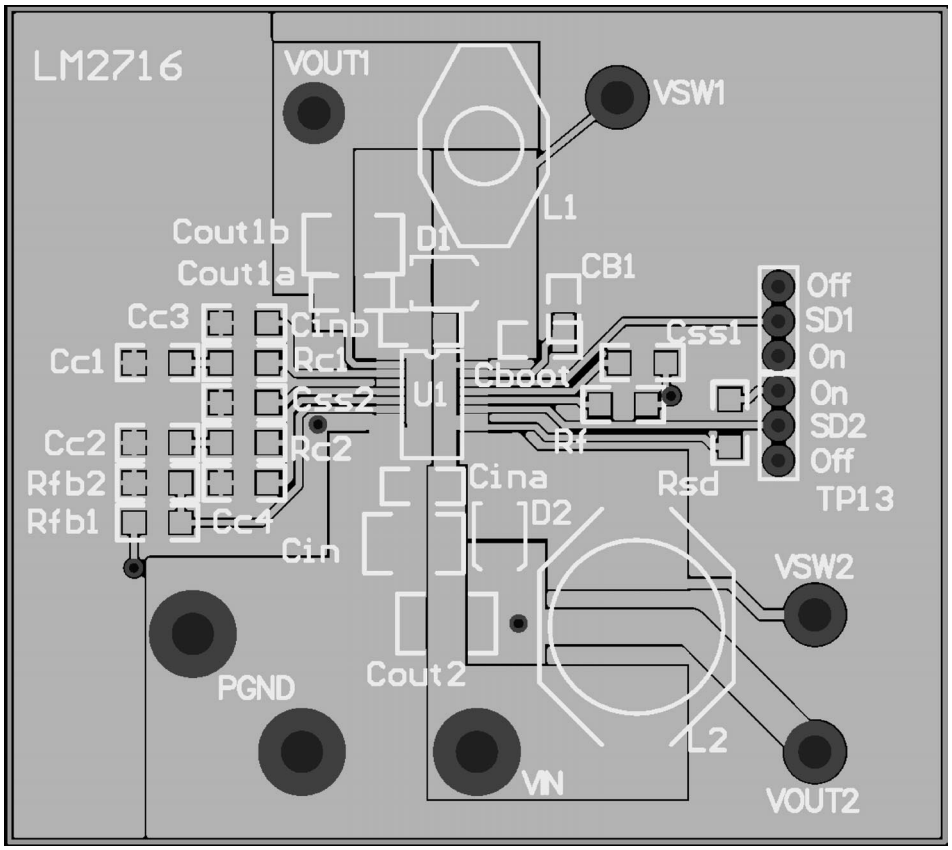

FIGURE 4. PCB Layout, Top

Application Information (Continued)

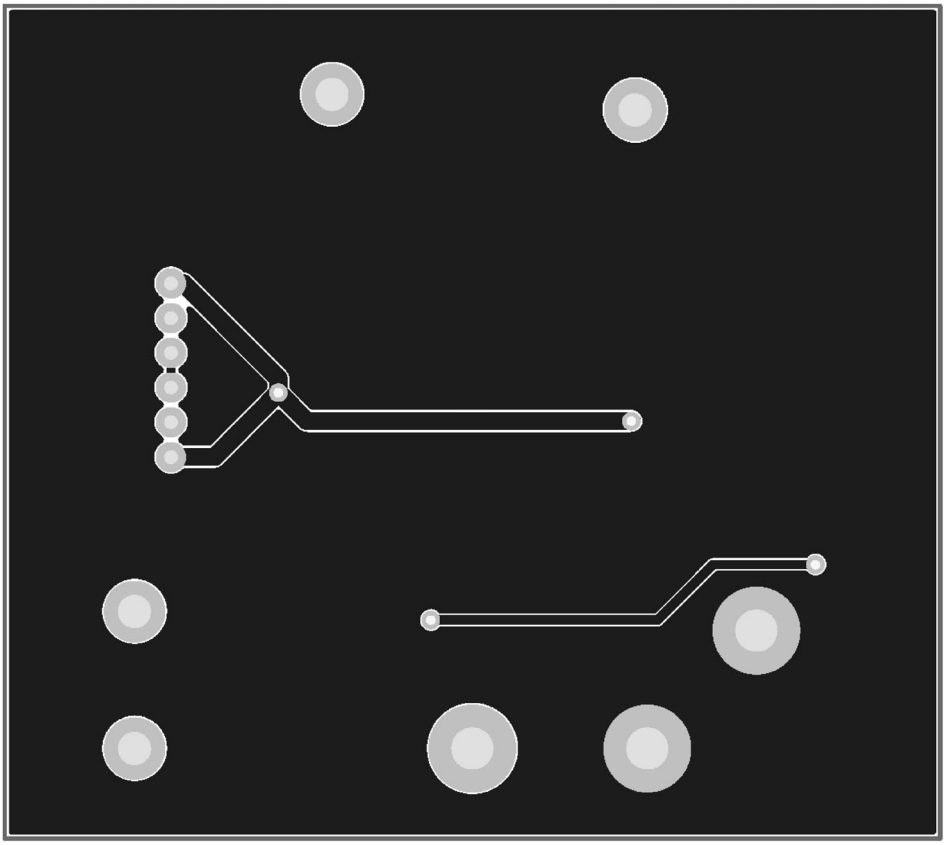

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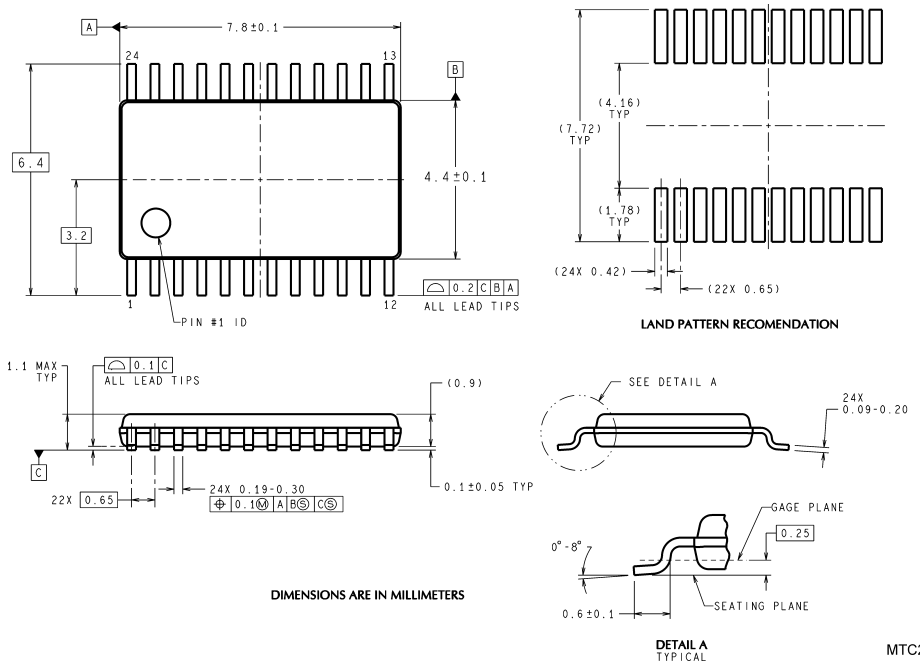
FIGURE 5. PCB Layout, Bottom

Physical Dimensions inches (millimeters) unless otherwise noted



MTC24 (Rev E)

TSSOP-24 Pin Package (MTC)
For Ordering, Refer to Ordering Information Table
NS Package Number MTC24

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