National Semiconductor

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LM2502
Mobile Pixel Link (MPL) Display Interface Serializer and Deserializer

General Description

The LM2502 device is a dual link display interface SERDES that adapts existing CPU / video busses to a low power current-mode serial MPL link. The chipset may also be used for a RGB565 application with glue logic. The interconnect is reduced from 22 signals to only 3 active signals with the LM2502 chipset easing flex interconnect design, size and cost.

The Master Serializer (SER) resides beside an application processor or baseband processor and translates a parallel bus from LVCMOS levels to serial MPL levels for transmission over a flex cable and PCB traces to the Slave Deserializer (DES) located near the display module.

Dual display support is provided for a primary and sub display through the use of two ChipSelect signals. A Mode pin selects either a i80 or m68 style interface.

The Power_Down (PD*) input controls the power state of the MPL interface. When PD* is asserted, the MD1/0 and MC signals are powered down to save current.

The LM2502 implements the physical layer of the MPL Standard (MPL-0). The LM2502 is offered in NOPB (Lead-free) UFBGA and LLP packages.

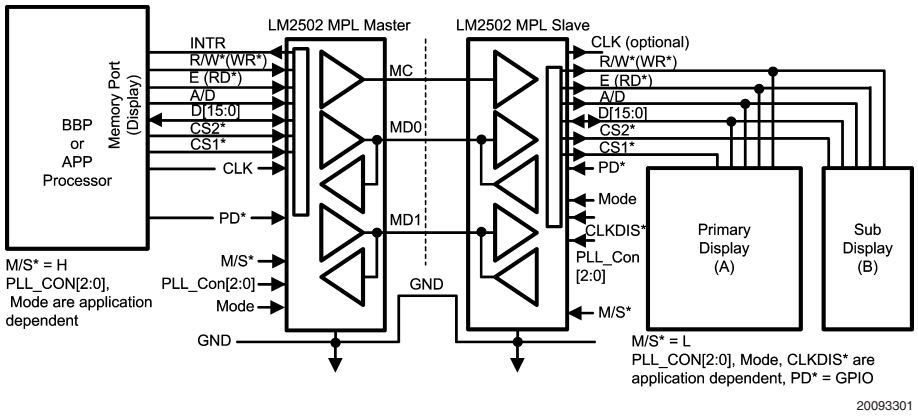
Features

- >300 Mbps Dual Link Raw Throughput
- MPL Physical Layer (MPL-0)
- Pin selectable Master / Slave mode
- Frequency Reference Transport
- Complete LVCMOS / MPL Translation
- Interface Modes:
  — 16-bit CPU, i80 or m68 style
  — RGB565 with glue logic
- –30˚C to 85˚C Operating Range
- Link power down mode reduces I_{DDZ} < 10 µA
- Dual Display Support (CS1* & CS2*)
- Via-less MPL interconnect feature
- 3.0V Supply Voltage (V_{DD} and V_{DDA})
- Interfaces to 1.7V to 3.3V Logic (V_{DDIO})

System Benefits

- Small Interface
- Low Power
- Low EMI
- Frequency Reference Transport
- Intrinsic Level Translation

Typical Application Diagram



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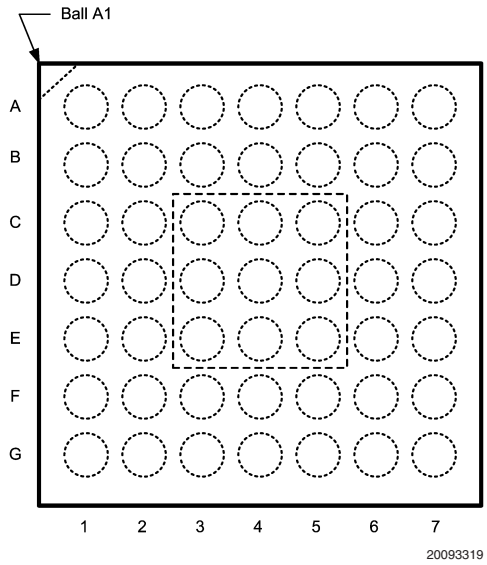
Ordering Information

NSID	Package Type	Package ID
LM2502SM	49 Lead UFBGA style, 4.0 X 4.0 X 1.0 mm, 0.5 mm pitch 1000 std reel, LM2502SMX 4500 reel	SLH49A
LM2502SQ	40 Lead LLP style, 5.0 X 5.0 X 0.8 mm, 0.4 mm pitch 1000 std reel, LM2502SQX 4500 reel	SQF40A

UFBGA Connection Diagram



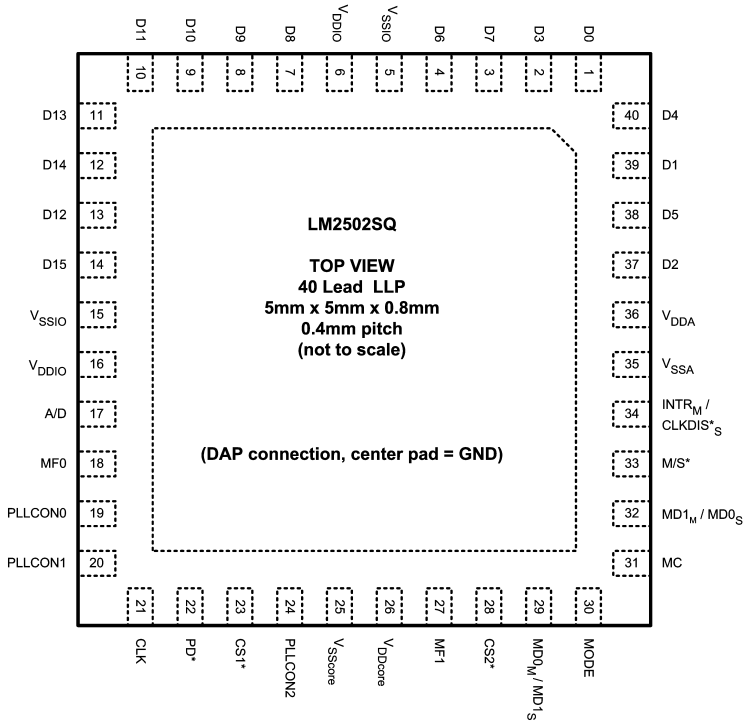
TOP VIEW
(not to scale)

TABLE 1. Ball Assignment

Ball #	Master	Slave		Ball #	Master	Slave
A1	D0	D0		D5	NC	NC
A2	D1	D1		D6	V_{SScore}	V_{SScore}
A3	D2	D2		D7	V_{DDcore}	V_{DDcore}
A4	V_{DDA}	V_{DDA}		E1	D8	D8
A5	**INTR**	**CLKDIS***		E2	D9	D9
A6	**MD1**	**MD0**		E3	NC	NC
A7	MC	MC		E4	NC	NC
B1	D3	D3		E5	NC	NC
B2	D4	D4		E6	CS1*	CS1*
B3	D5	D5		E7	PLLCON2	PLLCON2
B4	V_{SSA}	V_{SSA}		F1	D10	D10
B5	M/S*	M/S*		F2	D11	D11
B6	Mode	Mode		F3	D12	D12
B7	**MD0**	**MD1**		F4	V_{SSIO}	V_{SSIO}
C1	D6	D6		F5	MF0	MF0
C2	D7	D7		F6	PLLCON1	PLLCON1
C3	NC	NC		F7	PD*	PD*
C4	NC	NC		G1	D13	D13
C5	NC	NC		G2	D14	D14
C6	CS2*	CS2*		G3	D15	D15
C7	MF1	MF1		G4	V_{DDIO}	V_{DDIO}
D1	V_{DDIO}	V_{DDIO}		G5	A/D	A/D
D2	V_{SSIO}	V_{SSIO}		G6	PLLCON0	PLLCON0
D3	NC	NC		G7	CLK	CLK
D4	NC	NC		NC = Not Connected		

Note: Three pins are different between Master and Slave configurations - see also *Figure 17*

LLP Connection Diagram



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TOP VIEW
(not to scale)

TABLE 2. Pad Assignment

Pin #	Master	Slave		Ball #	Master	Slave
1	D0	D0		21	CLK	CLK
2	D3	D3		22	PD*	PD*
3	D7	D7		23	CS1*	CS1*
4	D6	D6		24	PLLCON2	PLLCON2
5	V_{SSIO}	V_{SSIO}		25	V_{SScore}	V_{SScore}
6	V_{DDIO}	V_{DDIO}		26	V_{DDcore}	V_{DDcore}
7	D8	D8		27	MF1	MF1
8	D9	D9		28	CS2*	CS2*
9	D10	D10		29	**$MD0_M$**	**$MD1_S$**
10	D11	D11		30	MODE	MODE
11	D13	D13		31	MC	MC
12	D14	D14		32	**$MD1_M$**	**$MD0_S$**
13	D12	D12		33	M/S*	M/S*
14	D15	D15		34	**$INTR_M$**	**$CLKDIS*_S$**
15	V_{SSIO}	V_{SSIO}		35	V_{SSA}	V_{SSA}
16	V_{DDIO}	V_{DDIO}		36	V_{DDA}	V_{DDA}
17	A/D	A/D		37	D2	D2
18	MF0	MF0		38	D5	D5
19	PLLCON0	PLLCON0		39	D1	D1
20	PLLCON1	PLLCON1		40	D4	D4
DAP	GND	GND		DAP	GND	GND

Note: Three pins are different between Master and Slave configurations.

Pin Descriptions

Pin Name	No. of Pins	I/O, Type	Description	
			Master (SER)	Slave (DES)
MPL SERIAL BUS PINS				
MD[1:0]	2	IO, MPL	MPL Data Line Driver/Receiver	MPL Data Receiver/Line Driver
MC	1	IO, MPL	MPL Clock Line Driver	MPL Clock Receiver
V_{SSA}		Ground	MPL Ground - see Power/Ground Pins	MPL Ground - see Power/Ground Pins
CONFIGURATION/PARALLEL BUS PINS				
M/S*	1	I, LVCMOS	Master/Slave* Input, M/S* = H for Master	Master/Slave* Input M/S* = L for Slave
PD*	1	I, LVCMOS	Power_Down* Input, H = Active L = Power Down Mode	Power_Down* Input, H = Active L = Power Down Mode
MF0 (E or RD*)	1	IO, LVCMOS	Multi-function Input Zero (0): If MODE = L (m68 mode), E input pin, data is latched on E High-to-Low transition or E may be static High and Data is latched on CS* Low-to-High edge If MODE = H (i80 mode), Read Enable input pin, active low. Read data is driven when both RD* and CS* are Low.	Multi-function Output Zero (0): If MODE = L (m68 mode), E output pin, static High. If MODE = H (i80 mode), Read Enable output pin, active Low.
MF1 (R/W* or WR*)	1	IO, LVCMOS	Multi-function Input One (1): If Mode = L (m68 mode), Read/Write* pin, Read High, Write* Low If Mode = H (i80 mode), Write* enable input pin, active Low. Write data is latched on the Low-to-High transition of either WR* or CS* (which ever occurs first).	Multi-function Output One (1): If Mode = L (m68 mode) Read/Write* pin, Read High, Write* Low If Mode = H (i80 mode) Write* enable output pin, active Low.
CS1*	1	IO, LVCMOS	ChipSelect1* – Input H = Ignored L = Active	ChipSelect1* – Output H = Ignored L = Active
CS2*	1	IO, LVCMOS	ChipSelect2* – Input H = Ignored L = Active	ChipSelect2* – Output H = Ignored L = Active
A/D (RS or A0)	1	IO, LVCMOS	Address/Data – Input H = Data L = Address (Command)	Address/Data – Output H = Data L = Address (Command)
D[15:0]	16	IO, LVCMOS	Data Bus – Inputs/Outputs	Data Bus – Outputs/Inputs
INTR or CLKDIS*	1	O or I, LVCMOS	INTR is asserted when the read data is ready and de-asserted upon a second CPU Read cycle.	Clock Disable - CLKDIS*: H = CLK output ON L = CLK output LOW, allows for the Slave clock output to be held static if not used.
CLK	1	IO, LVCMOS	Clock Input	Clock Output (Frequency Reference) – no phase relationship to data – frequency reference only.
Mode	1	I, LVCMOS	Mode Input Pin H = i80 Mode, L = m68 Mode	Mode Input Pin H = i80 Mode, L = m68 Mode
PLL_CON [2:0]	3	I, LVCMOS	PLL Configuration Input Pins – see *Table 10*	Clock Divisor Configuration Input Pins – see *Table 10*

Pin Descriptions (Continued)

Pin Name	No. of Pins	I/O, Type	Description	
			Master (SER)	Slave (DES)
POWER/GROUND PINS				
V_{DDA}	1	Power	Power Supply Pin for the MPL Interface. 2.9V to 3.3V	
V_{SSA}	1	Ground	Ground Pin for the MPL Interface, a low impedance ground path is required between the Master and the Slave device - see Applications Information section.	
V_{DDcore}	1	Power	Power Supply Pin for the digital core. 2.9V to 3.3V	
V_{SScore}	1	Ground	Ground Pin for the digital core.	
V_{DDIO}	2	Power	Power Supply Pin for the parallel interface. 1.7V to 3.3V	
V_{SSIO}	2	Ground	Ground Pin for the parallel interface.	
	9	NC	Not Connected (C3-5, D3-5, E3-5). **UFBGA Package only.**	
	1	Ground	DAP = Ground. **LLP Package only.**	

Note:
I = Input, O = Output, IO = Input/Output, $V_{DDIO} \leq V_{DD}$ ($V_{DDA} = V_{DDcore}$). Do not float input pins.

Master Pinout - UFBGA Package

MST	1	2	3	4	5	6	7
A	D0	D1	D2	V_{DDA}	INTR	MD1	MC
B	D3	D4	D5	V_{SSA}	M/S*	Mode	MD0
C	D6	D7	NC	NC	NC	CS2*	MF1
D	V_{DDIO}	V_{SSIO}	NC	NC	NC	V_{SScore}	V_{DDcore}
E	D8	D9	NC	NC	NC	CS1*	PLLCON2
F	D10	D11	D12	V_{SSIO}	MF0	PLLCON1	PD*
G	D13	D14	D15	V_{DDIO}	A/D	PLLCON0	CLK

Slave Pinout - UFBGA Package

SLV	1	2	3	4	5	6	7
A	D0	D1	D2	V_{DDA}	CLKDIS*	MD0	MC
B	D3	D4	D5	V_{SSA}	M/S*	Mode	MD1
C	D6	D7	NC	NC	NC	CS2*	MF1
D	V_{DDIO}	V_{SSIO}	NC	NC	NC	V_{SScore}	V_{DDcore}
E	D8	D9	NC	NC	NC	CS1*	PLLCON2
F	D10	D11	D12	V_{SSIO}	MF0	PLLCON1	PD*
G	D13	D14	D15	V_{DDIO}	A/D	PLLCON0	CLK

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DDA})	−0.3V to +4.0V
Supply Voltage (V_{DD})	−0.3V to +4.0V
Supply Voltage (V_{DDIO})	−0.3V to +4.0V
LVCMOS Input/Output Voltage	−0.3V to (V_{DDIO} +0.3V)
MPL Input/Output Voltage	−0.3V to (V_{DDA} +0.3V)
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature Soldering, 40 Seconds	+260˚C
ESD Ratings:	
HBM, 1.5 kΩ, 100pF	≥±2 kV
EIAJ, 0Ω, 200 pF	≥±200V
Maximum Package Power Dissipation Capacity at 25˚C	
UFBGA Package (Note 4)	2.5 W
Derate UFBGA Package above 25˚C	25 mW/˚C
Theta JA	45˚C/W
LLP Package (Note 4)	1.39 W
Derate LLP Package above 25˚C	11 mW/˚C
Theta JA	90˚C/W

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DDA} to V_{SSA} and V_{DDcore} to V_{SScore}	2.9	3.0	3.3	V
V_{DDIO} to V_{SSIO}	1.7		3.3	V
Clock Frequency	3.0		26	MHz
Ambient Temperature	−30	25	85	˚C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
MPL							
I_{OLL}	Logic Low Current (5X I_B)			3.67 I_B	5.0 I_B	6.33 I_B	µA
I_{OMS}	Mid Scale Current				3.0 I_B		µA
I_{OLH}	Logic High Current (1X I_B)			0.7 I_B	1.0 I_B	1.3 I_B	µA
I_B	Current Bias				150		µA
I_{OFF}	MPL Leakage Current	PD* = L (PowerDown mode)		−2	0	+2	µA
LVCMOS (1.7V to 3.3V Operation)							
V_{IH}	Input Voltage High Level	V_{DDIO} = 2.0V to 3.3V		0.7 V_{DDIO}		V_{DDIO} +0.3	V
		V_{DDIO} = 1.7V to <2.0V		0.8 V_{DDIO}			
V_{IL}	Input Voltage Low Level	V_{DDIO} = 2.0V to 3.3V		−0.3		0.3 V_{DDIO}	V
		V_{DDIO} = 1.7V to <2.0V		−0.3		0.2 V_{DDIO}	V
V_{HY}	Input Hysteresis	V_{DDIO} = 3.0V			500		mV
		V_{DDIO} = 1.8V			300		mV
I_{IN}	Input Current (includes I_{OZ})	LVCMOS IO Signals		−2	0	+2	µA
I_{IH}	Input Current High Level	LVCMOS Input Only Signals (i.e. Mode)		−1	0	+1	µA
I_{IL}	Input Current Low Level			−1	0	+1	µA
V_{OH}	Output Voltage High Level	I_{OH} = −2 mA	V_{DDIO} = 3.3V	0.8 V_{DDIO}	2.8		V
			V_{DDIO} = 1.7V		1.6		
V_{OL}	Output Voltage Low Level	I_{OL} = 2 mA	V_{DDIO} = 3.3V		0.08	0.2 V_{DDIO}	V
			V_{DDIO} = 1.7V		0.12		
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{DDIO} = 1.7 V			−5		mA
		V_{OUT} = 0V, V_{DDIO} = 3.3 V			−30		mA

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
SUPPLY CURRENT							
I_{DD}	Total Supply Current — Enabled Conditions: MC = 76.8 MHz, MD = 1010-0101 pattern (worse case toggle, rail-to-rail levels), CLK = 19.2 MHz (4X) (Note 7)	Master	V_{DDIO}		15	220	µA
			$V_{DD} = V_{DDA}$		14	25	mA
		Slave, C_L = 10 pF	V_{DDIO}		1.5	9.0	mA
			$V_{DD} = V_{DDA}$		9.0	13.0	mA
	Total Supply Current — Enabled Conditions: MC = 20 MHz, MD = 1010-0101 pattern (worse case toggle, rail-to-rail levels), CLK = 5 MHz (4X)	Master	V_{DDIO} = 1.8V		10		µA
			$V_{DD} = V_{DDA}$ = 3V		5		mA
		Slave, C_L = 10 pF	V_{DDIO} = 1.8V		1		mA
			$V_{DD} = V_{DDA}$ = 3V		4		mA
I_{DDZ}	Supply Current — Disabled	Power_Down Mode, PD* = 0V			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PARALLEL BUS TIMING							
t_{SET}	Set Up Time, Data to Edge	Inputs		5			ns
t_{HOLD}	Hold Time, Edge to Data			5			ns
t_{RISE}	Rise Time	*Figure 2*, Outputs, C_L = 10 pF Edge sensitive outputs tested only: m68 mode: CS1*, CS2* and CLKout i80 mode: RD*, WR*, and CLKout	V_{DDIO} = 1.7V	2	7	14	ns
			V_{DDIO} = 3.3V	1	2	10	ns
t_{FALL}	Fall Time		V_{DDIO} = 1.7V	2	6	14	ns
			V_{DDIO} = 3.3V	1	2	10	ns
CLK_{DC}	Output Clock Duty Cycle	CLKDIS* = H, Slave (DES)			50		%
Parallel Bus Timing - See *Figures 13, 14, 15, 16* and *Table 5*, *Table 6*, *Table 7*, and *Table 8*							
SERIAL BUS TIMING							
t_{DVBC}	Data Valid before Clock	Master-to-Slave (Note 5)		2.0			ns
t_{DVAC}	Data Valid after Clock			0.5			ns
POWER UP TIMING(Note 5)							
t_0	Master PLL Lock Counter		*Figure 6*		4096		CLK cycles
t_1	MC Pulse Width Low (Master)				11		CLK cycles
t_2	MC Pulse Width HIGH (Master)				11		CLK cycles
t_3	MC Pulse Width Low (Master)				11		CLK cycles
t_4	CLK-Out Delay (Slave)				7		MC cycles
t_5	Power Up Total delay ($t_0 + t_1 + t_2 + t_3 + t_4$)				4133		CLK cycles

Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER UP TIMING(Note 5)						
MPL POWER OFF TIMING						
t_{PAZ}	Disable Time to Power Down	*Figure 7*, This parameter is functionally tested by the I_{DDZ} parameter. (Note 6)			50	ms

Recommended Input Timing Requirements

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER REFERENCE CLOCK (CLK)						
f_{CLK}	Clock Frequency	See *Table 10* (Note 5)	3		26	MHz
t_{CP}	Clock Period		38.5		333	ns
CLK_{DC}	Clock Duty Cycle		40	50	60	%
t_T	Clock Transition Times (Rise or Fall, 20%–80%)		1		14	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for VDDIO = 1.8V and VDD = VDDA = 3.0V and $T_A = 25^{\circ}C$.

Note 3: Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

Note 4: UFBGA assumes 4 layer PCB, LLP assumes 2 layer PCB for thermal calculations.

Note 5: This parameter is Guaranteed by Design (GBD) based on simulation or bench characterization.

Note 6: This parameter is guaranteed by a ATE tester delay, actual turn off time is faster.

Note 7: Typical supply condition is V_{DDIO} = 1.8V and $V_{DD} = V_{DDA}$ = 3.0V, Maximum supply condition is $V_{DDIO} = V_{DD} = V_{DDA}$ = 3.3V for the I_{DD} parameter.

Timing Diagrams

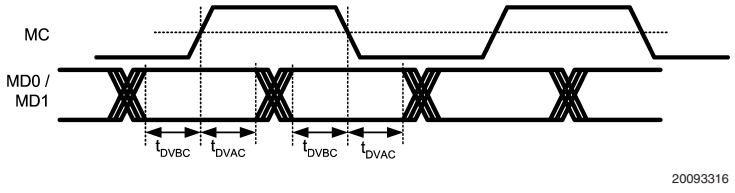


FIGURE 1. Serial Data Valid — Master to Slave

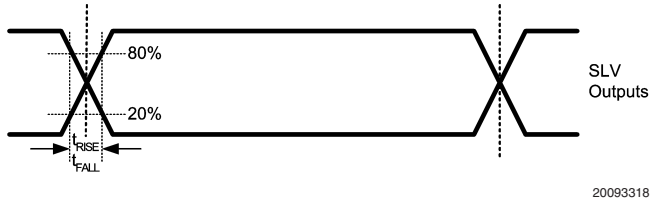


FIGURE 2. Slave Output Rise and Fall Time

Functional Description

BUS OVERVIEW

The LM2502 is a dual link Transceiver configurable part that supports a 16-bit CPU (m68 or i80) style interface. The MPL physical layer is purpose-built for an extremely low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the MPL receiver. A maximum raw throughput of 307 Mbps (raw) is possible with this chipset. When the protocol overhead is taken into account, a maximum data throughput of 245 Mbps is possible. The MPL interface is designed for use with common 50Ω to 100Ω lines using standard materials and connectors. Lines may be microstrip or stripline construction. Total length of the interconnect is expected to be less than 20cm.

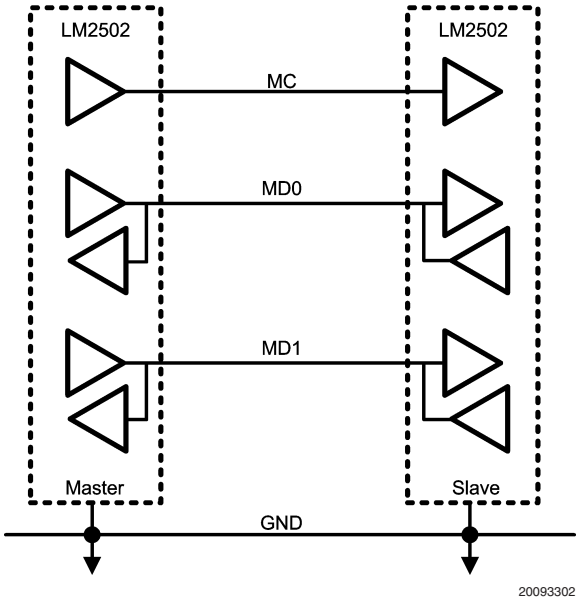


FIGURE 3. MPL Point-to-Point Bus

SERIAL BUS TIMING

Data valid is relative to both edges for a WRITE as shown in *Figure 4*. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, and Skew between data lines should be less than 500ps.

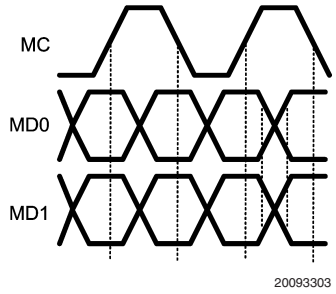


FIGURE 4. Dual Link Timing (WRITE)

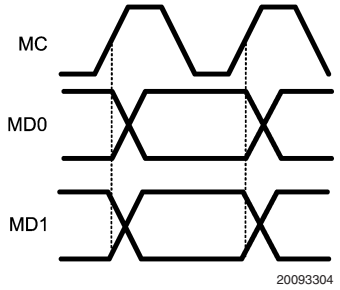


FIGURE 5. Dual Link Timing (READ)

Data is strobed out on the rising edge by the Slave for a READ as shown in *Figure 5*. The Master monitors for the start bit transition (Low to High) and selects the best strobe to sample the incoming data on. This is done to account for the round trip delay of the interconnect and application data rate.

Functional Description (Continued)

SERIAL BUS PHASES

There are four bus phases on the MPL serial bus. These are determined by the state of the MC and MD lines. The MPL bus phases are shown in *Table 3*.

TABLE 3. Link Phases

Name		MC State	MDn State	Phase Description	Pre-Phase	Post-Phase
OFF (O)		0	0	Link is Off	A, I or LU	LU
IDLE (I)		A	L	Data is Static (Low)	A or LU	A or O
Active (A)	Data Out WRITE	A	X	Data Out (Write) — includes command, Data Out Phases	LU, A, or I	A, I, or O
	Data In READ	A	X	Data In (Read) — includes command, TA', Data In, and TA" phases	LU, A, or I	A, I, or O
LINK-UP (LU)	Master	H	-	Master initiated Link-Up	O	A, I, or O

Notes on MC/MD Line State:
0 = no current (off)
L = Logic Low — The higher level of current on the MC and MD lines
H = Logic High — The lower level of current on the MC and MD lines
X = Low or High
A = Active Clock

SERIAL BUS START UP TIMING

In the Serial Bus OFF phase, Master transmitters for MD0, MD1 and MC are turned off such that zero current flows over the MPL lines. In addition, both the Master and the Slave are internally held in a low power state. When the PD* input pins are de-asserted (driven High) the Master enables its PLL and waits for enough time to pass for its PLL to lock. After the Master's PLL is locked (t0 = 4,096 CLK Cycles), the Master will perform an MPL start up sequence. The Slave will also power up and await the start up sequence from the Master.

The MPL start up sequence gives the Slave an opportunity to optimize the current sources in its transceiver to maximize noise margins. The Master begins the sequence by driving the MC line logically Low for 11 CLK cycles (t1). During this part of the sequence the Slave's transceiver samples the MC current flow and adjusts itself to interpret that amount of current as a logical Low. Next the Master drives the MC line logically HIGH for 11 CLK cycles (t2). On the Low-to-High transition of the MC – point B – the Slave latches the current source configuration. This optimized configuration is held as long as the MPL remains up. Next, the Master drives both the MC and the MD lines to a logical Low for another 11 CLK cycles (t3), after which it begins to toggle the MC line at a rate determined by its PLL Configuration pins. The Master will continue to toggle the MC line as long as its PD* pin remains de-asserted (High). At this point the MPL bus may remain in IDLE phase, enter the ACTIVE phase or return to the OFF phase. Active data will occur at the Slave output latency delays (Master + line + Slave) after the data is applied to the Master input. Possible start points are shown by the "C" arrow in *Figure 6*.

After seven subsequent MC cycles the Slave will start toggling its CLK pin at a rate configured by its CLK Divisor pins.

In the *Figure 6* example, an IDLE bus phase is shown until point C, after which the bus is active and the High start bit on MD initiates the transfer of information.

Functional Description (Continued)

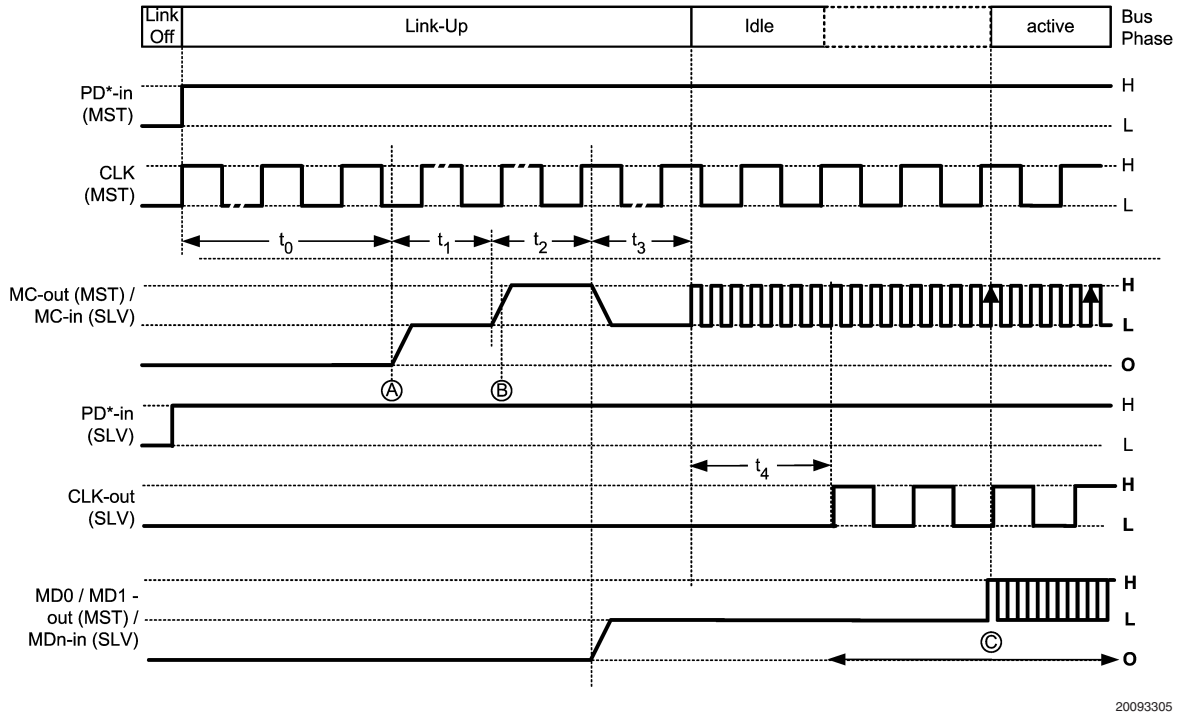


FIGURE 6. MPL Power Up Timing

OFF PHASE

In the OFF phase, both Master and Slave MPL transmitters are turned off with zero current flowing on the MC and MD lines. *Figure 7* shows the transition of the MPL bus into the OFF phase. If an MPL line is driven to a logical Low (high current) when the OFF phase is entered it may temporarily pass through as a logical High (low current) before reaching the zero line current state.

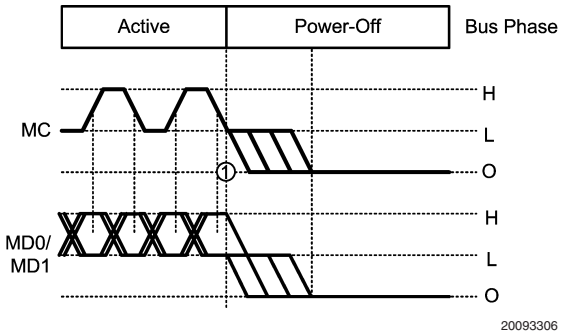


FIGURE 7. MPL Power Down Timing

The link may be powered down by asserting both the Master's and Slaves's PD* input pins (Low). This causes the devices to immediately put the link to the OFF Phase and internally enter a low power state. To avoid loss of data the Master's PD* input should only be asserted after the MPL bus has been in the IDLE state for at least 20 MC clock cycles. This gives the Slave enough time to complete any write operations received from the MPL bus.

CPU INTERFACE COMPATIBILITY

The CPU Interface mode provides compatibility between a CPU Interface and a small form factor (SFF) Display or other fixed I/O port application. Two options are allowed:

TABLE 4. Modes

Mode	Description
0	m68 Interface (E, R/W*), 16-bit support
1	i80 Interface (WR*, RD*), 16-bit support

It is not required that both the Master and the Slave to be configured in the same mode. For example the Master may be configured as an 80xx (i80) interface while the Slave is configured for an 68xx (m68) interface.

Control information is carried over both MD lines. MD0 carries the D0–7 data bits while MD1 the D8–15 data bits. See *Figure 8*.

Functional Description (Continued)

WRITE TRANSACTION

The WRITE transaction consists of two MC edges of control information followed by 8 MC edges of write data. Since WRITE transactions transfer information on both edges of MC it takes 5 MC cycles to complete a write transaction. The MD0 line carries the Start bit (High), the A/D (Address/Data) bit and then the data payload of 8 bits (D0–7). The MD1 line carries the R/W* bit (Read/Write*), the CS1/2 bit and then the data payload of 8 bits (D8–15). The data payload is sent least significant bit (LSB) first. The CS1/2 bit denotes which Chipset pin was active. CS1/2 = HIGH designates that CS1* is active (Low). CS1/2 = LOW designates that CS2* is active (Low). CS1* and CS2* LOW is not allowed.

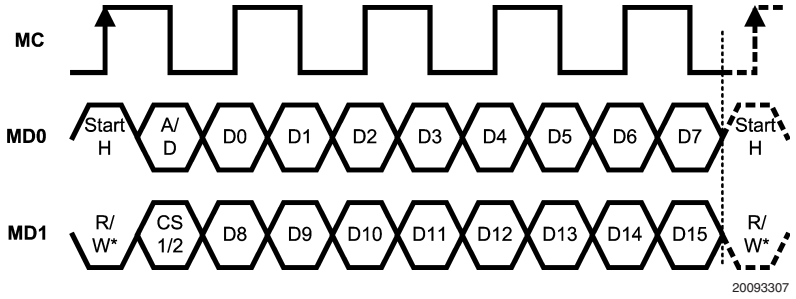


FIGURE 8. Dual MD Link WRITE Transaction

READ TRANSACTION

The READ transaction is variable in length. It consists of four sections.

In the first section the Master sends a READ_Command to the slave. This command is sent in a single MC cycle (2 edges) and uses a similar format to the 1st cycle of the WRITE transaction. The MD0 line carries the Start bit (High) and the A/D (Address/Data) bit. The MD1 line carries the R/W* bit (High for reads) and the CS1/2 bit.

In the second section (TA') the MD lines are turned around, such that the Master becomes the receiver and Slave becomes the transmitter. The Slave must drive the MD lines low by the 14th clock edge. It may then idle the line at the Logic Low state or drive the line High to indicate that read data transmission is starting. This ensures that the MD lines are a stable LOW state and that the Low-to-High transition of the "Start" bit is seen by the Master.

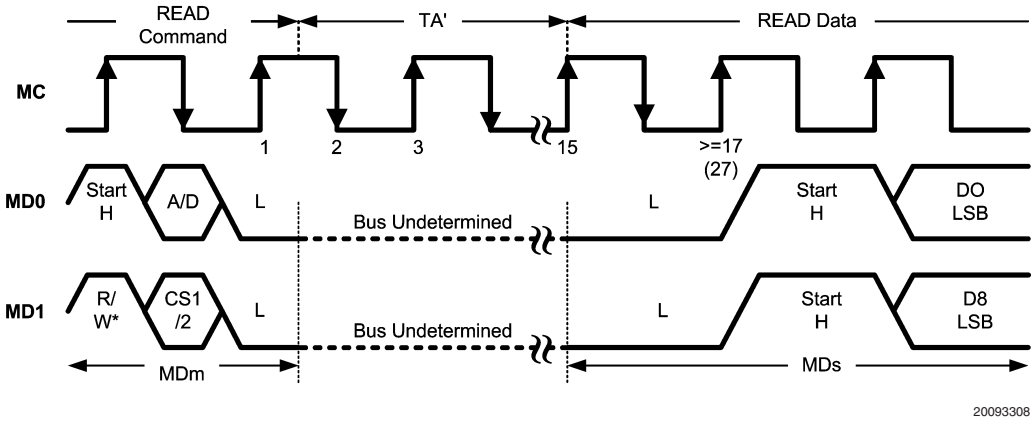


FIGURE 9. READ_Command and TA'

The third section consists of the transfer of the read data from the Slave to the Master. Note that the READ_Data operates on single-edge strobing (Rising Edge ONLY). Therefore the back channel data signaling rate is ½ of the forward channel (Master-to-Slave direction). When the Slave is ready to transmit data back to the Master it drives the MD lines High to indicate start of read data, followed by 8 MC cycles of the actual read data payload. As in the WRITE command MD0 carries D0–7 and MD1 carries D8–5. The Master monitors for the start bit transition (Low to High) and selects the best strobe to sample the incoming data on. This is done to account for the round trip delay of the interconnect and application data rate.

The Master detects the location of the START bit on MD0 and selects the best strobe for data capture. Skew between the data lines is constrained tighter in the Master-to-Slave direction (Write) than in the Read direction due to the data rate difference. The Master uses its internal clock (multiple phases) to latch the data.

The fourth and final section (TA") occurs after the read data has been transferred from the Slave to the Master. In the

Functional Description (Continued)

fourth section the MD lines are again turned around, such that the Master becomes the transmitter and the Slave becomes the receiver. The Slave drives the MD lines Low for 1 bit width and then turns off. The MD lines are off momentarily to avoid driver contention. The Master then drives the MD line Low for 1 bit time and then idles the bus until the next transaction is sent.

During a READ transaction (Double Read access on the Master), other MPL transactions are not allowed until the current READ dual cycle is completed.

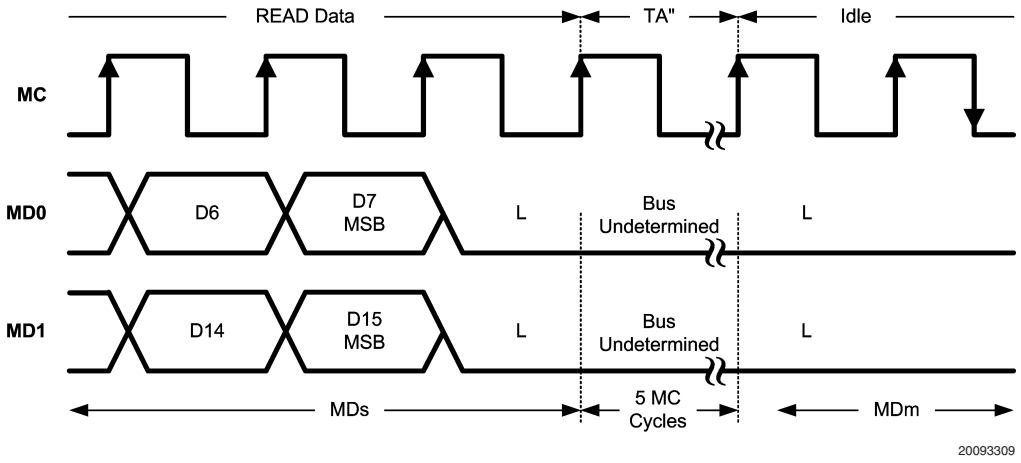


FIGURE 10. READ_Data and TA"

To account for the latency through the MPL link, a dual READ operation is required by the host. The first read returns invalid data (all Low). Once data has returned to the Master LM2502, the INTR signal is asserted to inform the host to initiate a second read operation. When the Master LM2502 sees the Read signal/CS* combination, it will deassert the INTR signal and Valid data is presented.

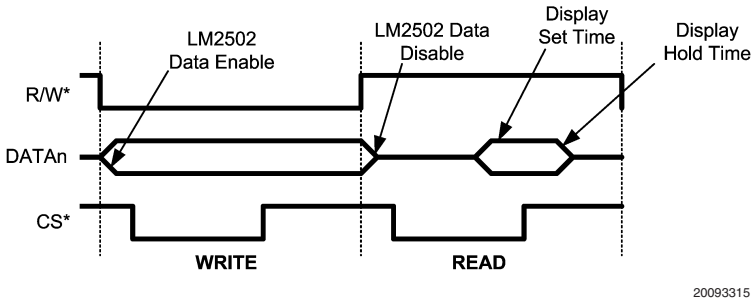


FIGURE 11. Slave WRITE and Slave READ m68 mode Operation

Figure 11 illustrates a m68 mode WRITE followed by a READ operation (Slave output to Display). At the end of the WRITE operation the SLAVE outputs are turned off. The SLAVE latches in the READ data on the rising edge of the CS* signal as shown. The Display should disable its outputs prior to the next operation to avoid any bus contention.

Functional Description (Continued)

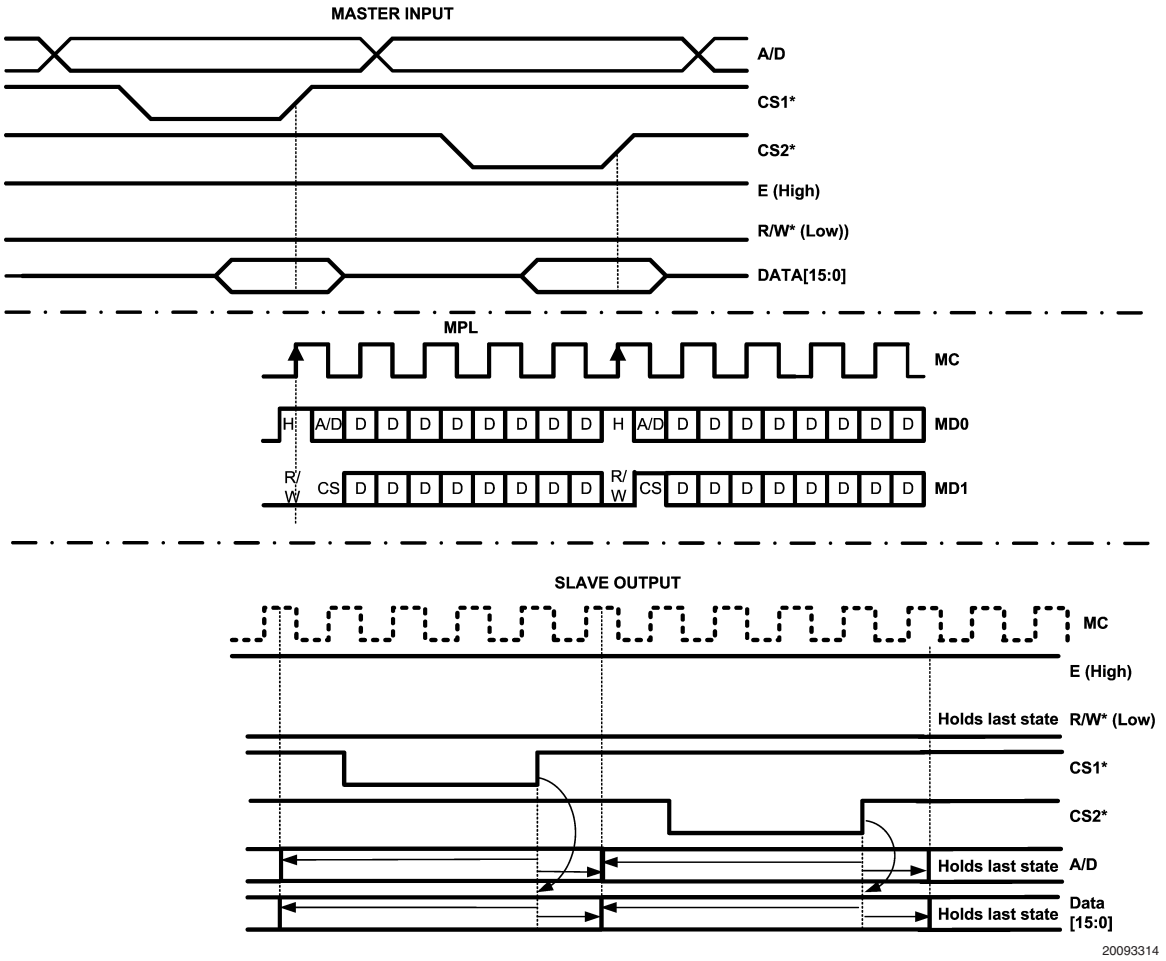


FIGURE 12. Back-to-Back WRITE Operations — m68 Mode

Figure 12 illustrates a m68 mode WRITE operation to the main display (CS1*) followed by a WRITE operation to the sub display (CS2*). This example shows the maximum operation rate with no idle time between the serial transactions.

Functional Description (Continued)

CPU MODE — WRITE — m68

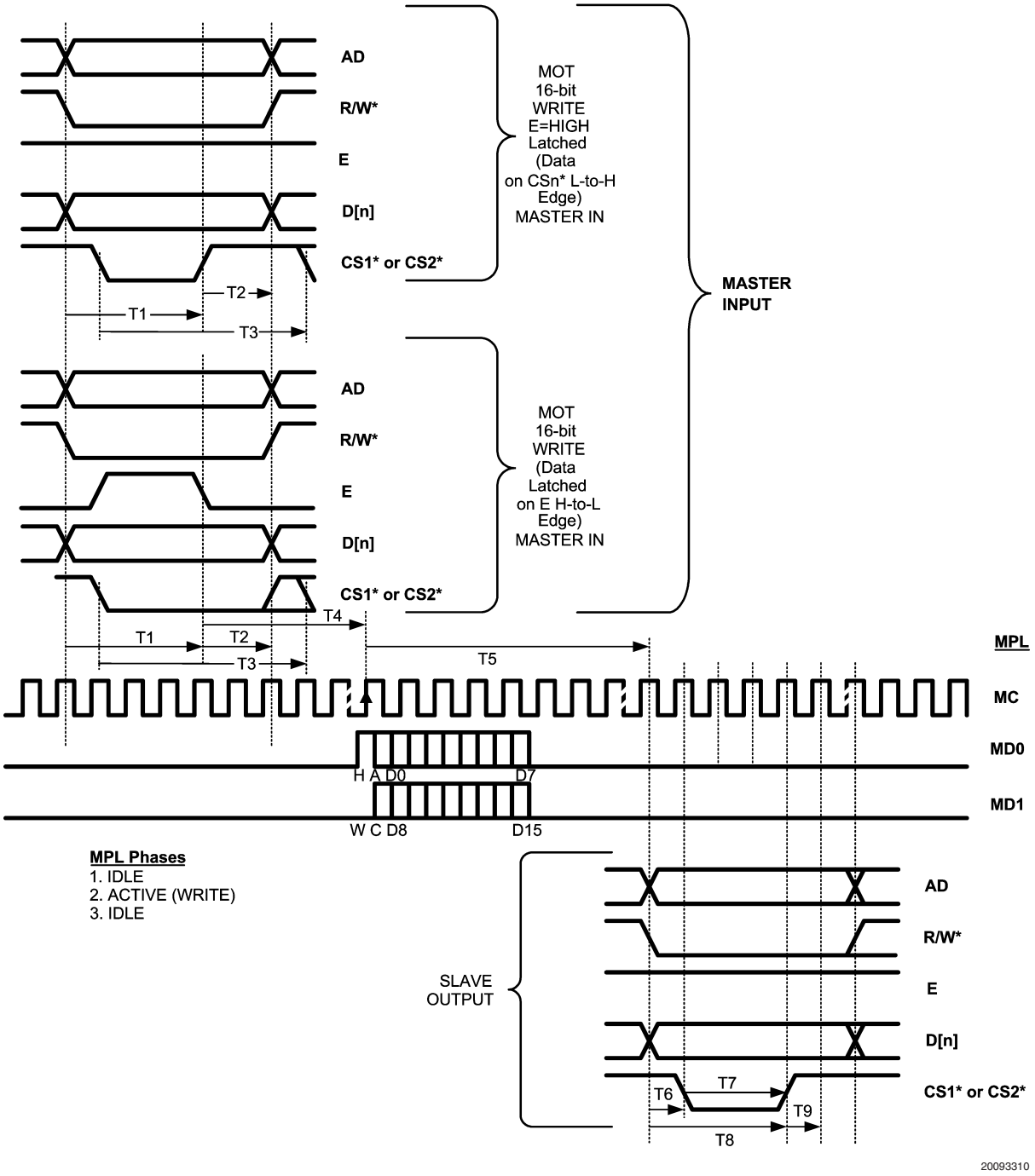


FIGURE 13. WRITE — MOT 6800 µP Interface

Functional Description (Continued)

TABLE 5. WRITE—MOT 6800 µP Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Data Setup Time before ChipSelect* Low-High (or E High-Low)	5			ns
T2	MasterIN	Data Hold after ChipSelect* Low-High (or E High-Low)	5			ns
T3	MasterIN	ChipSelect* Recovery Time, (Note 5)	6			MC Cycles
T4	Master	Master Latency		5		MC Cycles
T5	Slave	Slave Latency		9		MC Cycles
T6	SlaveOUT	Data Valid before ChipSelect* High-Low		1		MC Cycles
T7	SlaveOUT	ChipSelect* Low Pulse Width		3		MC Cycles
T8	SlaveOUT	Data Valid before ChipSelect* Low-High		4		MC Cycles
T9	SlaveOUT	Data Valid after ChipSelect* Low-High		1		MC Cycles

Functional Description (Continued)

CPU MODE — READ — m68

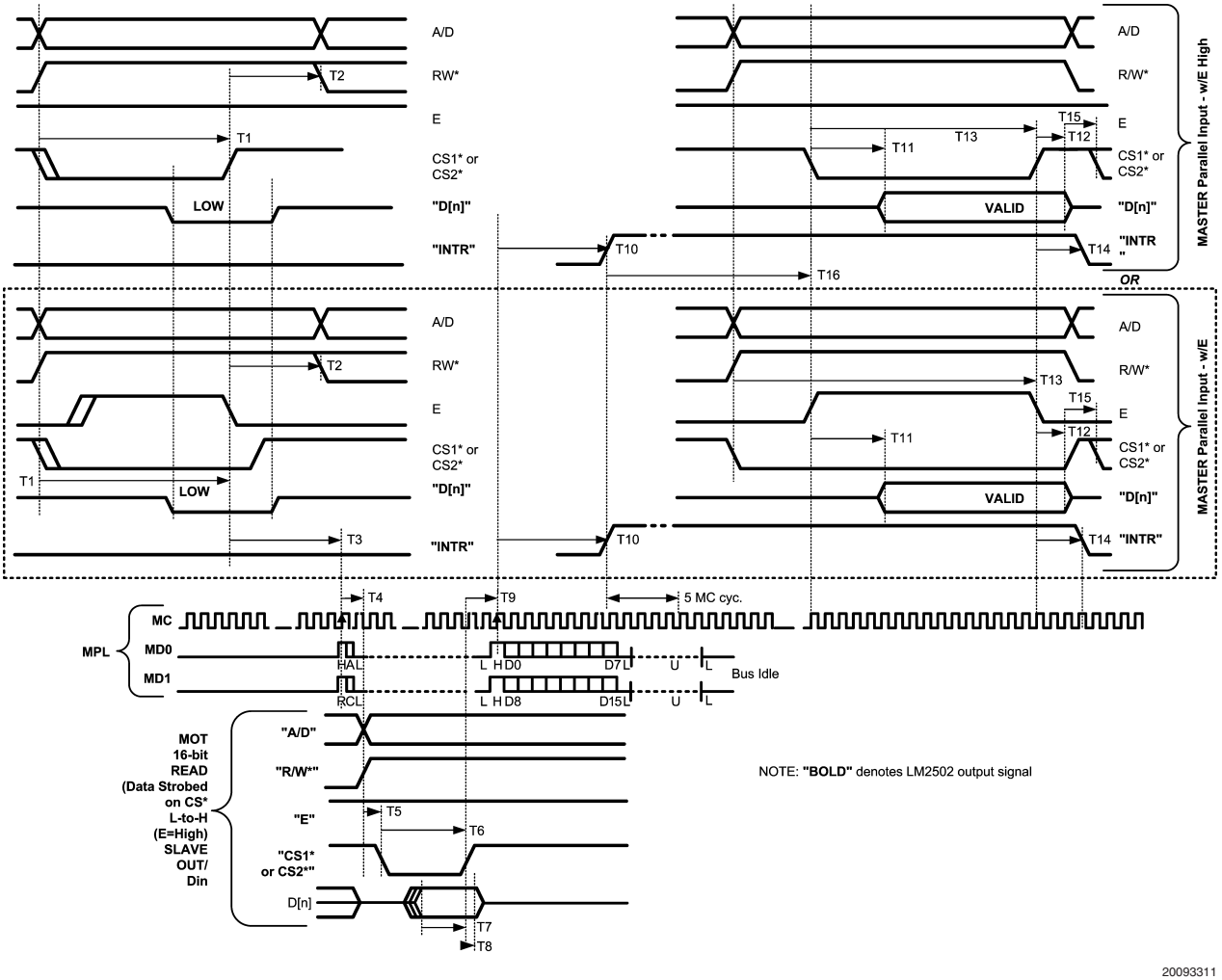


FIGURE 14. READ — 6800 µP Interface

TABLE 6. READ — 6800 µP Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Set Up Time (A/D, R/W*) and Data On Time	20			ns
T2	MasterIN	Hold Time (A/D, R/W*) and Data Off Time		15		ns
T3	Master	Master Latency		5		MC Cycles
T4	Slave	Slave Latency		6		MC Cycles
T5	Slave	ChipSelect* Delay		1		MC Cycles
T6	Slave	ChipSelect Low Pulse Width		6		MC Cycles
T7	Slave	Data Set Up Time	5			ns
T8	Slave	Data Hold Time	15			ns
T9	Slave	Slave Read Latency		4		MC Cycles
T10	Master	MST Read Latency and INTR Delay		12		MC Cycles
T11	Master	Data Delay		18.6		ns
T12	MasterOUT	Data Valid after Strobe		15		ns
T13	MasterOUT	CS* or E active pulse width	20			ns
T14	MasterOUT	INTR De-assert		5		MC Cycles

Functional Description (Continued)

TABLE 6. READ—6800 µP Interface Parameters (Continued)

No.		Parameter	Min	Typ	Max	Units
T15	MasterOUT	Recovery Time		5		ns
T16	MasterOUT	INTR Response, (Note 5)	0			MC Cycles

For the MOT CPU 68xx mode, the Master accepts data on the CS* Low-to-High transition or the E High-to-Low transition, which ever come first. The Slave output only uses the CS* pin for data strobe/latch, as the E signal is held constantly High.

CPU MODE—WRITE—i80

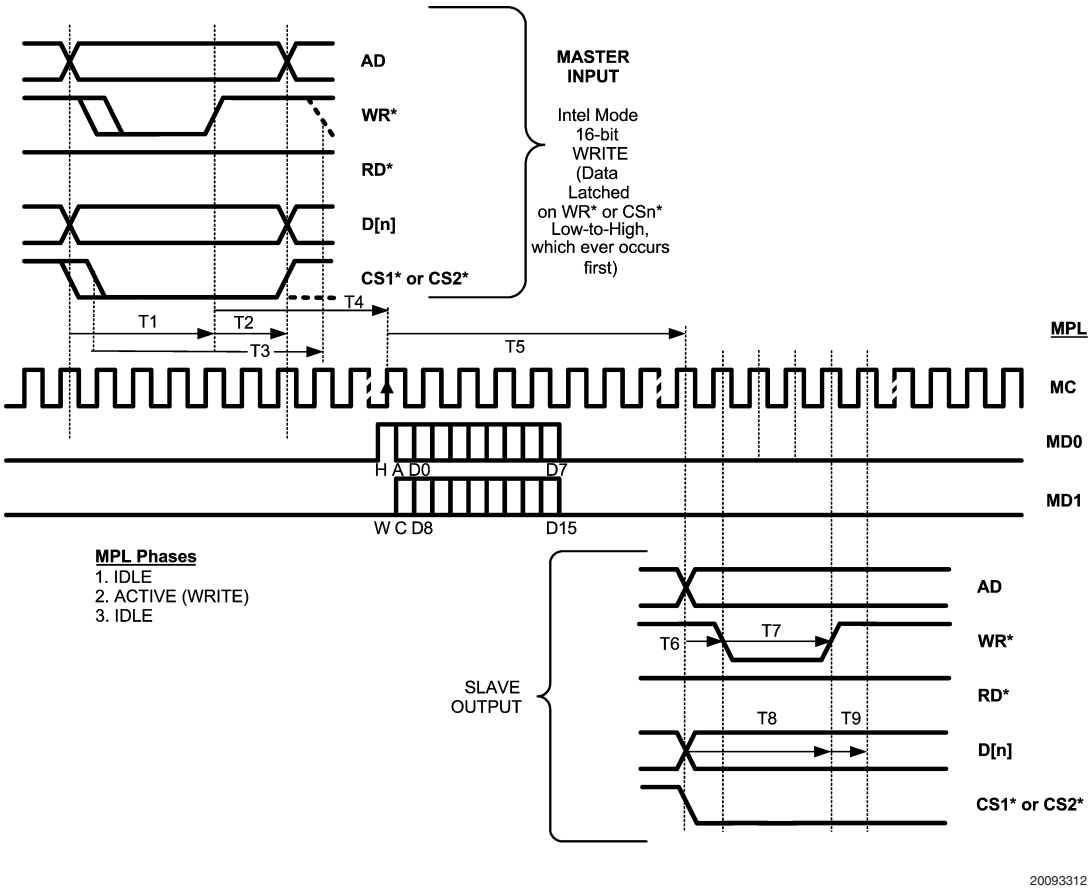


FIGURE 15. WRITE—80xx µP Interface

TABLE 7. WRITE—80xx µP Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Data Setup before Write* High	5			ns
T2	MasterIN	Data Hold after Write* High	5			ns
T3	MasterIN	Write* Recovery Time, (Note 5)	6			MC Cycles
T4	Master	Master Latency		5		MC Cycles
T5	Slave	Slave Latency		9		MC Cycles
T6	SlaveOUT	Data Valid before Write* High-to-Low		1		MC Cycles
T7	SlaveOUT	WR* Pulse Width Low		3		MC Cycles
T8	SlaveOUT	Data Valid before Write* Low-to-High		4		MC Cycles
T9	SlaveOUT	Data Valid after Write* Low-to-High		1		MC Cycles

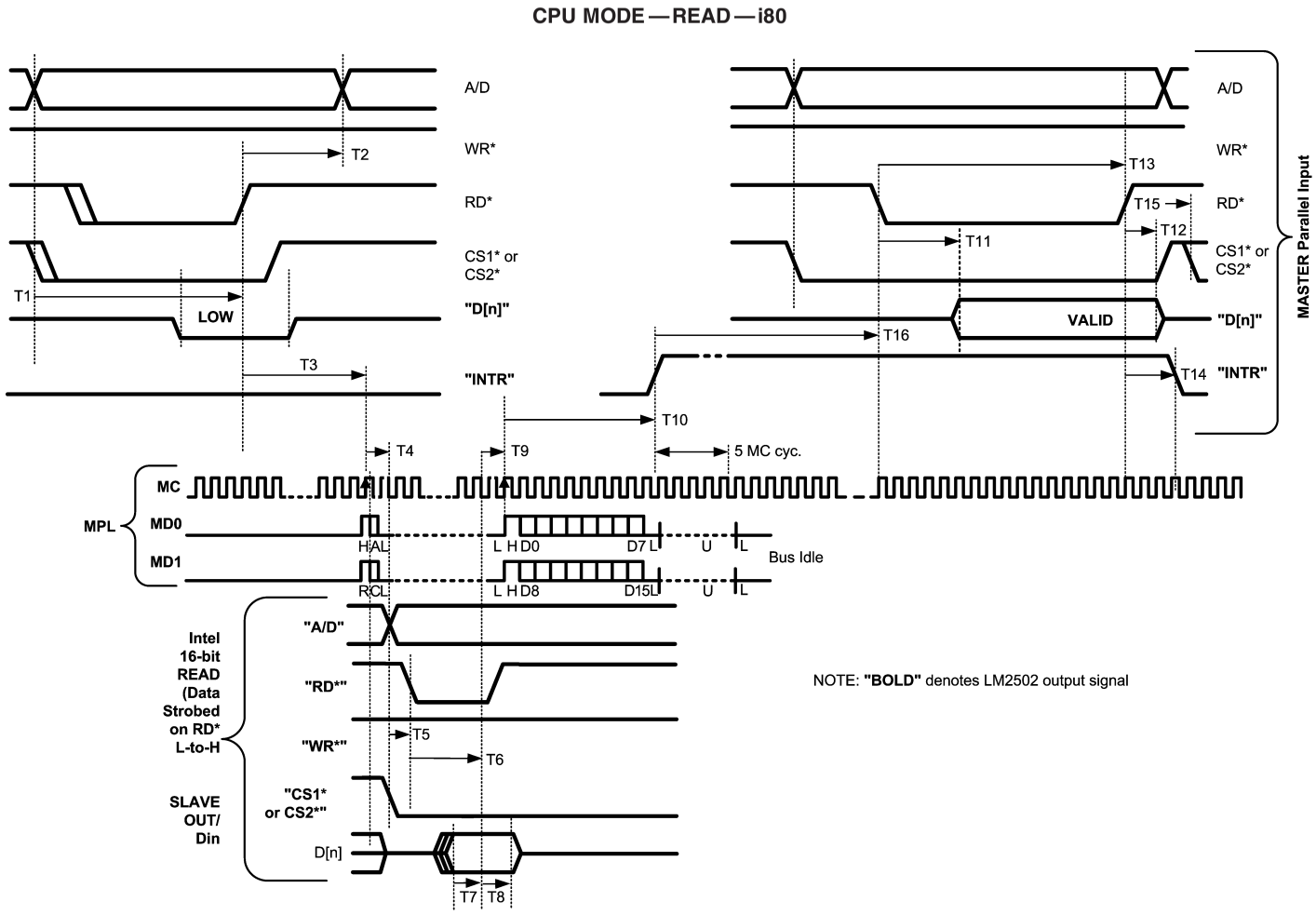


FIGURE 16. READ — INTEL µP Interface

Functional Description (Continued)

TABLE 8. READ—Intel µP Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Set Up Time (A/D, RD*) and Data On Time	20			ns
T2	MasterIN	Hold Time (A/D, RD*) and Data Off Time		15		ns
T3	Master	Master Latency		5		MC Cycles
T4	Slave	Slave Latency		6		MC Cycles
T5	Slave	Read* Delay		1		MC Cycles
T6	Slave	Read Low Pulse Width		6		MC Cycles
T7	Slave	Data Set Up Time	5			ns
T8	Slave	Data Hold Time	15			ns
T9	Slave	Slave Read Latency		4		MC Cycles
T10	Master	MST Read Latency and INTR Delay		12		MC Cycles
T11	Master	Data Delay		18.6		ns
T12	MasterOUT	Data Valid after Strobe		15		ns
T13	MasterOUT	RD* active pulse width	20			ns
T14	MasterOUT	INTR De-assert		5		MC Cycles
T15	MasterOUT	Recovery Time		5		ns
T16	MasterOUT	INTR Response, (Note 5)	0			MC Cycles

LM2502 Features and Operation

POWER SUPPLIES

The V_{DDcore} and V_{DDA} (MPL and PLL) must be connected to the same potential between 2.9V and 3.3V. V_{DDIO} powers the logic interface and may be powered between 1.7 and 3.3V to be compatible with a wide range of host and target devices. V_{DDIO} should not be powered up without V_{DDcore}/ V_{DDA} applied as V_{DDcore} biases the IO ring. During power up, all rails should power up at the same time, or V_{DDcore}/ V_{DDA} should lead.

POWER DOWN/OFF

The Master and the Slave provide a PD* pin to save power when the link is not needed. A Low on this pin will power down the entire device and turn off the line current to MD0, MD1, and MC.

During power up, the PD* inputs should be held LOW and released once power is stable and within specification. The Slave PD* may be released first or at the same time as the Master's PD* pin. CLK (Master) should be applied prior to releasing PD*. If the Powerdown state is not required, the PD* pins maybe connected to V_{DDIO}, however V_{DDIO} should power up smooth through the logic threshold region.

In Powerdown (PD* = GND) the following outputs are driven to:

Master:

INTR = L

Slave depends on mode configuration - see *Table 9*.

TABLE 9. SLV Output in Powerdown

Pin	SLV i80	SLV m68
AD	H	H
Data[n]	L	L
CLK	L	L
CS1*	H	H
CS2*	L	H
MF0	H	H
MF1	H	H

BYPASS RECOMMENDATIONS

Bypass capacitors should be placed near the power supply pins of the device. Use high frequency ceramic (surface mount recommended) 0.1 µF capacitors. A 2.2 to 4.7 µF Tantalum capacitor is recommended near the Master (SER) V_{DDA} pin for PLL bypass. Connect bypass capacitors with wide traces and use dual or larger via to reduce resistance and inductance of the feeds. Utilizing a thin spacing between power and ground planes will provide good high frequency bypass above the frequency range where most typical surface mount capacitors are less effective. To gain the maximum benefit from this, low inductance feed points are important. Also, adjacent signal layers can be filled to create additional capacitance. Minimize loops in the ground returns also for improved signal fidelity and lowest emissions.

UN-USED/OPEN PINS

Unused inputs must be tied to the proper input level—do not float them. Unused outputs should be left open to minimize power dissipation.

PHASE-LOCKED LOOP

When the LM2502 is configured as a Master, a PLL is enabled to generate the serial link clock. The Phase-locked loop system generates the serial data clock at several multiples of the input clock. The PLL operates with an input clock

LM2502 Features and Operation

(Continued)

between 3 and 26 MHz. See *Table 10* below, Multiplier/ Divisor times CLK rate must also be less than 76.8 MHz. The 76.8 MHz limitation is based on the semiconductor process used on this implementation—it is not an MPL limitation.

Line rate should also be selected such that it is faster than the input load rate when bursting data across the link. Otherwise 8/10 X Line rate must be greater than the input load rate to the Master. At the maximum raw data rate of 307 Mbps, the maximum information rate is 245 Mbps. Thus the parallel load rate at the Master input must not exceed 15.4 Mega Transfers per second sustained (of 16 data bits). The Master can accommodate up to four words at a higher rate due to internal FIFOs.

Configuration pins (PLL_CON[2:0], and M/S*) are used to determine the mode of which the part is operating in. In the Slave configuration the PLL block is disabled. The Slave PLL_CON pins are required to set up the proper divisor for the CLK pin. Slave PLL_CON[2:0] pins do not need to be set the same as the Master, this allows for clock multiplication / division to be supported for the output clock reference signal.

RESET

On both the Master and the Slave, the PD* pin resets the logic. The PD* pins should be held low until the power supply has ramped up and is stable and within specifications. The Slave PD* pin should be driven High first or at the same time as the Master. This will ensure that the Slave sees the start up sequence from the Master.

MASTER/SLAVE SELECTION

The M/S* pin is used to configure the device as either a Master or Slave device. When the M/S* pin is a Logic High, the Master configuration is selected. The Driver block is enabled for the MC line, and the MD lines. When the M/S* pin is a Logic Low, the Slave configuration is selected. The Receiver block is enabled for the MC line, and the MD lines.

TABLE 10. PLL_CON Settings

PLLCON2	PLLCON1	PLLCON0	Multiplier (Master) MC out	Divisor (Slave) CLKout	Minimum CLK Input	Maximum CLK Input (MC ≦ 76.8 MHz)
0	0	0	CLK X 2	MC / 2	13 MHz	26 MHz
0	0	1	CLK X 4	MC / 4	6 MHz	19.2 MHz
0	1	0	CLK X 6	MC / 6	3 MHz	12.8 MHz
0	1	1	CLK X 7	MC / 7	3 MHz	10.97 MHz
1	0	0	CLK X 8	MC / 8	3 MHz	9.60 MHz
1	0	1	CLK X 9	MC / 9	3 MHz	8.53 MHz
1	1	0	CLK X 10	MC / 10	3 MHz	7.68 MHz
1	1	1				*(Reserved)*

Application Information

SYSTEM CONSIDERATIONS

When employing the MPL SERDES chipset in place of a parallel bus, a few system considerations must be taken into account. Before sending commands (ie initialization commands) to the display, the SERDES must be ready to transmit data across the link. The MPL link must be powered up, and the PLL must be locked. Also a review of the Slave output timing should be completed to insure that the timing parameters provided by the Slave output meet the requirements of the LCD driver input. Specifically, pulse width on CSn*, RD* / WR*, data valid time, and bus cycle rate should be reviewed and checked for inter-operability. Additional details are provided next:

The MPL link should be started up as follows: The chipset should be powered up first, V_{DDIO} should not be powered up first, it may be at the same time as V_{DD}/V_{DDA} or lag. During power up, the PD* inputs should be held LOW and released once power is stable and within specification. The Slave PD* may be released first or at the same time as the Master. CLK should be applied prior to releasing PD*.

Before data can be sent across the MPL serial link, the link must be ready for transmission. The CLK needs to be applied to the device, and the PLL locked. This is controlled by a keep-off counter set for 4096 cycles. After the PLL has lock and the counter expired, an additional 40 clock cycles are required for the calibration of the MPL link. After this, data may now be written to the device.

It takes 5MC Cycles to send a 16-bit CPU Write including the serial overhead. The MC cycle time is calculated based on the PLL_CON[2:0] setting and also the input clock frequency. For example, a 19.2MHz input CLK and a 4X PLLCON setting yields a MC frequency of 76.8MHz. Thus it takes 65.1ns to send the word in serial form. To allow some idle time between transmissions (this will force a bit sync per word if the gap is long enough in between), the load rate on the Master input should not be faster than 6MC cycles, or every 78ns in our example to support a data pipe line. This is sometimes referred to as the bus cycle time (time between commands).

The Slave output times is also a function of MC cycles. Note that in i80 mode, the width of the WR* pulse (in m68 mode the width of the CS*) pulse low is **three MC cycles** regardless of the pulse width applied to the Master input. System designers need to check compatibility with the display driver to ensure this pulse width meets its requirement. If it is too fast, select a lower PLLCON setting or apply a slower input clock.

The CLK input must be free running and not gapped. If the clock is stopped a RESET (PD* = Low) cycle should be done and the link brought up again.

Application Information (Continued)

MPL SWAP FEATURE

The LM2502 provides a swap function of MPL MD lines depending upon the state of the M/S* pin. This facilitates a straight through MPL interface design eliminating the needs for via and crossovers as shown on *Figure 17*. See also Connection Diagram and *Table 1*.

Note that three pins are defined differently on the MASTER and the SLAVE configured device. Schematic Capture device diagrams should take this into account for proper connection. The following pin descriptions apply for the three pins given in Ball Number : Master (Slave) function

UFBGA Package

- A5 : INTR (CLKDIS*)
- A6 : MD1 (MD0)
- B7 : MD0 (MD1)

LLP Package

- 34 : INTR (CLKDIS*)
- 32 : MD1 (MD0)
- 29 : MD0 (MD1)

FLEX CIRCUIT RECOMMENDATIONS

The three MPL lines should generally run together to minimize any trace length differences (skew). For impedance control and also noise isolation (crosstalk), guard ground traces are recommended in between the signals. Commonly a Ground-Signal-Ground (GSGSGSG) layout is used. Locate fast edge rate and large swing signals further away to also minimize any coupling (unwanted crosstalk). In a stacked flex interconnect, crosstalk also needs to be taken into account in the above and below layers (vertical direction). To minimize any coupling locate MPL traces next to a ground layer. Power rails also tend to generate less noise than LVCMOS so they are also good candidates for use as isolation and separation.

The interconnect from the Master to the Slave typically acts like a transmission line. Thus impedance control and ground returns are an important part of system design. Impedance should be in the 50 to 100 Ohm nominal range for the LM2502. Testing has been done with cables ranging from 40 to 110 Ohms without error (BER Testing). To obtain the impedance, adjacent grounds are typically required (1 layer flex), or a ground shield / layer. Total interconnect length is intended to be in the 20cm range, however 30cm is possible at lower data rates. Skew should be less than 500ps to maximize timing margins.

GROUNDING

While the LM2502 employs three separate types of ground pins, these are intended to be connected together to a common ground plane. The separate ground pins help to isolate switching currents from different sections of the integrated circuit (IC). Also required is a nearby signal return (ground) for the MPL signals. These should be provided next to the MPL signals, as that will create the smallest current loop area. The grounds are also useful for noise isolation and impedance control.

PCB RECOMMENDATIONS

General guidelines for the PCB design:

- Floor plan, locate MPL Master near the connector to limit chance of cross talk to high speed serial signals.
- Route serial traces together, minimize the number of layer changes to reduce loading.
- Use ground lines are guards to minimize any noise coupling (guarantees distance).
- Avoid parallel runs with fast edge, large LVCMOS swings.
- Also use a GSGSG pinout in connectors (Board to Board or ZIF).
- Slave device - follow similar guidelines.
- Bypass the device with MLC surface mount devices and thinly separated power and ground planes with low inductance feeds.
- High current returns should have a separate path with a width proportional to the amount of current carried to minimize any resulting IR effects.

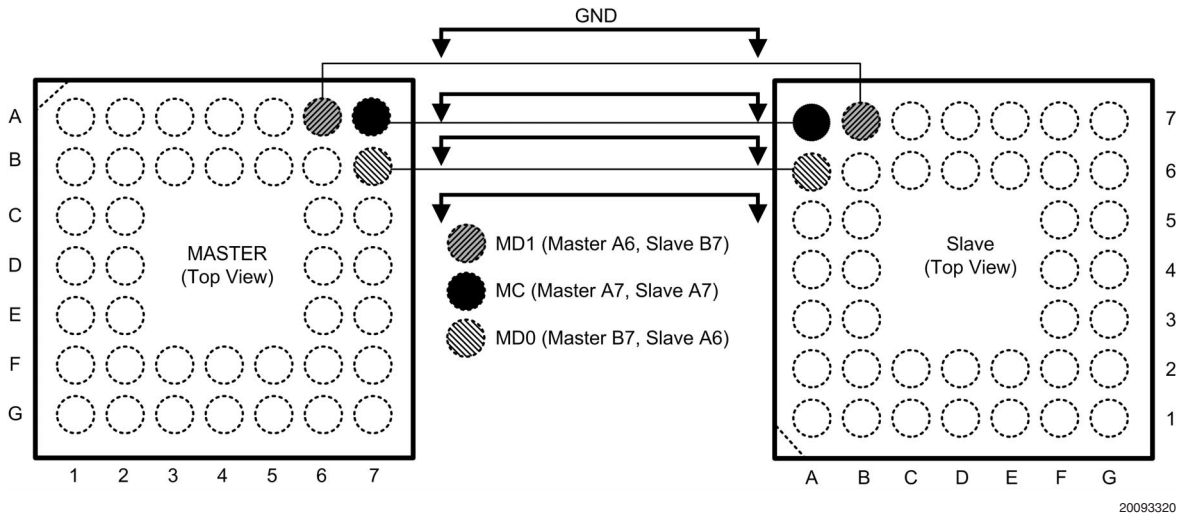


FIGURE 17. MPL Interface Layout - UFBGA Example

Application Information (Continued)

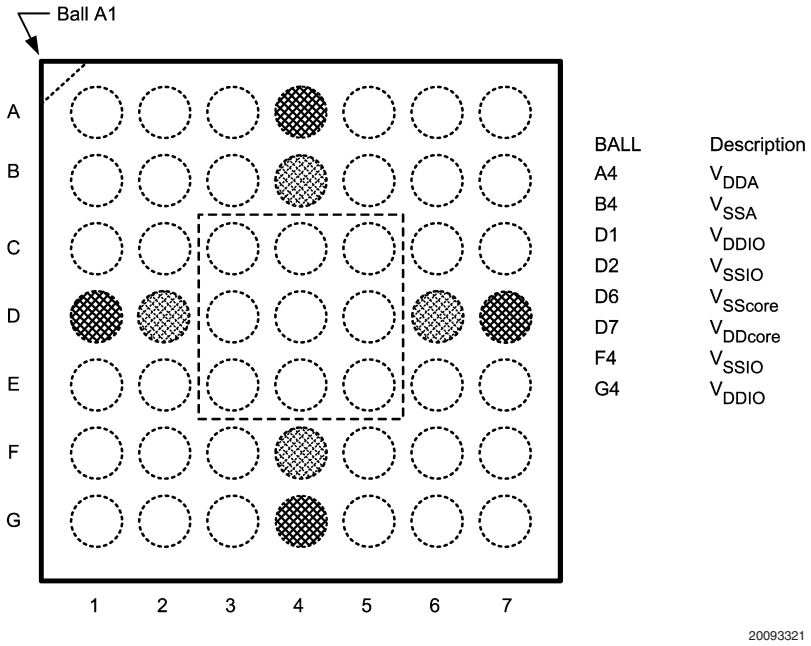


FIGURE 18. LM2502 UFBGA Package PWR (V_{DD}) and GND (V_{SS}) Balls

DISPLAY APPLICATION

The LM2502 chipset is intended for Interface between a host (processor) and a Display. It supports a 16 or 8-bit CPU style interface and can be configured for i80 or m68 modes.

The Master side connection is shown in *Figure 19*. Input Clock frequency and the selection of the PLL_CON setting are determined by system parameters. These include the required display bandwidth, the Master load rate and the Display Driver input timing requirements. See the **System Considerations** section for more details.

The Display side parallel bus may be connected to one or two displays. Each display has its own chipselect signal. If only one display is required, the unused CS signal should be tied HIGH (V_{DDIO}) on the Master, and the unused output left open on the Slave. The Slave provides an optional clock output. If this is desired the CLKDIS* pin needs to be also tied HIGH. A different PLL_CON setting can be used to alter the frequency if desired. As the Divisor setting in the Slave is not used for data recovery. For the dual display application, the multidrop bus should be laid out to minimize any resulting stub lengths on the Data, A/D, and control signals.

If required, the Slave output clock can be enabled to provide a output frequency reference. The frequency can be adjusted by setting different PLL_CON (divisor) settings (on the Slave). This can then be used as a frequency reference signal to the display module or other subsystem (ie camera module). If the CLK output is not needed, tie the Slave CLKDIS* pin Low to disable it. The Clock is available when ever the MPL link is enabled.

Application Information (Continued)

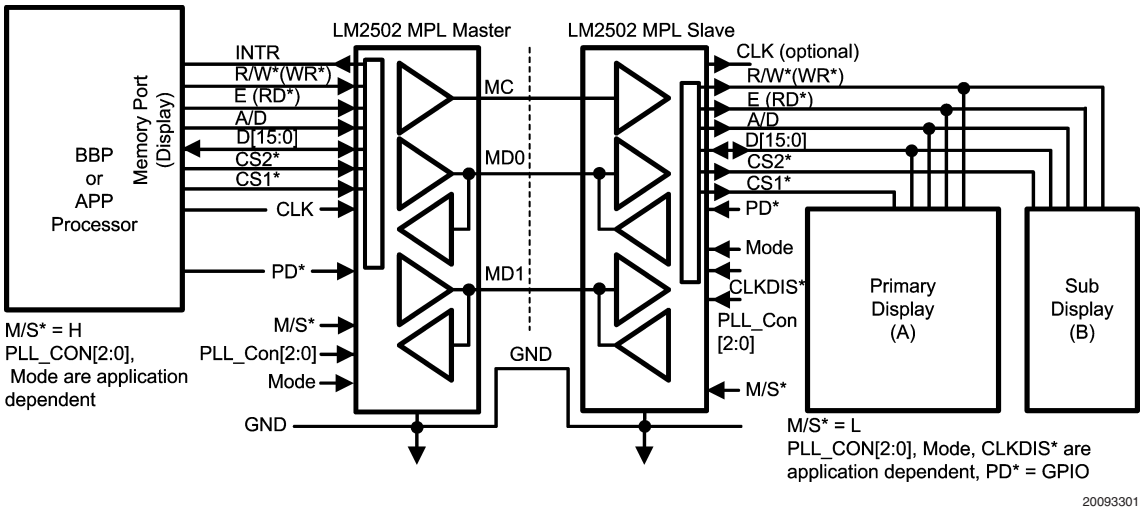


FIGURE 19. Display Interface Application

RGB565 APPLICATION

The LM2502 chipset may also be configured for a RGB565 application. This is also known as a "buffer-less" or "dumb" display application. In this configuration 16 color bits (R[4:0], G[5:0], B[4:0]), Pixel Clock (PCLK) and two control bits (VS and HS) are supported. An external invertor is also required.

To configure for the RGB565 mode, the i80 mode must be selected. The Pixel clock should be connected to both the CLK input and the WR* pins on the Master. The PLL_CON pins should be configured for a 6X mode, as it takes 5 MC cycles to transfer the RGB data, and the 6X setting will provide a 50% output PCLK from the Slave device. The 50% duty cycle PCLK is created by the WR* signal which pulses low for 3 MC cycles and is high for 2 MC cycles and an idle MC cycle. See *Figure 20* for details. Support is provided for PCLKs in the 3 to 12.8 MHz range. PLLCON setting of X8 is also possible, however, the Slave output PCLK (WR*) will have some duty cycle distortion (37.5%) and the CLK range is further restricted.

Slower PCLK rates maybe supported if a higher frequency multiple of the PCLK is available. For example, if a 2MHz PCLK is required, then a 6MHz CLK (freq locked, not phase) may be applied to the MST CLK input and the 2MHz PCLK to the MST WR* signal input. The PLLCON setting should be selected as 2X (PLLCON[2:0] = 000'b). Once again 5 MC cycles are required to transfer the pixel data, and the WR* (PCLK) will be 50% duty cycle. The applied CLK and PLLCON should be selected such that is creates a 6X multiple on MC to ensure a 50% duty cycle.

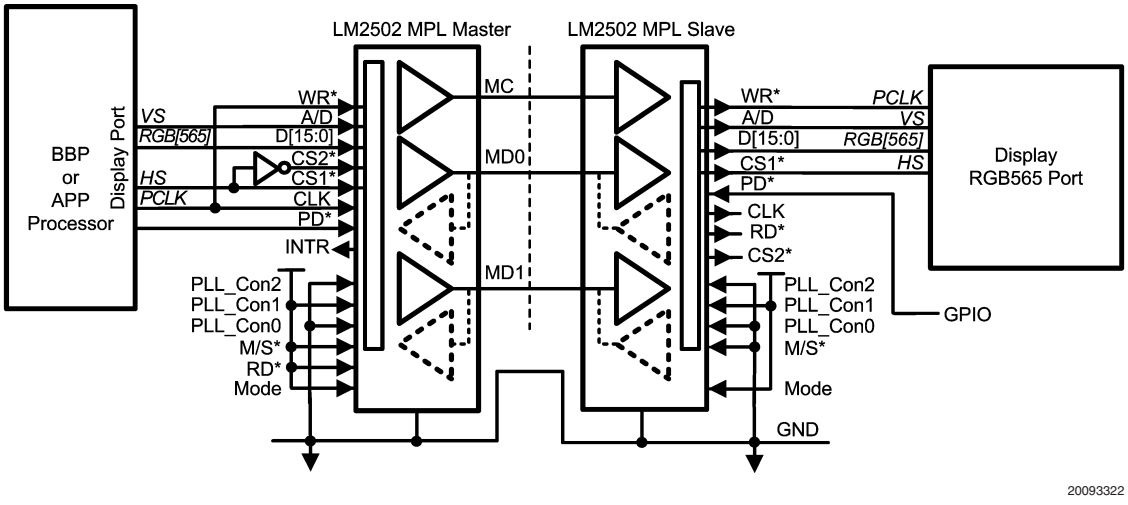


FIGURE 20. RGB565 Application

QVGA Example - For a QVGA display (320 by 240), with 16 bits of color depth and 60 frames per second, a net bandwidth requirement is 73.728 Mbps. Maximum transfer rate

Application Information (Continued)

for the LM2502 chipset is 245 Mbps (307 Mbps raw - includes overhead), thus there is adequate bandwidth for this application and even larger resolution displays.

Figure 21 shows the typical timing of the RGB application. The 6X PLL setting (PLLCON[2:0] = 010'b) is selected. The PCLK is applied to both the WR* and CLK inputs on the Master. The rising edge on the WR* (PCLK) signal samples the data by the Master for serialization. The CLK input can be the PCLK (if timing requirements are met) or a synchronous clock to the PCLK signal. The HS connects to the CS1* signal and the HS* (inverted HS) is connected to the CS2*. With this configuration there will always be a valid CS* LOW on the Master input. The RGB information is then serialized and passed to the Slave via the MPL bus. It takes 5 MC cycles to complete the transfer and with the 6X PLL setting, there will be two idle bits on the MD (1 MC cycle) lines before the next transfer. Recovery of the RGB interface (RGB565, HS, VS and PCLK) is provided at the Slave output. The PCLK is slightly shifted later in time (1 MC cycle) but adequate timing margin (increased set, shorted hold) is still provided.

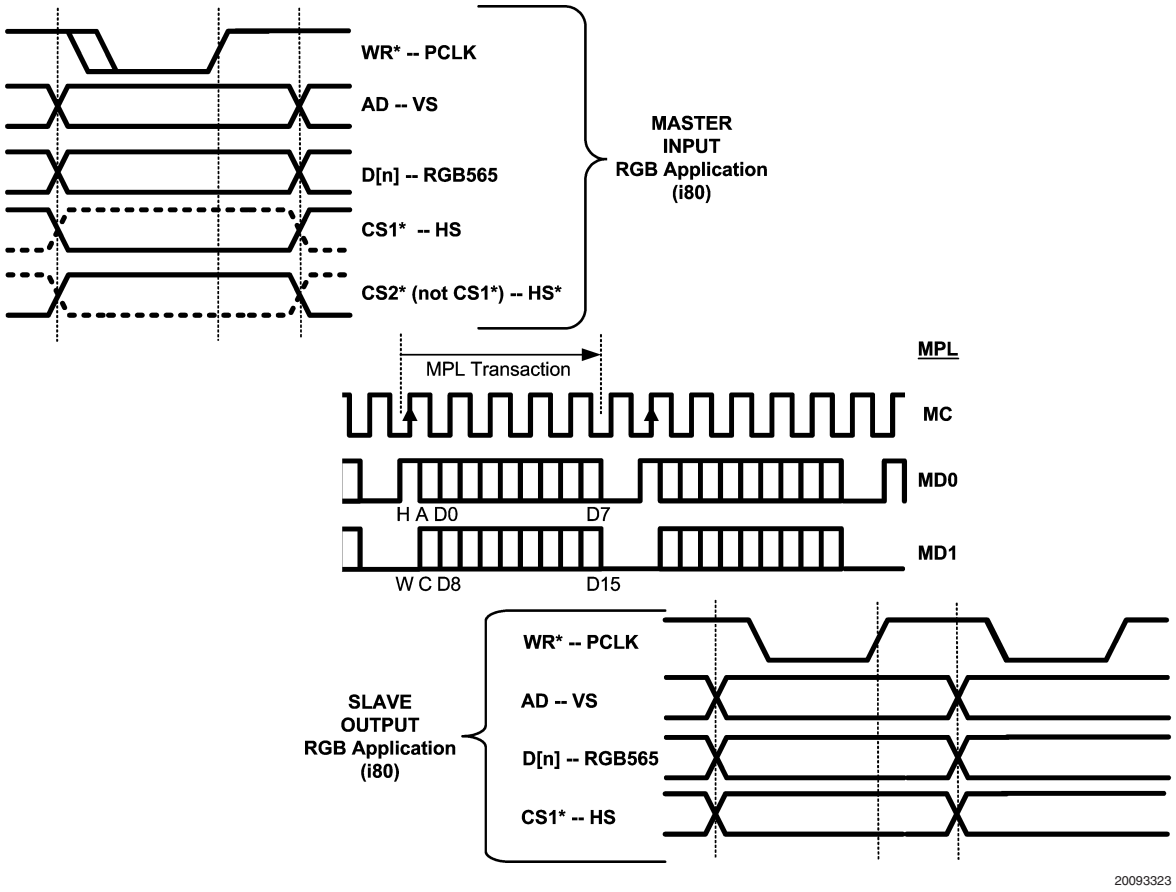
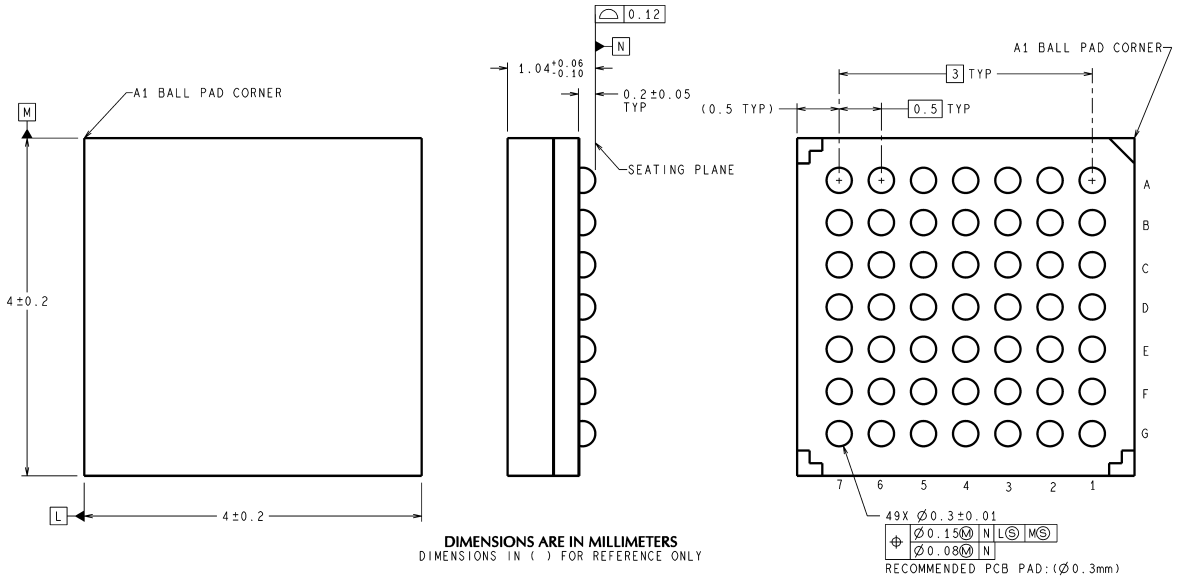


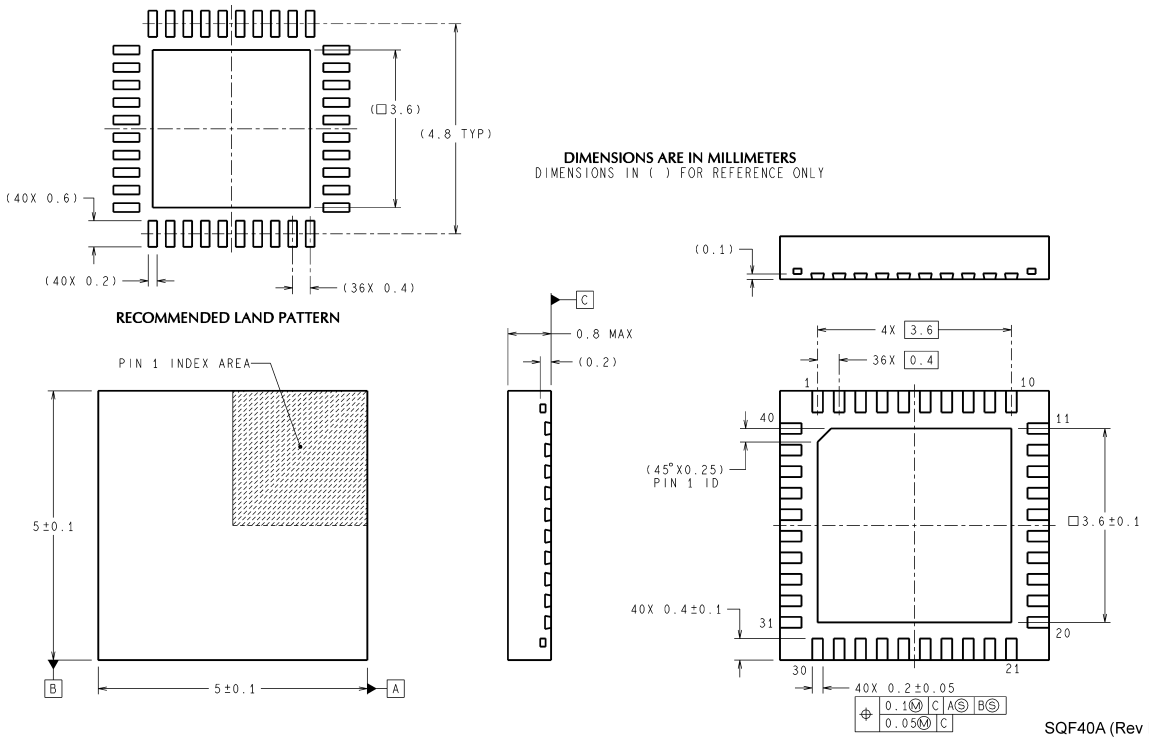
FIGURE 21. RGB565 Application Timing

Physical Dimensions inches (millimeters) unless otherwise noted



SLH49A (Rev B)

49 Lead UFBGA, 0.5mm pitch
Order Number LM2502SM
NS Package Number SLH49A



SQF40A (Rev B)

40 Lead LLP, 0.4mm pitch
Order Number LM2502SQ
NS Package Number SQF40A

Notes

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