

Low forward voltage Transil™, transient voltage suppressor

Features

- Low forward voltage: 1.05 V @ 850 mA
- Peak pulse power (8/20 μs): 350 W
- Very low clamping factor V_{CL}/V_{BR}
- Unidirectional device
- Fast response time
- Very thin package: 0.605 mm
- RoHS compliant

Complies with the following standards:

- IEC 61000-4-2 level 4
 - ± 15 kV (air discharge)
 - ± 8 kV (contact discharge)

Description

The LFTVS7-1F3 is a single line diode designed specifically for the protection of integrated circuits in portable equipment and miniaturized electronics devices subject to ESD and EOS transient overvoltages.

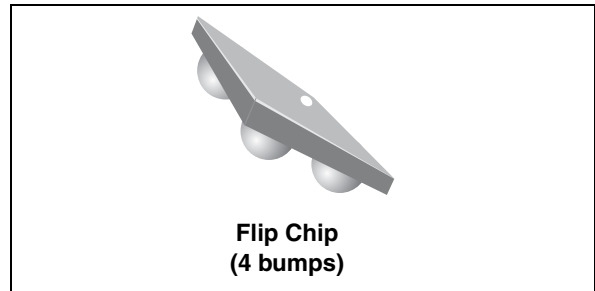


Figure 1. Pin configuration (bump side)

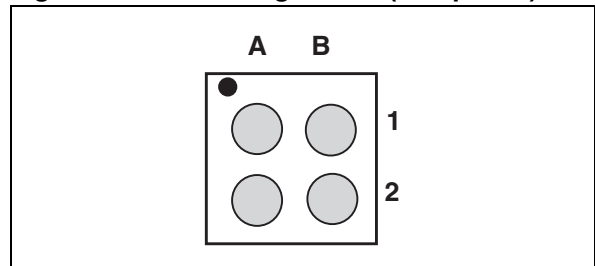
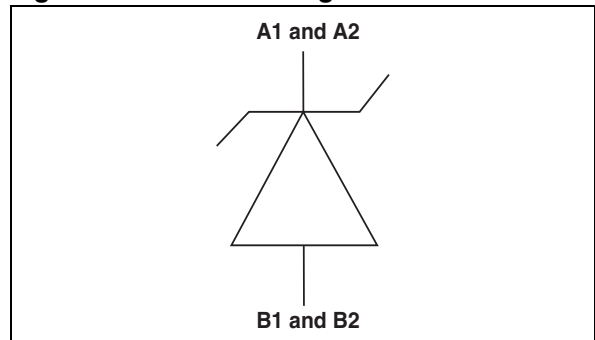


Figure 2. Device configuration



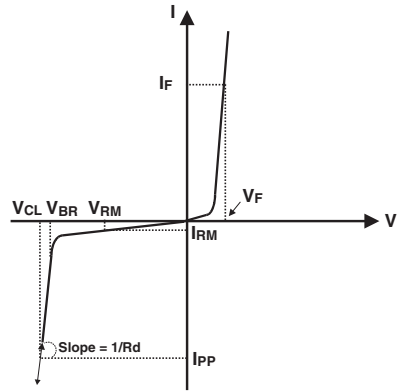
TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Test condition	Value	Unit
P_{PP}	Peak pulse power dissipation (10/1000 μs pulse)	$T_j \text{ initial} = T_{amb}$	75	W
	Peak pulse power dissipation (8/20 μs pulse)		350	
I_{FSM}	Non repetitive surge peak forward current	$t_p = 10\text{ ms}$ $T_j \text{ initial} = T_{amb}$	11	A
T_j	Maximum operating junction temperature		125	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		-55 to +150	$^{\circ}\text{C}$

Table 2. Electrical characteristics ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter				
V_{BR}	Breakdown voltage				
I_{RM}	Leakage current @ V_{RM}				
V_{RM}	Stand-off voltage				
V_{CL}	Clamping voltage				
R_d	Dynamic impedance				
I_{PP}	Peak pulse current				
αT	Voltage temperature coefficient				
V_F	Forward voltage drop				
Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 15\text{ mA}$	7			V
I_{RM}	$V_{RM} = 5.5\text{ V}$			500	nA
V_{CL}	$I_{PP} = 1\text{ A}^{(1)}$			10	V
V_F	$I_F = 850\text{ mA}$			1.05	V
αT				6	$10^{-4}/^{\circ}\text{C}$
C_{line}	$V_R = 0\text{ V}$, $V_{OSC} = 30\text{ mV}$, $F = 1\text{ MHz}$		320		pF

1. 8 / 20 μs pulse waveform

Figure 3. Relative variation of peak pulse power versus initial junction temperature

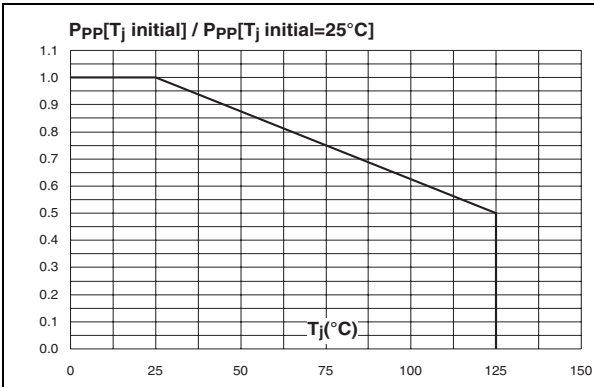


Figure 4. Peak pulse power versus exponential pulse duration (typical value)

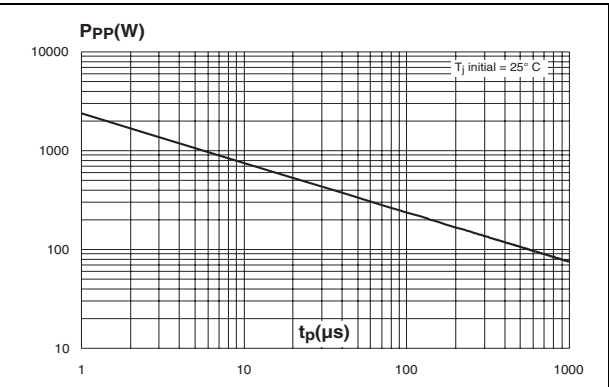


Figure 5. Clamping voltage versus peak pulse current (typical values)

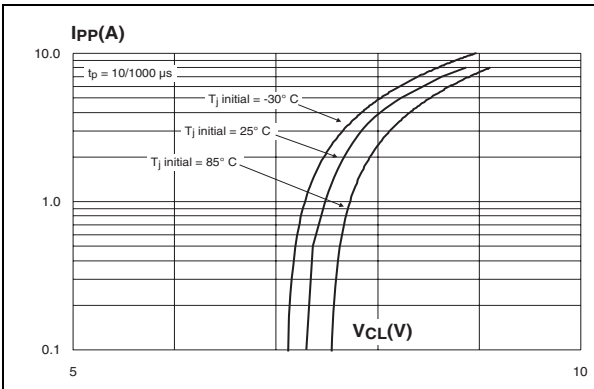


Figure 6. Relative variation of leakage current versus junction temperature (typical values)

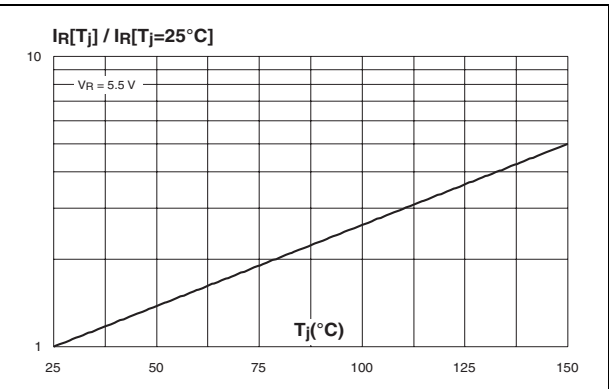


Figure 7. Forward voltage drop versus peak forward current (typical values)

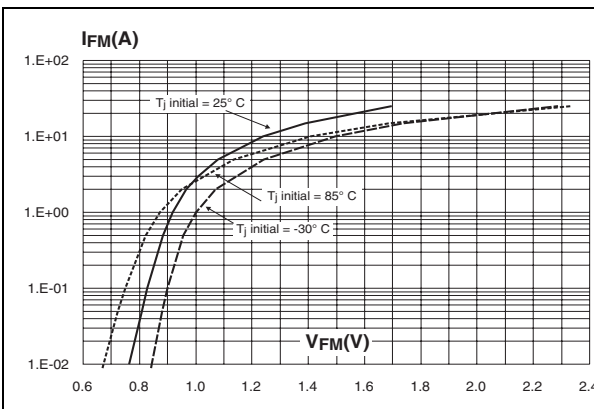


Figure 8. Junction capacitance versus reverse voltage applied (typical values)

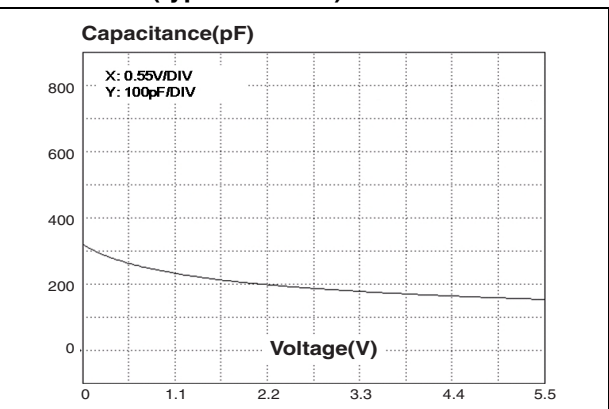


Figure 9. Breakdown voltage versus initial junction temperature (typical value)

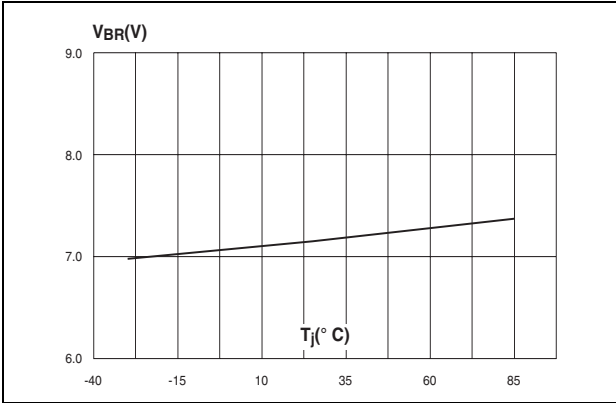


Figure 10. Frequency response

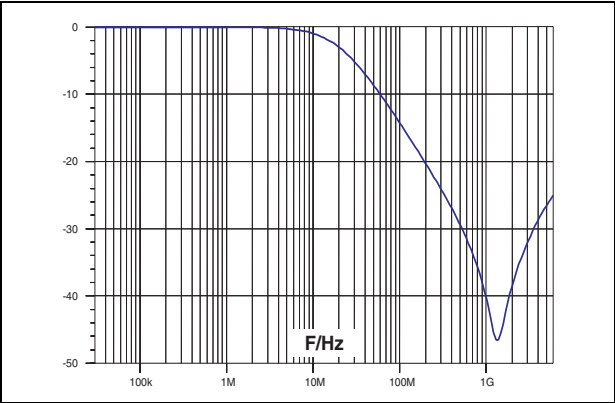


Figure 11. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

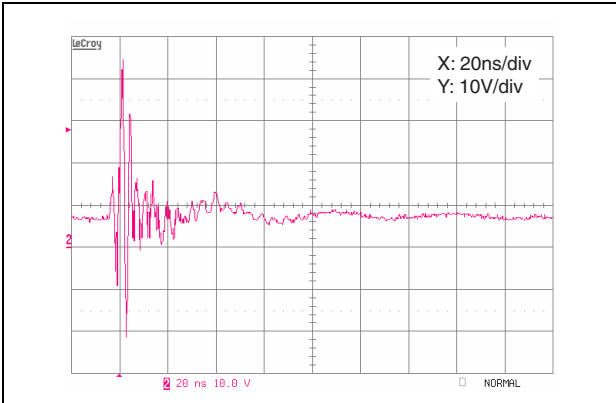
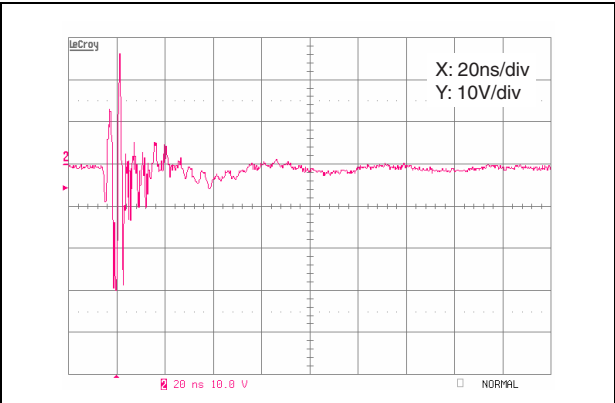
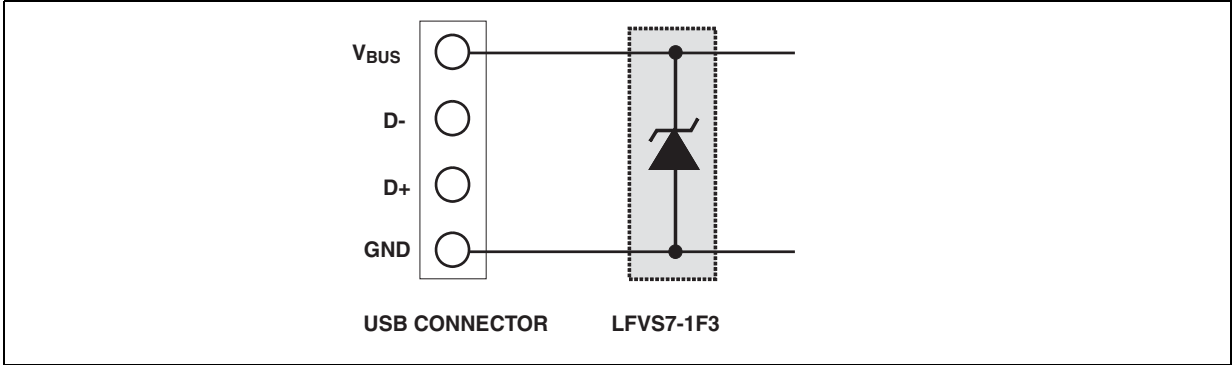


Figure 12. ESD response to IEC 61000-4-2 (-8 kV contact discharge)



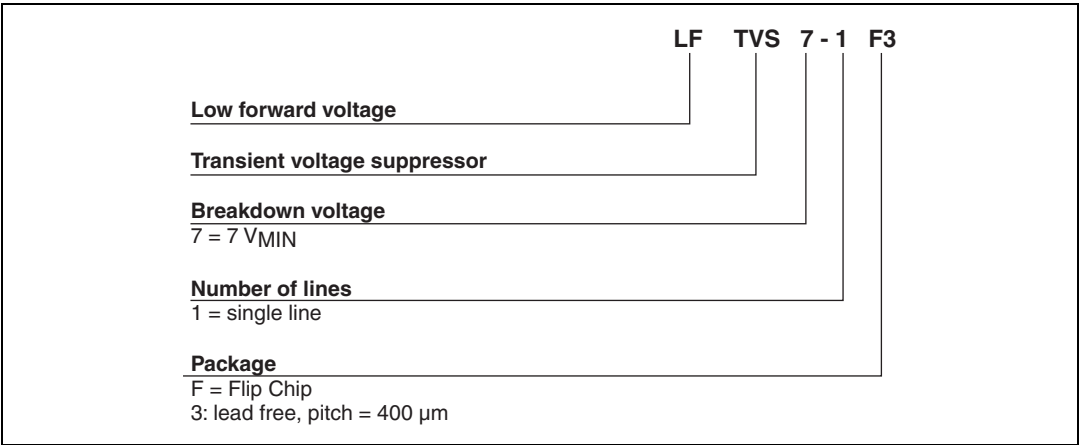
2 Application information

Figure 13. Application schematic



3 Ordering information scheme

Figure 14. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 15. Flip Chip dimensions

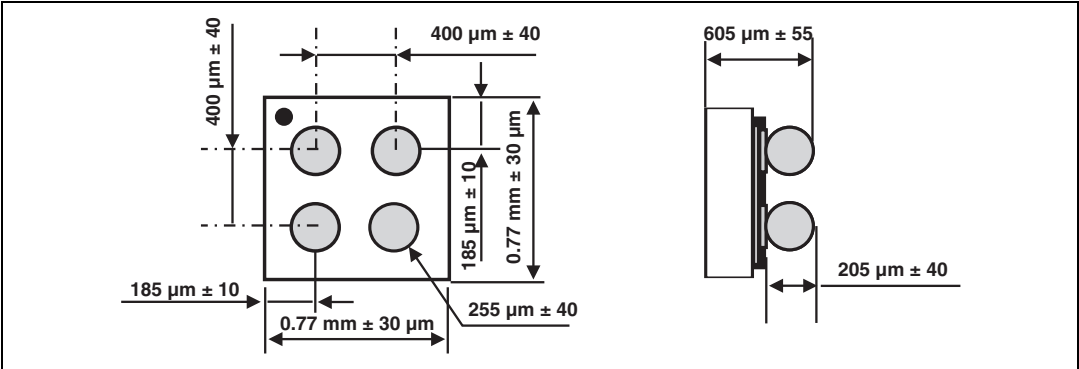
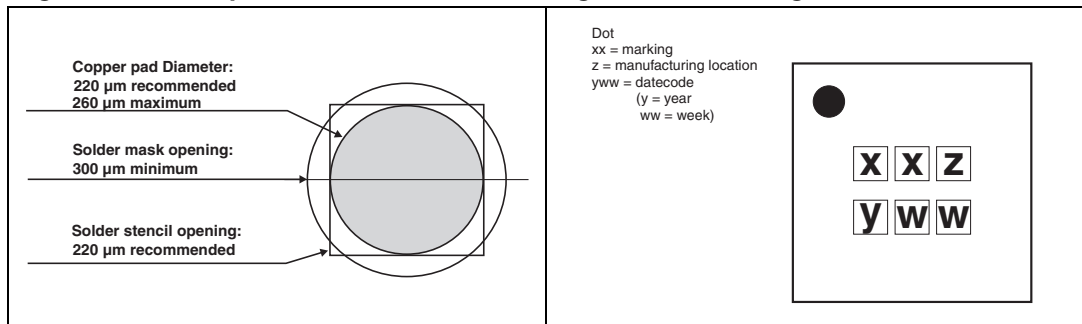
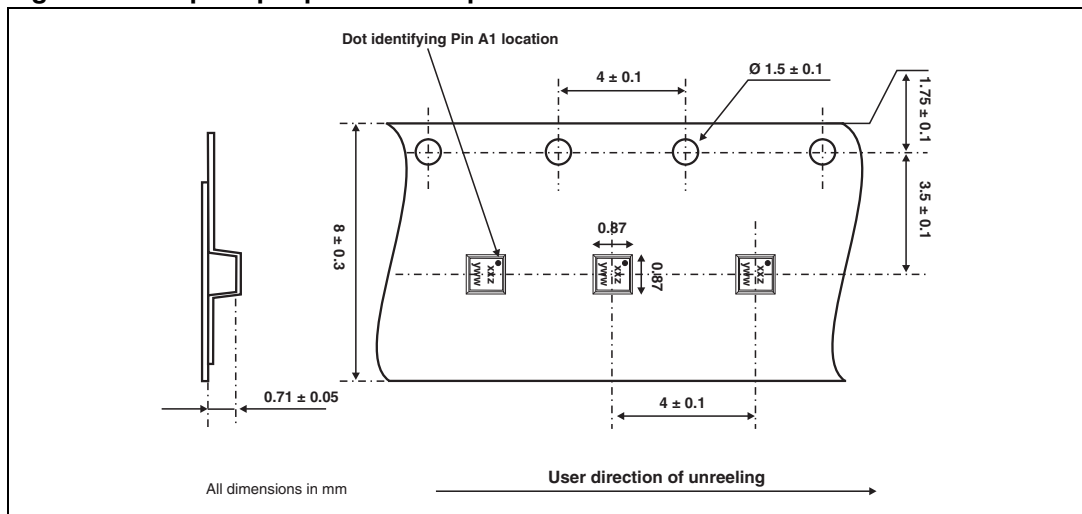


Figure 16. Foot print recommendations Figure 17. Marking**Figure 18. Flip Chip tape and reel specifications**

Note:

More information is available in the application notes:

AN2348: "400 μm Flip Chip: Package description and recommendations for use"

AN1751: "EMI Filters: Recommendations and measurements"

5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
LFTVS7-1F3	EJ	Flip Chip	0.86 mg	5000	Tape and reel (7")

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
01-Mar-2007	1	Initial release.
16-Apr-2008	2	Updated ECOPACK statement. Updated Figure 14 , and Figure 15 . Reformatted to current standards. Changed V_F from 1.2 to 1.05 V.

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