


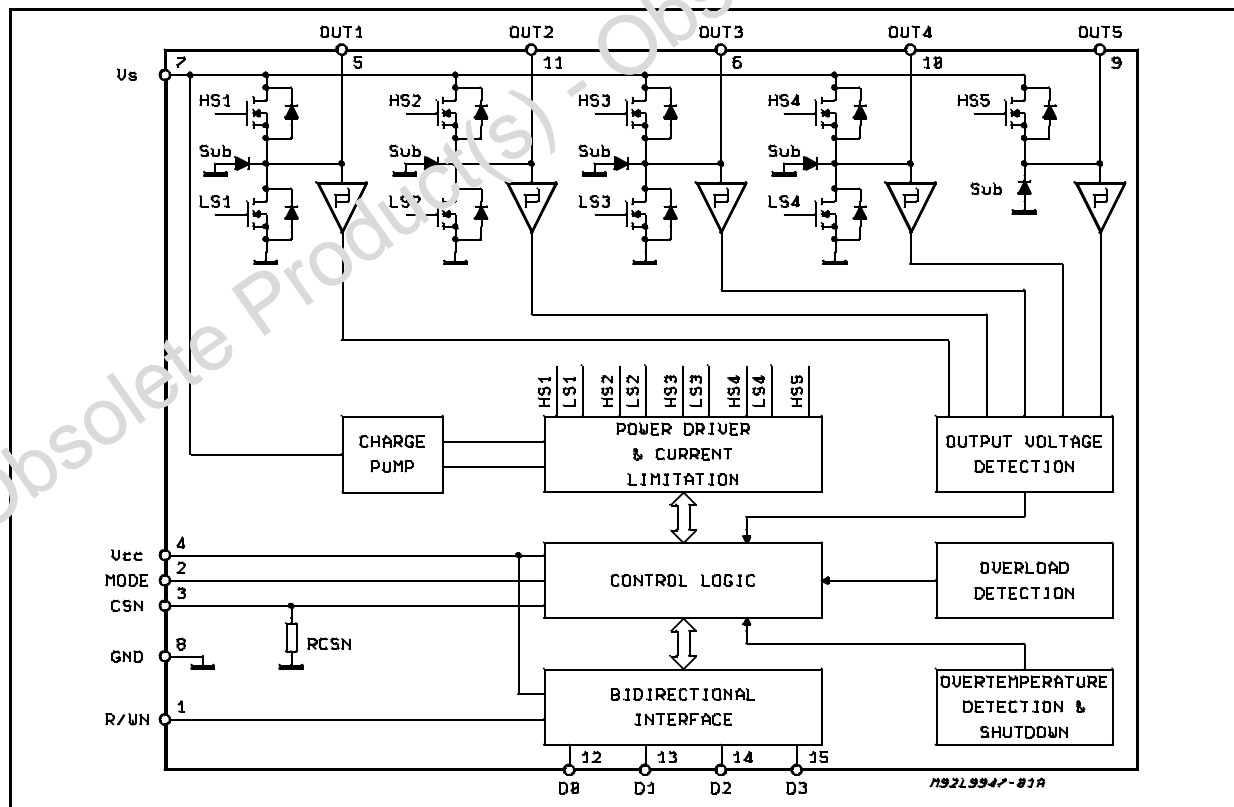
## QUAD HALF-BRIDGE AND SINGLE HIGH-SIDE DRIVER

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- Multiwatt 15**
- ORDERING NUMBER: L9947S**

## DESCRIPTION

The L9947 is a bus controlled power interface in-

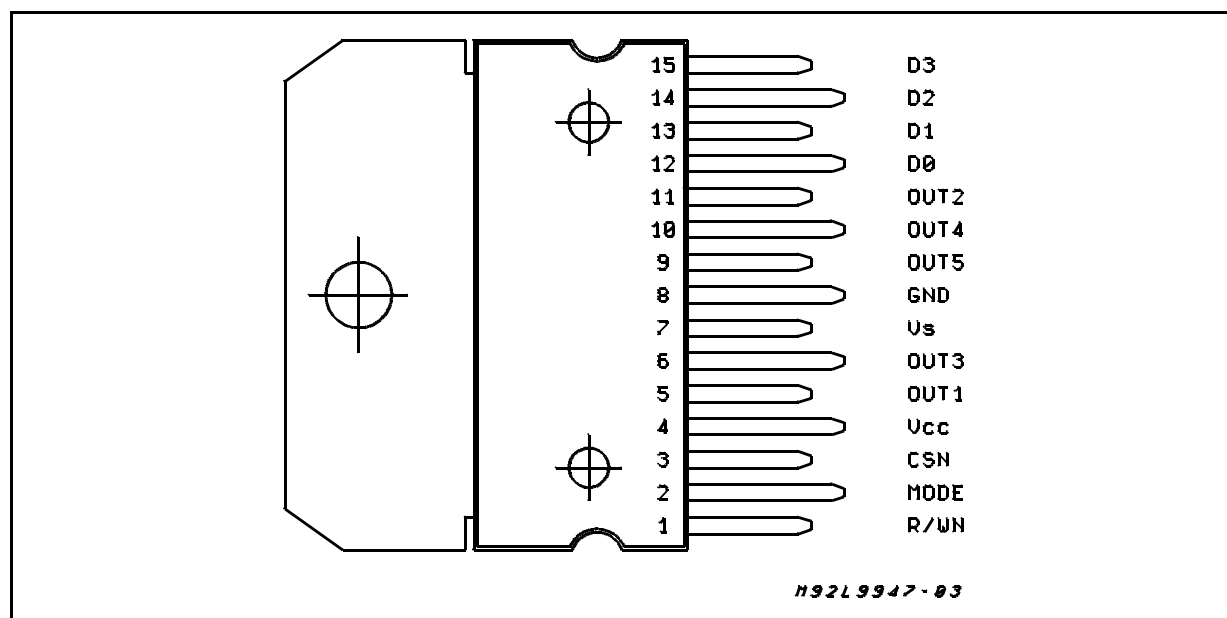
### BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_S$	DC Supply Voltage	26	V
	Single Pulse $t_{max} < 400ms$	40	V
$I_S$	Negative Supply Current	-9	A
$V_{CC}$	Stabilized Supply Voltage	-0.3 to 6V	V
$V_{CSN}, V_{R/WN}, V_{MODE}$	Digital Input Voltage	-0.3 to $V_{CC}+0.3$	V
$V_{D0-D3}$	Digital Input/ Output Voltage	-0.3 to $V_{CC}+0.3$	V
$I_{OUT1-OUT5}$	Output Current Power	internal limited	
$T_j$	Operating Junction Temperature	-40 to 150	°C
$T_j - SD$	Thermal Shutdown Junction Temperature	min 150	°C
$T_j - HYS$	Thermal Junction Temperature Hysteresis	20	K

## PIN CONNECTION



## THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th j-amb}$	Thermal Resistance Junction Ambient $P_{tot} = 25W$ ; free air; DC	38	°C/W
$Z_{th j-amb}$	Thermal Resistance Junction Ambient still air; single pulse $t_p = 20s$	10	°C/W

**ELECTRICAL CHARACTERISTICS** ( $V_S = 8$  to  $16V$ ;  $V_{CC} = 4.5$  to  $5.5V$ ;  $T_j = -40$  to  $150^\circ C$ ; unless otherwise specified; the voltage are referred to GND and currents are assumed positive, when the current flows into the pin.)

**SUPPLY:**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$I_{CC}$	DC Supply Current	$V_S = 16V$ ; $V_{CC} = 5.5V$ ; (status 8)		5		mA
$I_S$	DC Supply Current	$V_S = 16V$ ; $V_{CC} = 5.5V$ ; (status 8)		10		mA
$I_{CC} + I_S$	Sum Supply Current <sup>(1)</sup>	$I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0$ ; Standby (status 2) $V_S = 14V$ ; $V_{CC} = 5.5V$ ; $T_j = -40$ to $25^\circ C$			100	$\mu A$
		$I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{OUT4} = I_{OUT5} = 0$ ; Standby (status 2) $V_S = 14V$ ; $V_{CC} = 5.5V$ ; $T_j > 25^\circ C$			150	$\mu A$
		$V_S < 14V$ ; $V_{CC} = 5.5V$ ; $I_{OUT} = 0$ ; (status 17);			3	mA
$V_{SOVT}$	Overvoltage Shutdown Threshold		17		25	V

**CONTROL INPUTS: CNS, R/WN, MODE**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{INL}$	Input Low Level	$V_{CC} = 5V$			1.5	V
$V_{INH}$	Input High Level	$V_{CC} = 5V$	3.5			V
$V_{INHyst}$	Input Hysteresis	$V_{CC} = 5V$ ;	0.5			V
$I_{INL}$	Input Current Low	$V_{CC} = 5V$ ; $V_{IN} = 0$	-10		10	$\mu A$
$I_{INH}$	Input Current High (with exception of CSN Input)	$V_{CC} = 5V$ ; $V_{IN} = 5V$	-10		10	$\mu A$
$R_{CSN}$	Input Resistance to GND (pull down at CSN pin)		20			K $\Omega$

**DATA INPUT: D0 - D3**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{DINL}$	Input Low Level	$V_{CC} = 5V$ ; $MODE = 0$			1.5	V
$V_{DINH}$	Input High Level	$V_{CC} = 5V$ ; $MODE = 0$	3.5			V
$V_{DINHyst}$	Input Hysteresis	$V_{CC} = 5V$ ; $MODE = 0$	0.5			V
$I_{DINL}$	Input Current Low	$V_{CC} = 5V$ ; $V_{IN} = 0$	-10		10	$\mu A$
$I_{DINH}$	Input Current High	$V_{CC} = 5V$ ; $V_{IN} = 5V$	-10		10	$\mu A$

**DATA OUTPUT: D0 - D3**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{DOL}$	Output Low Level	$V_{CC} = 5V$ ; $I_D = 0.5mA$ ; $MODE = 1$			0.6	V
$V_{DINH}$	Input High Level	$V_{CC} = 5V$ ; $I_D = 0.5mA$ ; $MODE = 1$	4			V

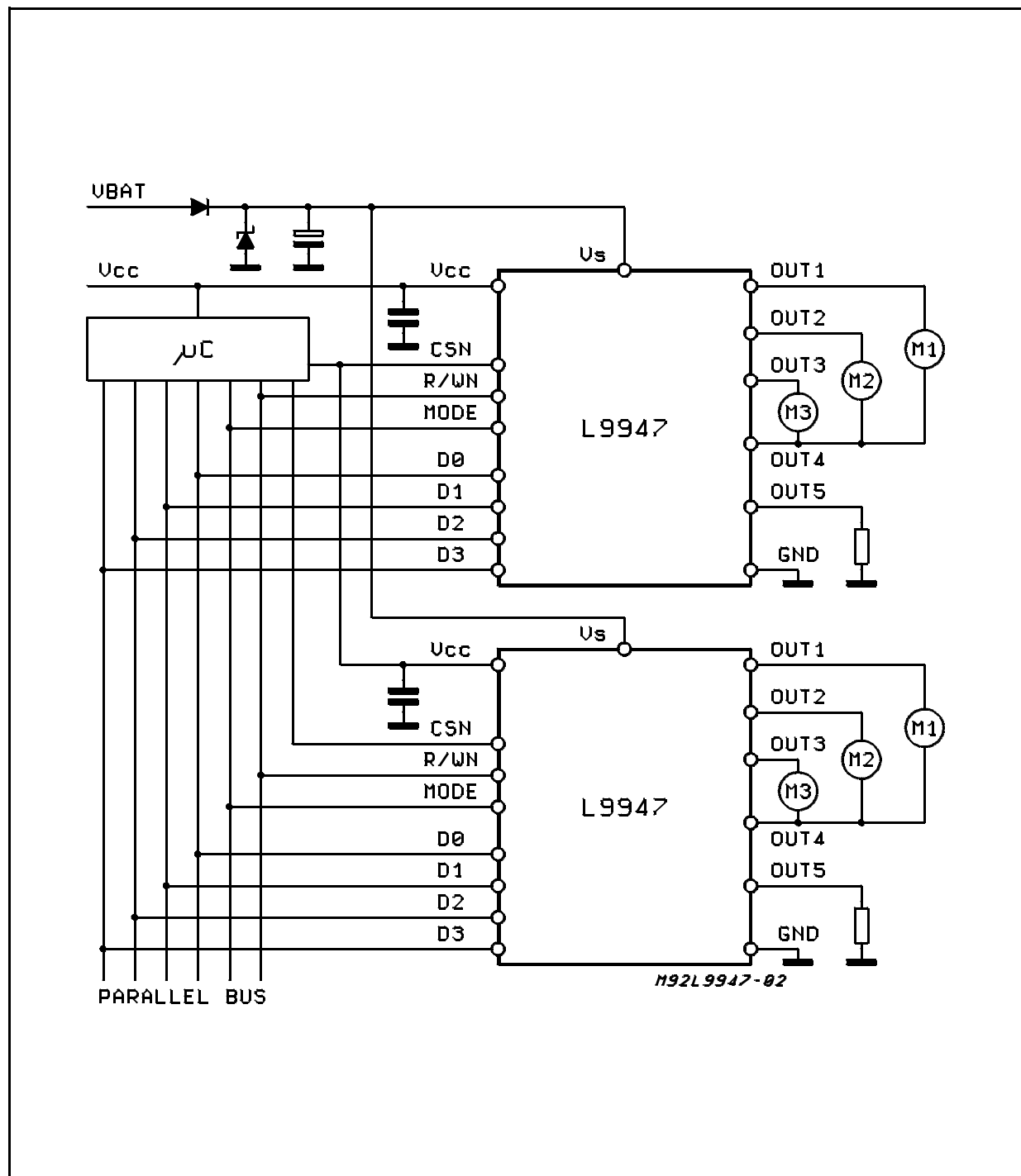
Note (1): Off-State Leakage Current of each single output  $\leq 25\mu A$ ,  $T_j = -40$  to  $150^\circ C$ .

**ELECTRICAL CHARACTERISTICS** (continued)**OUTPUTS:**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
RON OUT1	On Resistance to Supply or GND	$V_S = 8V; T_j = 125^\circ C; I_{OUT} = \pm 0.5A$			6	$\Omega$
		$V_S \geq 10V; T_j = 125^\circ C; I_{OUT} = \pm 0.5A$			3.95	$\Omega$
RON OUT2	On Resistance to Supply or GND	$V_S = 8V; T_j = 125^\circ C; I_{OUT} = \pm 0.5A$			6	$\Omega$
		$V_S \geq 10V; T_j = 125^\circ C; I_{OUT} = \pm 0.5A$			3.95	$\Omega$
RON OUT3	On Resistance to Supply or GND	$V_S = 8V; T_j = 125^\circ C; I_{OUT} = \pm 2.5A$			600	m $\Omega$
		$V_S \geq 10V; T_j = 125^\circ C; I_{OUT} = \pm 2.5A$			395	m $\Omega$
RON OUT4	On Resistance to Supply or GND	$V_S = 8V; T_j = 125^\circ C; I_{OUT} = \pm 2.5A$			600	m $\Omega$
		$V_S \geq 10V; T_j = 125^\circ C; I_{OUT} = \pm 2.5A$			395	m $\Omega$
RON OUT5	On Resistance to Supply	$V_S = 8V; T_j = 125^\circ C; I_{OUT} = -2A$			1.0	$\Omega$
		$V_S \geq 10V; T_j = 125^\circ C; I_{OUT} = -2A$			0.7	$\Omega$
$ I_{OUT1} $	Output Current Limitation to Supply or GND	For the function of the short circuit current limitation see the functional description (pag....)	0.67		2	A
$ I_{OUT2} $	Output Current Limitation to Supply or GND		0.67		2	A
$ I_{OUT3} $	Output Current Limitation to Supply or GND		4		12	A
$ I_{OUT4} $	Output Current Limitation to Supply or GND		4		12	A
$ I_{OUT5} $	Output Current Limitation to GND		2.5		7.5	A
$I_{OUT1}$	Output Current	$V_{OUT1} = 2.5V; (\text{status } 18)$	5		15	mA
$I_{OUT2}$	Output Current	$V_{OUT2} = 2.5V; (\text{status } 18)$	5		15	mA
$I_{OUT3}$	Output Current	$V_{OUT3} = 2.5V; (\text{status } 18)$	5		15	mA
$I_{OUT4}$	Output Current	$V_{OUT4} = 2.5V; (\text{status } 17)$	80		500	mA
		$V_{OUT4} = V_S - 2.5V; (\text{status } 16 \text{ or } 18)$	-80		-500	mA
$I_{OUT5}$	Output Current	$V_{OUT5} = V_S - 2.5V; (\text{status } 18)$	-5		-15	mA
VOUT1-5	Output Voltage Detection Thresholds	$V_S = 13V; (\text{status } 11)$				
		LOW	4.9	0.4 $V_S$	5.5	V
		HIGH	7.5	0.6 $V_S$	8.1	V
T <sub>JOT</sub>	Overtemperature Detection Thresholds	HYSTERESIS				V
		status 12 - 15		130		$^\circ C$
		steady state $t > 20ms$	125		$< T_{JSD}$	$^\circ C$
t <sub>isc</sub>	Overcurrent Switch off Time		50			$\mu s$
f <sub>osc</sub>	Internal Oscillator Frequency			250		KHz

## APPLICATION CIRCUIT DIAGRAM

Figure 1: Recommended Application Circuit.














## FUNCTIONAL DESCRIPTION

The L9947 is a power interface circuit designed for a multiplex system controlled by a parallel μC bus. The bus consists of four bidirectional data wires D0 - D3 and three control wires read/write (R/WN), mode (MODE) and chip select (CSN).

The device needs two supply voltages. The first voltage supplies the half bridges, high side driver and its driving part. The second one is a 5V stabilized supply. The function of the device in the typical operating modes is described in the following tables.

Output Activating/write Table 1

Status	CSN	R/WN	MODE	D0	D1	D2	D3	OUT1	OUT2	OUT3	OUT4	OUT5	FUNCTION	
1	1	X	X	X	X	X	X	AB	AB	AB	AB	AB	Hold output behaviours as programmed before	
2		0	0	0	0	0	0	T	T	T	T	T	All Outputs, Standby mode	
3		0	0	0	0	1	0	SRC	T	T	SNK	T	M1, right	
4		0	0	1	1	0	0	SNK	T	T	SRC	T	M1, left	
5		0	0	1	0	1	0	T	SRC	T	SNK	T	M2, right	
6		0	0	0	1	0	0	T	SNK	T	SRC	T	M2, left	
7		0	0	0	1	1	0	T	T	SRC	SNK	T	M3, right	
8		0	0		0	0	0	T	T	SNK	SRC	T	M3, left	
9		0	0		1	1	1	0	SNK	SNK	SNK	SNK	T	Braking
10		0	0	0	0	0	1	T	T	T	T	SRC	High side driver	






**Notes:**

Where CSN = 0 the device is (for  $t \leq 100\mu s$ ) transparent, in this condition any change of Data D0 .... D3 will lead to the appropriate output response.

Deselecting the circuit (CSN ) the last programmed status will be stored.




**Diagnostic / read. Table 2:**

In readout modes the port D0 .... D3 is acting as an output showing the conditions detected before.


Status	CSN	R/WN	MODE	D0	D1	D2	D3	Function
11		1	0	OUT1	OUT2	OUT3	OUT4	OUT1, OUT2, OUT3, OUT4;
12		1	1	0	0	OT	OUT5	• No failure, OT, OUT5;
13		1	1	1	0	OT	OUT5	• OVC1, OT, OUT5;
14		1	1	0	1	OT	OUT5	• OVC2, OT, OUT5;
15		1	1	1	1	OT	OUT5	OVC or OVC1 or OVC2 OT, OUT5;

**Diagnostic / write. Table 3:**

Diagnostic modes are used to check the load status for broken or shorted wires.

Status	CSN	R/WN	MODE	D0	D1	D2	D3	OUT1	OUT2	OUT3	OUT4	OUT5	Function
16		0	1	0	1	0	X	T	T	T	140mA SRC	T	
17		0	1	1	0	0	X	T	T	T	140mA SNK	T	$I_s + I_{cc} \leq 1mA$ for $I_{OUT4} = 0$
18		0	1	0	1	1	X	10mA SNK	10mA SNK	10mA SNK	140mA SRC	10mA SRC	


**Standby and clear / write. Table 4:**

Status	CSN	R/WN	MODE	D0	D1	D2	D3	OUT1	OUT2	OUT3	OUT4	OUT5	Function
19		0	0	1	1	1	1	T	T	T	T	T	Clear
20	0	X	X	X	X	X	X	T	T	T	T	T	Clear, Static CSN = 0 will force clear status and standby after $100\mu s$ without respect of data inputs

**Symbols:**

1: Logic High  
0: Logic Low  
T: Tristate  
X: Don't care

AB: As before

 Low pulse  $t < 100\mu s$

SRC: Source

SNK: Sink

OT: Overtemperature

OVC1: Overcurrent 1

OVC2: Overcurrent 2

OVV: Overvoltage

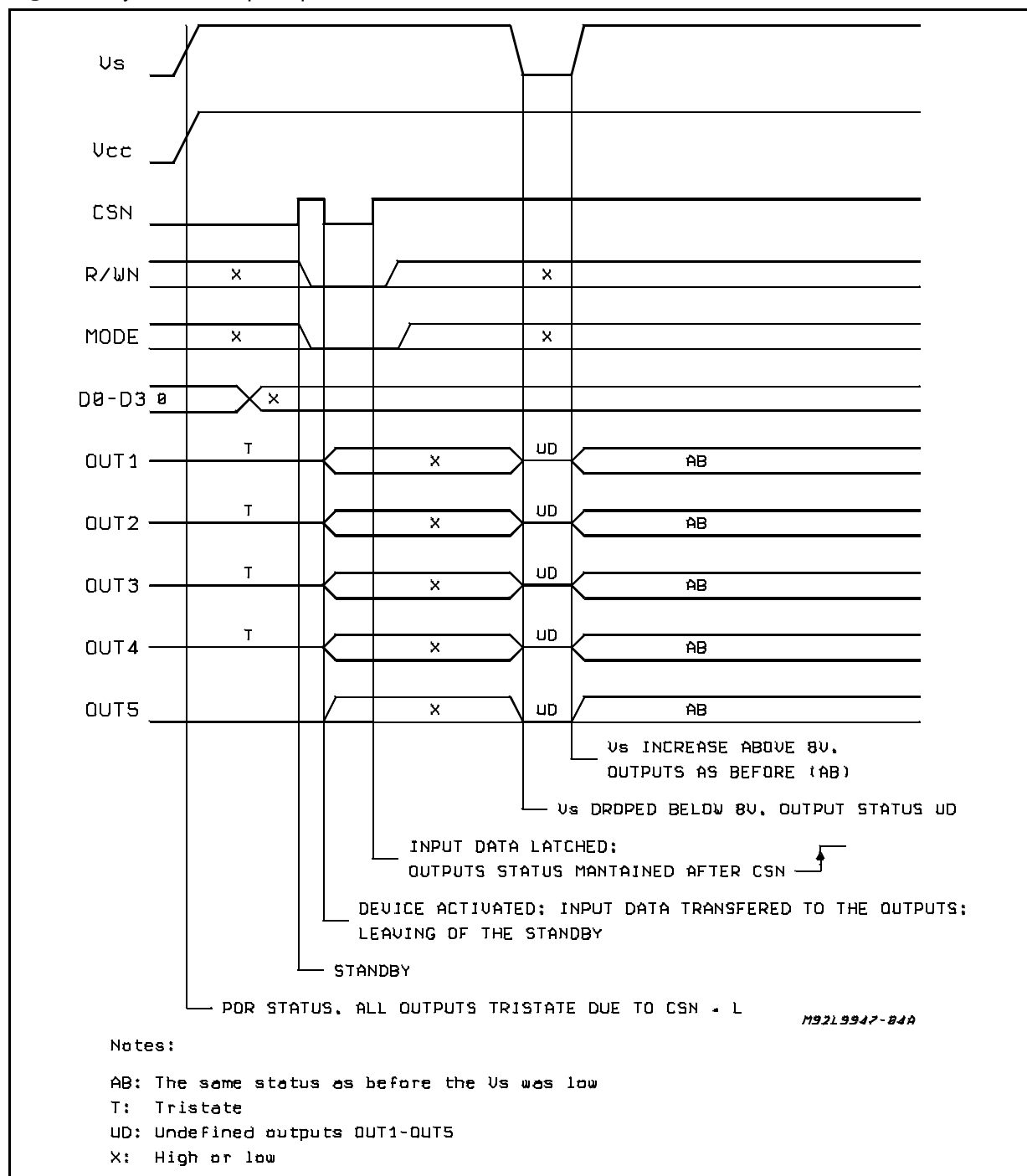
OUTX:

- High if output voltage

was  $> 0.6V_s$  during test

- Low if output voltage

was  $< 0.4V_s$  during test

**Figure 2: System Startup Sequence****SYSTEM STARTUP (figure 2)**

It is not mandatory that Vs is present before Vcc. With the presence of the Vcc the internal logic would be reseted and the system restarts under control of the inputs. If CSN = 0 for more than 100µs after the presence of Vcc the standby mode is activated. Standby is also activated when the CSN and VCC would be high at the same

time. When CSN = 0 and Vcc goes up, the device is not controlled by the bus. The outputs remain in tristate but the current consumption is larger than 100µA. A high - low - signal at the CSN - wire is mandatory to control the outputs. There is no undervoltage detection level for the supply voltage VS implemented. The VCC should be supplied from the same voltage supply as the driver of the D0 -D3 pins (eg. µC).

### DATA TRANSFER AND OUTPUTS ACTIVATING (Figure 3)

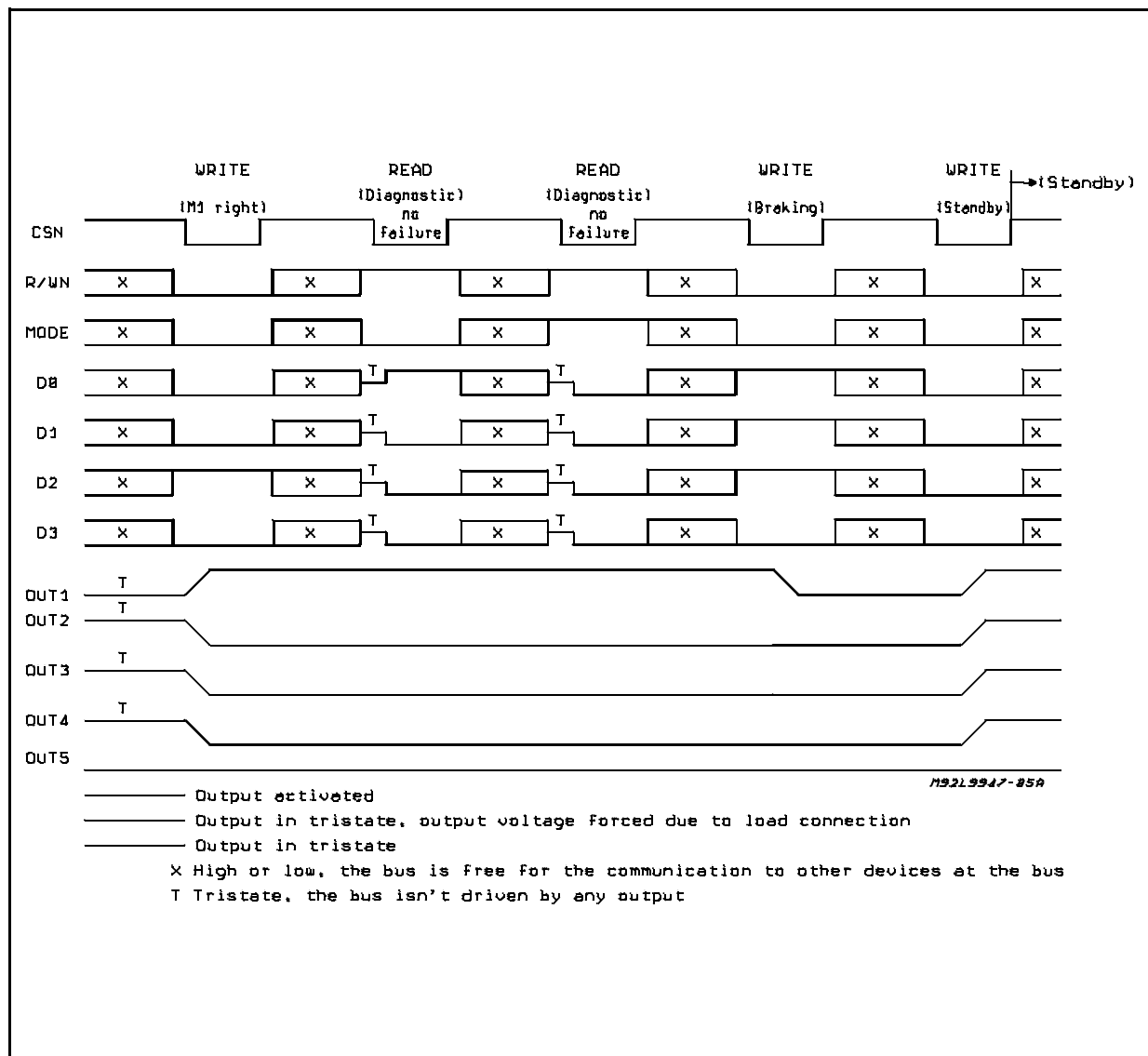
The half bridges of OUT1, OUT2 and OUT3 can be used with OUT4 to drive three bidirectional motors in full bridge configuration as shown in fig.1 Only one motor can be driven in the same time. The  $\mu$ C writes the corresponding word status 1 till 10 at the bus and latch it with a low pulse in the L9947. So the motor is activated. To stop the motor it is useful to insert a braking phase (status 9). In the braking condition there are all low side DMOS of the half bridges switched-on in this case the flyback currents flows through the low side switches instead of the intrinsic diodes of the half bridges. After that, the half bridges could be switched in tristate (T). The high side driver, OUT5 can be switched only when all

the half bridges are in tristate status 10.

The  $\mu$ C works always as master and the L9947 Power Interface as slave. That means: the  $\mu$ C starts the communication between the Power Interface and itself with low transition at the CSN line. CSN = 0, R/WN= 0 the L9947 reads the data at the bus and execute the command as shown in tables 1,3,4 (write mode). The high slope of the CSN stores the last command and execute it further. All inputs are disabled if CSN= 1.

So the bus can be used for another device. With CSN = 0 and R/WN = 1 the L9947 writes the status of the diagnostic at the parallel bus until CSN becomes high (table 2; status  $\mu + 15$ ) (read mode). The power outputs maintain the same status as before.

**Figure 3:** Signal sequence for data transfer to switch M1 right, read the output status, brake the motor and activate the standby mode.





**Bus Timing** (figure 4)

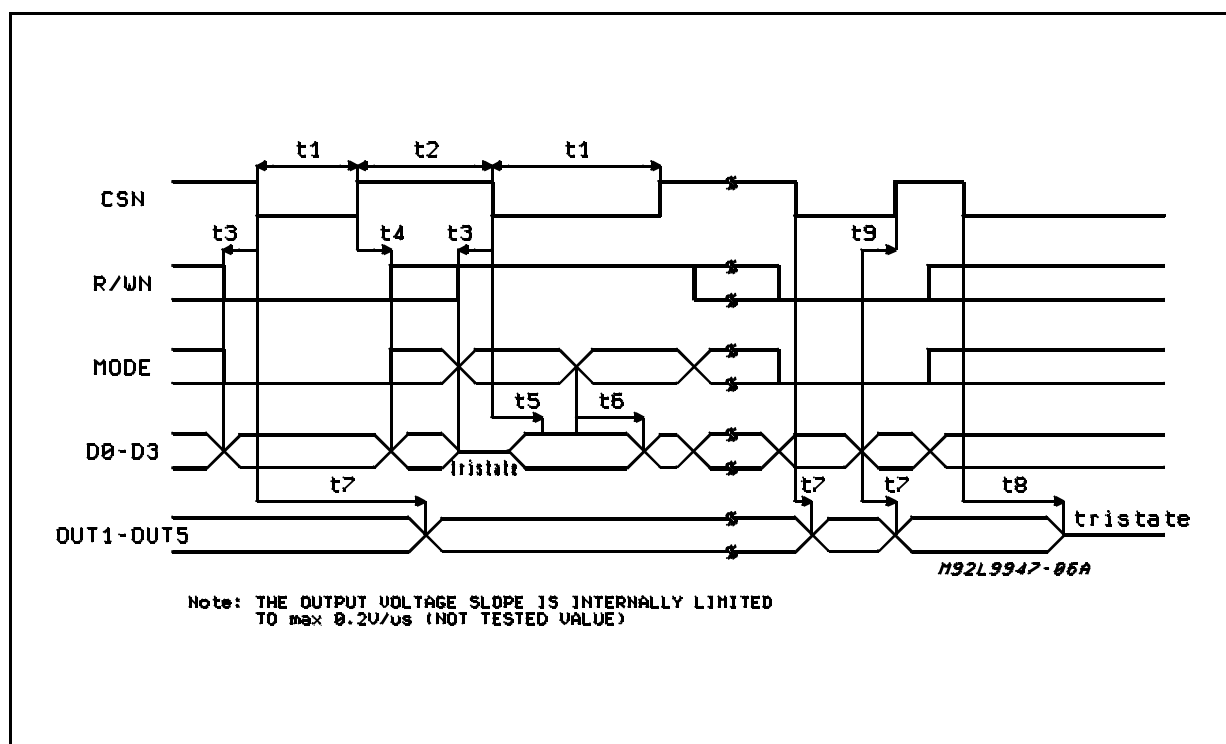
The bus signal must be defined  $t_3 = 1\mu\text{s}$  before CSN goes low. It is allowed to change the level of R/WN during CSN = 0. The other signals could be changed. To store a command it is mandatory to fix the D0 - D3 and MODE signals  $t_9 = 1\mu\text{s}$  before the positive edge of CSN.

**OVERCURRENT AT OUT1 - OUT5:**

The output currents of OUT1 - OUT5 are internally limited. This is realized in the following way:

When the output current reaches a certain level (see pag...) the Gate - Source voltage will be clamped to a lower level. The output current is now limited and follows the output ID, UDS characteristic for this Gate - Source voltage. An internal timer starts when the output voltage drop (Drain - Source) increases above 0.4Vs.

After 100 $\mu\text{s}$  typ. the output is switched OFF and the corresponding overcurrent bit (OVC1 or OVC2) will be set. The outputs can be activated again with the next input data word.

**Figure 4:** Bus and Outputs Timing Diagram**TIMING CHARACTERISTICS**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$t_1$	Width of CSN Low	20		90*	$\mu\text{s}$
$t_2$	Width of CSN High	10			$\mu\text{s}$
$t_3$	Input Signals Before Negative Edge of CSN	1			$\mu\text{s}$
$t_4$	Input Signals After Positive Edge of CSN	1			$\mu\text{s}$
$t_5$	Valid Diagnostic Data			10	$\mu\text{s}$
$t_6$	Valid Diagnostic Data			10	$\mu\text{s}$
$t_7$	Delay Time from Input to Power Output, $V_S = 13\text{V}$			300	$\mu\text{s}$
$t_8$	CSN = Low Duration (Pulse Length) for CLEAR of latched Data	100			$\mu\text{s}$
$t_9$	Input Data Before Positive Edge of CSN Which Should be Latched	1			$\mu\text{s}$

$t_1$  and  $t_5$  are derived from the internal oscillator frequency

$t_7$  varies with the supply voltage  $V_S$ , relating to the output voltage slope limitation

(\*) for  $t_1 \geq 100\mu\text{s}$  the latched data will be reseted due to CLEAR (status 20)

**Diagnostic** (TABLE 2; STATUS 11 - 15):

The diagnostic delivers the information of the output voltage status (high or low) at the outputs OUT1 - OUT5, overcurrent, overvoltage shutdown and over temperature. The output voltage detection is done by hysteresis comparators with thresholds at 0.4VS and 0.6 VS. The overcurrent (OVC) information is latched till a new or repeated write command was received. The OVC1 is set to high with the overcurrent condition at any of the half-bridge outputs. OVC2 error bit will be set with the overcurrent condition at OUT5. The overvoltage (OVV) is high till the supply voltage Vs exceeds the overvoltage threshold of 20V typ. The overtemperature (OT) is high if the junction temperature is less than typ. 30 Kevin below the thermal shutdown junction temperature (TJSD).

**Detection of Load Interruption** (TABLE 3):

The outputs OUT1 - OUT4 are connected by the motors in the application. The output OUT4 can be switched as current source or sink with typ. 140mA current capability (status 16 + 17). The sum of current consumption is <1mA if the output current IOUT4 = 0 (status 17). The diagnostic of the output voltage delivers the information if one or more of the half bridges is shorted to Vs or GND or the motor connections are interrupted. In status 18 the outputs OUT1 - OUT3 are switched as current sinks (typ. 10mA), OUT4 and OUT5 as current sources (OUT4 140mA, OUT5 10mA). With this current the influence of leakage currents and oxidized contacts is eliminated.

**Standby** (TABLE 1; STATUS 2):

The L9947 is set in standby mode with the positive edge of CSN when all other inputs are low. All latched data will be cleared and the inputs and outputs are in tristate. The total current consumption is less than 100µA. CSN=0 quits the standby. All latched data are cleared.

**Clear** (TABLE 4; STATUS 20):

If the chip select is low for ore than  $T_{CLR} = 100\mu s$ , the internal latched data will be cleared and the outputs become tristate. Repetitive high low edges activate the inputs again. Also a broken CSN-wire activates this clear function due to the internal pull down resistor at CSN input. After a clear, the L9947 goes in standby and can be

wake up with a negative edge of CSN.

**Thermal Shutdown:**

When the junction temperature increases above TJSD the power DMOS transistors are switched off until the junction temperature drops below the value TJSD - TJHYST.

**Clamp Current of The Power Outputs:**

For output voltages 10V and larger a clamp current of appr. 50µA will flow in the power outputs due to the internal gate-source voltage limitation, when the device is not in standby.

**Overvoltage Shutdown:**

When the supply voltage VS exceeds the overvoltage threshold VsQVT, typ. 20V, the outputs OUT1 - OUT5 go in tristate condition. If the supply voltage goes under the overvoltage shutdown threshold, the status is the same as before the overvoltage condition occurred.

**Undervoltage:**

In the voltage range  $2V < V_{CC} < 4V$  the internal logic is reseted and all outputs go in tristate. Also ground spikes on the VCC reset the logic. After an internal reset of the logic, the L9947 is controlled again by the inputs.

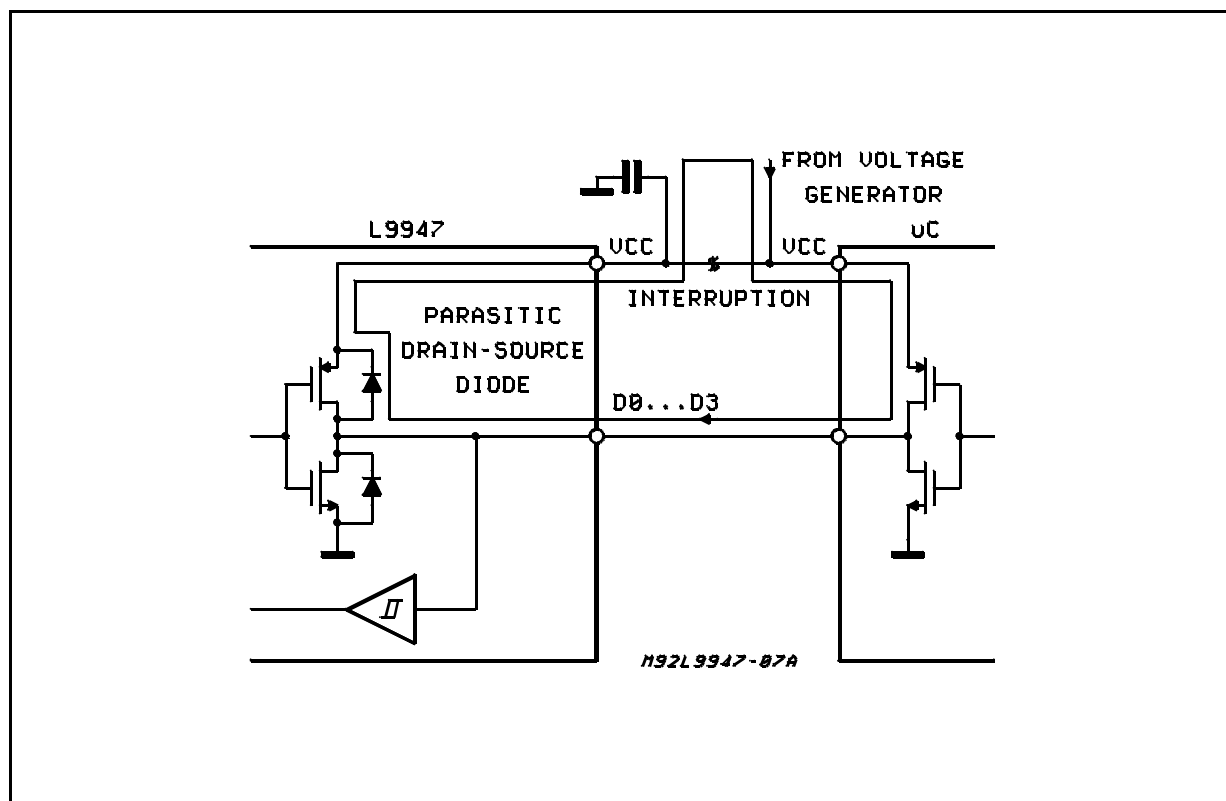
**Ground Interrupt:**

The L9947 is protected against interruption. The output OUT5 switches off at ground interruption. The outputs OUT1 - OUT4 are driven in full bridge configuration as shown in the application. There is no path through the load or direct to another ground. Thus, the device protected.

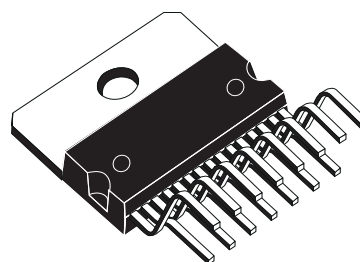
**VCC Interruption**

If the supply voltage Vs is present and VCC is interrupted or not supplied, than two cases can be distinguished:

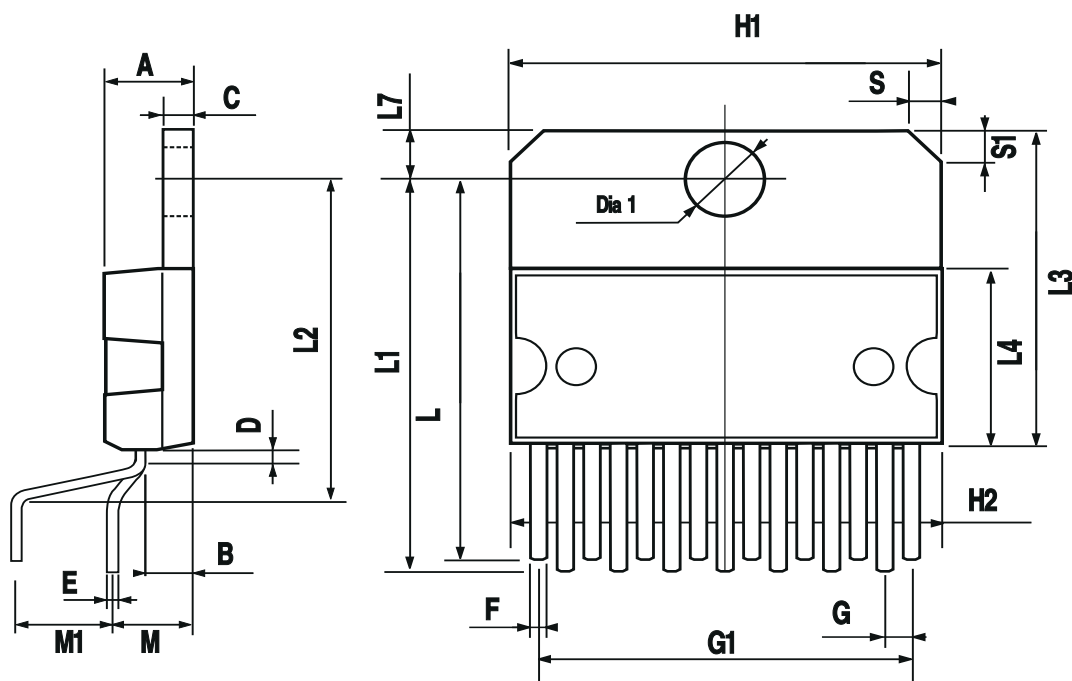
- 1 The data pins D0 - D3 are not driven by the µC or they are low. So the outputs OUT1 - OUT5 and D0 - D3 are in tristate.
- 2 One of the pins D0 - D3 is driven high the µC. This pin supplies the VCC pin by the drain-bulk-diode of the p-channel mos (fig.5). Depending of the CSN, R/WN and MODE inputs some undesirable functions can occur.

**Figure 5:** Supply Current Path at Vcc Interruption

## OUTLINE AND MECHANICAL DATA



## Multiwatt15 V



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