

## LOW DROP VOLTAGE REGULATOR

### 1 FEATURES

- OPERATING DC SUPPLY VOLTAGE RANGE  
5.6V TO 31V
- LOW QUIESCENT CURRENT  
(6 $\mu$ A Typ. @ 25°C with Enable Low)
- HIGH PRECISION OUTPUT VOLTAGE (2%)
- LOW DROPOUT VOLTAGE LESS THAN 0.5V
- RESET CIRCUIT SENSING THE OUTPUT  
VOLTAGE DOWN TO 1V
- PROGRAMMABLE RESET PULSE DELAY  
WITH EXTERNAL CAPACITOR
- WATCHDOG
- PROGRAMMABLE WATCHDOG TIMER WITH  
EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT  
CIRCUIT PROTECTION
- AUTOMOTIVE TEMPERATURE RANGE  
(T<sub>j</sub> = -40°C TO 150°C)
- ENABLE INPUT FOR ENABLING/DISABLING  
THE VOLTAGE REGULATOR OUTPUT

Figure 1. Packages

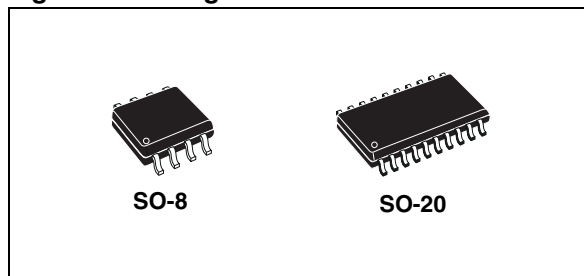
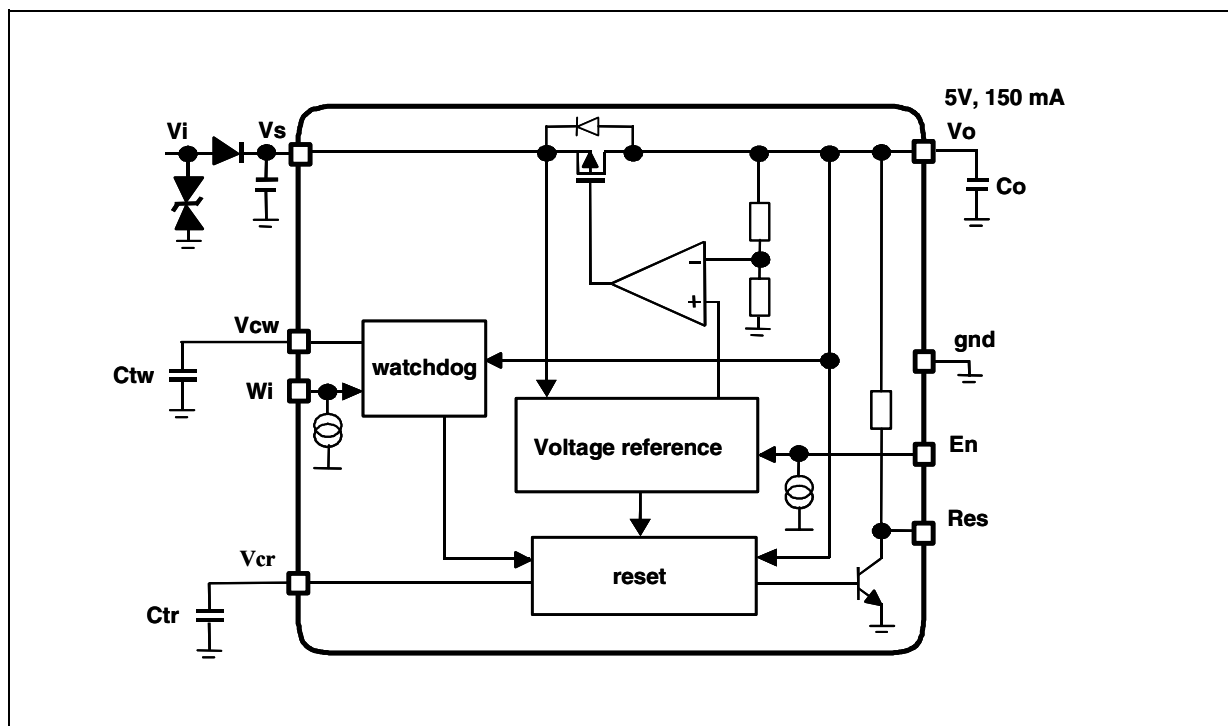


Table 1. Order Codes

Part Number	Package
L4979D	SO-8
L4979MD	SO-20
L4979D013TR	SO-8 in Tape & Reel
L4979MD013TR	SO-20 in Tape & Reel

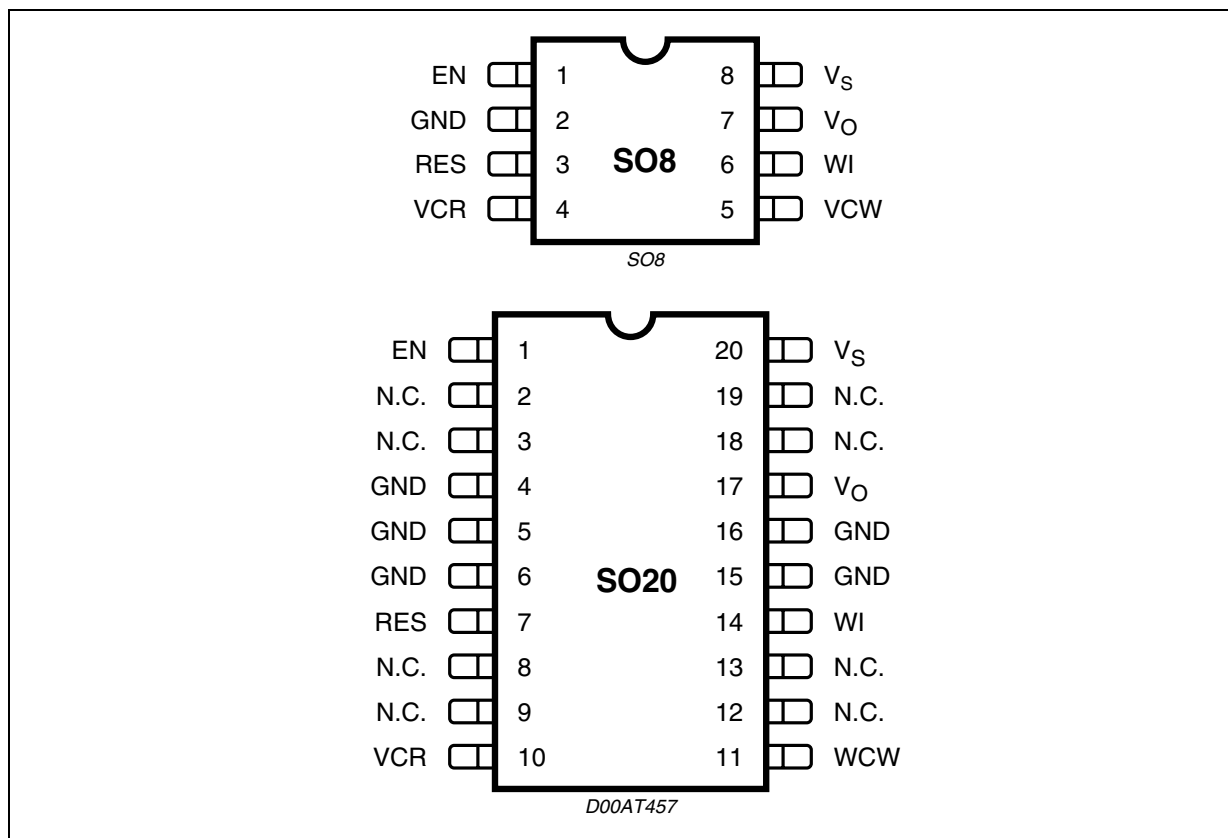
Figure 2. Block Diagram



**Table 2. Pin Function**

SO8 N°	SO20 N°	Pin Name	Function
1	1	En	Enable input If high, regulator, watchdog and reset are operating. If low, regulator, watchdog and reset are shut down.
2	4	gnd	Ground reference
	5,6,15,16	gnd	Ground These pins are to be connected to a heat spreader electrically grounded
3	7	Res	Reset output. It is pulled down when output voltage drops below Vo_th or frequency at Wi is too low.
4	10	Vcr	Reset timing adjust A capacitor between Vcr pin and gnd sets the reset delay time (trd)
5	11	Vcw	Watchdog timer adjust A capacitor between Vcw pin and gnd sets the time response of the watchdog monitor.
6	14	Wi	Watchdog input. If the frequency at this input pin is too low, the Reset output is activated.
7	17	Vo	Voltage regulator output Output capacitor >100nF is needed for regulator stability
8	20	Vs	Supply voltage Supply capacitor (e.g. 200nF) is needed for regulator stability.
	2, 3, 8, 9, 12, 13, 18, 19	N. C.	not connected

**Figure 3. Pins Connection (Top view)**



**Table 3. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
Vvsdc	DC supply voltage	-0.3 to 40	V
lvsc	Input current	internally limited	
Vvo	DC output voltage	-0.3 to 6	V
Ivo	DC output current	internally limited	
Vwi	Watchdog input voltage	-0.3 to $V_{VO} + 0.3$	V
Vod	Open drain output voltage (RES)	-0.3 to $V_{VO} + 0.3$	V
Iod	Open drain output current (RES)	internally limited	
Vcr	Reset delay voltage	-0.3 to $V_{VO} + 0.3$	V
Vcw	Watchdog delay voltage	-0.3 to $V_{VO} + 0.3$	V
Ven	Enable input voltage	-0.3 to 40	V
Tj	Junction temperature	-40 to 150	°C
VESD	ESD voltage level (HBM-MIL STD 883C)	±2	kV

Note: 1. Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

**Table 4. Thermal Data**

Symbol	Parameter	SO8	SO16+2+2	Unit
$R_{th\ j-amb}$	Thermal resistance Junction to Ambient	130 to 180	50 to 80	°C/W

**Table 5. Electrical Characteristics**

( $V_S = 5.6V$  to  $31V$ ,  $T_J = -40^\circ C$  to  $+150^\circ C$  unless otherwise specified)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>GENERAL</b>							
$V_S, V_O$	$I_q$	Quiescent current	$V_S = 13.5V, I_o = 150mA$ , enable high all I/O currents=0		1.5	3	mA
$V_S, V_O$	$I_q$	Quiescent current	$V_S = 13.5V, I_o = 0mA$ , enable high all I/O currents = 0		100	200	μA
$V_S, V_O$	$I_q$	Quiescent current	$V_S = 13.5V, I_o = 0mA$ , enable low all I/O currents = 0		6	20	μA
	$T_w$	Thermal protection temperature		150		190	°C
	$T_{w\_hy}$	Thermal protection temperature hysteresis			10		°C

Table 5: Electrical Characteristics (continued)

Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>VOLTAGE REGULATOR</b>							
V <sub>o</sub>	V <sub>o_ref</sub>	Output voltage	V <sub>s</sub> = 5.6 to 31V I <sub>o</sub> = 1 to 150mA	4.90	5.00	5.10	V
V <sub>o</sub>	I <sub>short</sub>	Output short circuit current <sup>(1)</sup>	V <sub>s</sub> = 13.5V	150	280	400	mA
V <sub>o</sub>	I <sub>lim</sub>	Output current limitation <sup>(1)</sup>	V <sub>s</sub> = 13.5V	150	320	500	mA
V <sub>s</sub> , V <sub>o</sub>	V <sub>line</sub>	Line regulation voltage	V <sub>s</sub> = 5.6 to 31V I <sub>o</sub> = 1 to 150mA			25	mV
V <sub>o</sub>	V <sub>load</sub>	Load regulation voltage	I <sub>o</sub> = 1 to 150mA			25	mV
V <sub>s</sub> , V <sub>o</sub>	V <sub>dp</sub>	Drop voltage	I <sub>o</sub> = 150mA		200	400	mV
V <sub>s</sub> , V <sub>o</sub>	SVR	Ripple rejection <sup>(2)</sup>	f <sub>r</sub> = 100 Hz	55			dB
<b>RESET</b>							
R <sub>es</sub>	V <sub>res_l</sub>	Reset output low voltage	R <sub>ext</sub> = 5kΩ to V <sub>o</sub> , V <sub>o</sub> > 1V			0.4	V
R <sub>es</sub>	I <sub>res_h</sub>	Reset output high leakage current	V <sub>res</sub> = 5V			1	μA
R <sub>es</sub>	R <sub>p_u</sub>	Internal Pull up resistance	with respect to V <sub>o</sub>	12	25	50	kΩ
R <sub>es</sub>	V <sub>o_th</sub>	Reset threshold voltage	V <sub>s</sub> = 5.6 to 31V I <sub>o</sub> = 1 to 150mA	6% below V <sub>o_ref</sub>	8% below V <sub>o_ref</sub>	10% below V <sub>o_ref</sub>	
V <sub>cr</sub>	V <sub>rhth</sub>	Reset timing high threshold	V <sub>s</sub> = 13.5V	44% V <sub>o_ref</sub>	47% V <sub>o_ref</sub>	50% V <sub>o_ref</sub>	
V <sub>cr</sub>	V <sub>rlth</sub>	Reset timing low threshold	V <sub>s</sub> = 13.5V	10% V <sub>o_ref</sub>	13% V <sub>o_ref</sub>	16% V <sub>o_ref</sub>	
V <sub>cr</sub>	I <sub>cr</sub>	Charge current	V <sub>s</sub> = 13.5V	8	17	30	μA
V <sub>cr</sub>	I <sub>dr</sub>	Discharge current	V <sub>s</sub> = 13.5V	8	17	30	μA
R <sub>es</sub>	t <sub>rr_2</sub>	Reset delay time <sup>(3)</sup>	V <sub>o</sub> = V <sub>o_th</sub> -100mV	100	250	700	μs
R <sub>es</sub>	t <sub>rd</sub>	Reset pulse delay	V <sub>s</sub> = 13.5V, C <sub>tr</sub> = 1nF	65		150	ms
<b>WATCHDOG</b>							
W <sub>i</sub>	V <sub>ih</sub>	Input high voltage	V <sub>s</sub> = 13.5V	3.5			V
W <sub>i</sub>	V <sub>il</sub>	Input low voltage	V <sub>s</sub> = 13.5V			1.5	V
W <sub>i</sub>	V <sub>ih</sub>	Input hysteresis	V <sub>s</sub> = 13.5V		300		mV
W <sub>i</sub>	I <sub>i</sub>	Pull down current	V <sub>s</sub> = 13.5V		10	20	μA
V <sub>cw</sub>	V <sub>whth</sub>	High threshold	V <sub>s</sub> = 13.5V	2.20	2.35	2.50	V
V <sub>cw</sub>	V <sub>wlth</sub>	Low threshold	V <sub>s</sub> = 13.5V	0.50	0.65	0.80	V

## ELECTRICAL CHARACTERISTICS (continued)

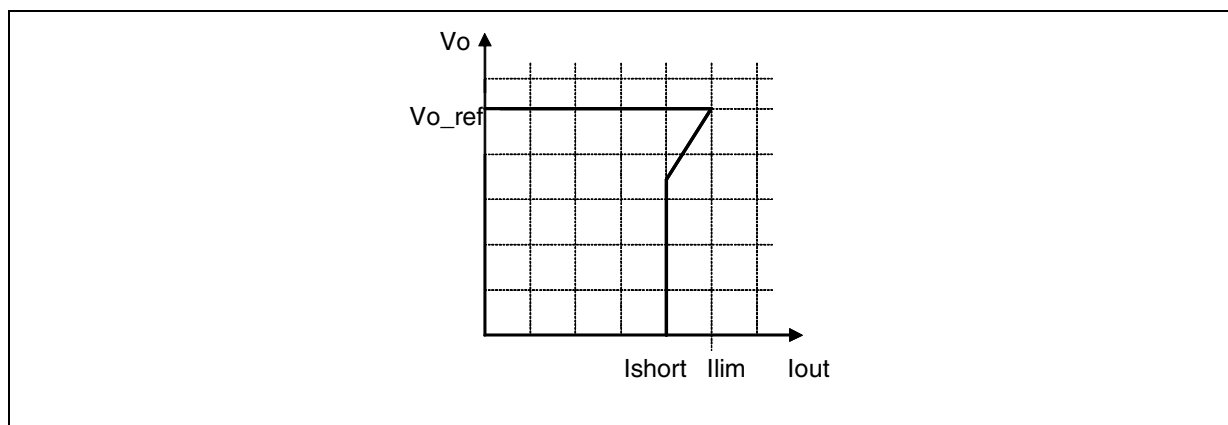
Pin	Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V <sub>cw</sub>	I <sub>cwc</sub>	Charge current	V <sub>s</sub> = 13.5V, V <sub>cw</sub> = 0.1V	4	7.5	14	μA
V <sub>cw</sub>	I <sub>cwd</sub>	Discharge current	V <sub>s</sub> = 13.5V, V <sub>cw</sub> = 2.5V	1.0	2.4	4.5	μA
V <sub>cw</sub>	T <sub>wop</sub>	Watchdog period	V <sub>s</sub> = 13.5V, C <sub>tw</sub> = 47nF	25	50	90	ms
R <sub>es</sub>	t <sub>wol</sub>	Watchdog output low time	V <sub>s</sub> = 13.5V, C <sub>tw</sub> = 47nF	6	10	22	ms
<b>ENABLE</b>							
E <sub>n</sub>	V <sub>en_l</sub>	Enable input low voltage				1	V
E <sub>n</sub>	V <sub>en_h</sub>	Enable input high voltage		3			V
E <sub>n</sub>	V <sub>en_hy</sub>	Enable input hysteresis		700	1000	1100	mV
E <sub>n</sub>	I <sub>leak</sub>	Pull down current	E <sub>n</sub> = 5V	2	10	20	μA

Note: 1. see fig4 (behavior of output current versus regulated voltage Vo)  
 2. guaranteed by design  
 3. When Vo becomes lower than 4V, the reset reaction time decreases down to 2μs assuring a faster reset condition in this particular case.

## 2 VOLTAGE REGULATOR

The voltage regulator uses a p-channel MOS transistor as a regulating element. With this structure a low drop-out voltage at current up to 150mA is achieved. The output voltage is regulated up to transient input supply voltage of 40V. No functional interruption due to over-voltage pulses is generated. The high precision of the output voltage is obtained with a pre-trimmed reference voltage. A short circuit protection to GND is provided.

Figure 4. Behavior of output current versus regulated voltage Vo (see a.m. Note 1)



## 3 RESET

The reset circuit monitors the output voltage  $V_o$ . If the output voltage drops below  $V_{o\_th}$  then  $R_{es}$  becomes low with a delay time  $t_{rr}$ . Real  $t_{rr}$  value changes as a non-linear function of  $\Delta(V_{o\_th} - V_o)$ . The reset low signal is guaranteed for an output voltage  $V_o$  greater than 1V.

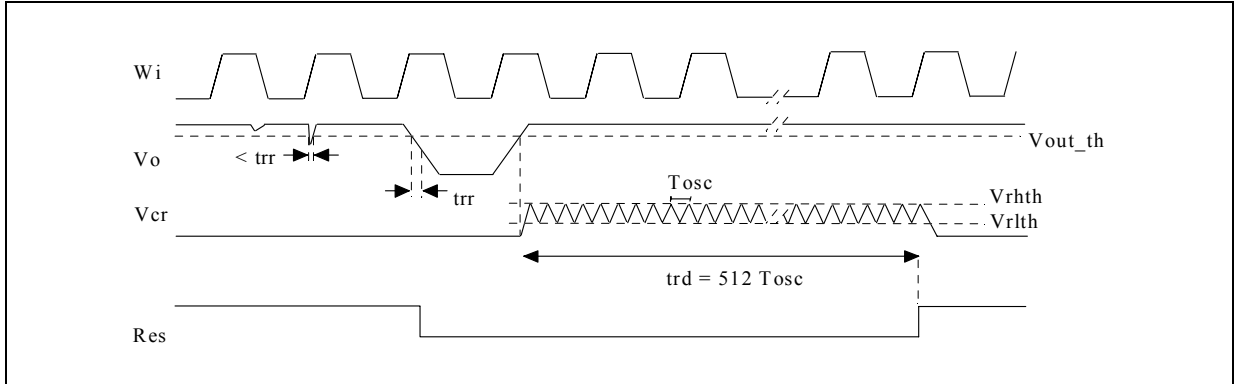
When the output voltage becomes higher than  $V_{o\_th}$  then  $R_{es}$  goes high with a delay  $t_{rd}$ . This delay is obtained by 512 periods of an oscillator (see fig. 5). The oscillator period is given by:

$$T_{osc} = \frac{[(V_{rth} - V_{rlth}) \cdot C_{tr}]}{I_{cr}} + \frac{[(V_{rth} - V_{rlth}) \cdot C_{tr}]}{I_{dr}}$$

and reset pulse delay  $t_{rd}$  is given by:

$$t_{rd} = 512 \times T_{osc}$$

**Figure 5. Reset Time Diagram.**



## 4 WATCHDOG

The watchdog input  $W_i$  monitors a connected microcontroller. If pulses are missing, the reset output  $Res$  is set to low. The pulse sequence time can be set within a wide range through the external capacitor  $C_{tw}$ . The watchdog circuit discharges the capacitor  $C_{tw}$  with the constant current  $I_{cwd}$ . If the lower threshold  $V_{wlth}$  is reached, a watchdog reset is generated. To prevent this reset, the microcontroller must generate a positive edge during the discharge of the capacitor before the voltage has reached the threshold  $V_{wlth}$ . In order to calculate the minimum time  $T_{dis}$  during which the microcontroller must generate the positive edge, the following equation can be used:

$$(V_{whth} - V_{wlth}) \times C_{tw} = I_{cwd} \times T_{dis}$$

Each  $W_i$  positive edge switches the current source from discharging to charging; the same happens when the lower  $V_{wlth}$  threshold is reached. When the voltage reaches the upper threshold  $V_{whth}$  the current switches from charging to discharging. The result is a saw tooth voltage at the watchdog timer capacitor  $C_{tw}$ .

**Figure 6. Watchdog time diagram**

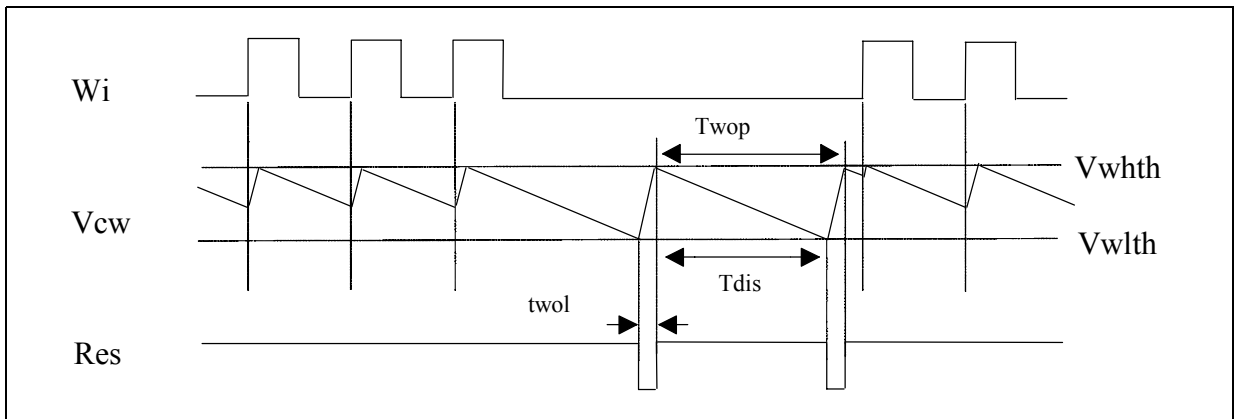
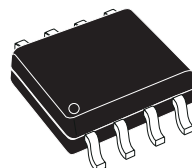


Figure 7. SO-8 Mechanical Data &amp; Package Dimensions

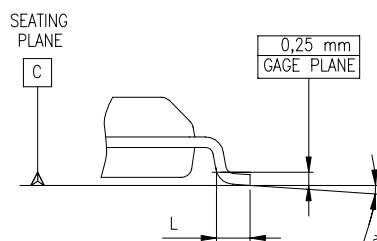
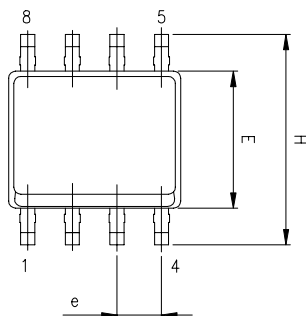
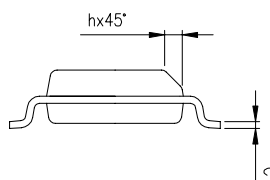
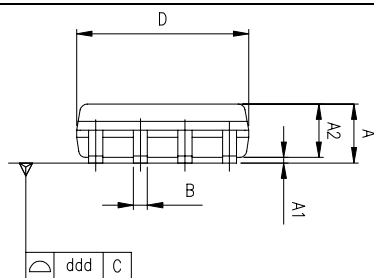
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

Note: (1) Dimensions D does not include mold flash, protrusions or gate burrs.  
Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

## OUTLINE AND MECHANICAL DATA



## SO-8



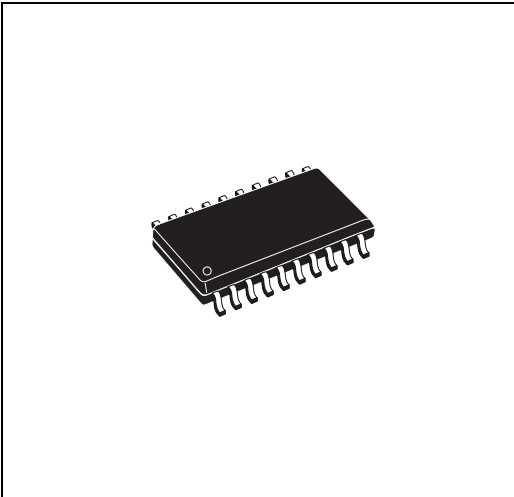
0016023 C

Figure 8. SO-20 Mechanical Data & Package Dimensions

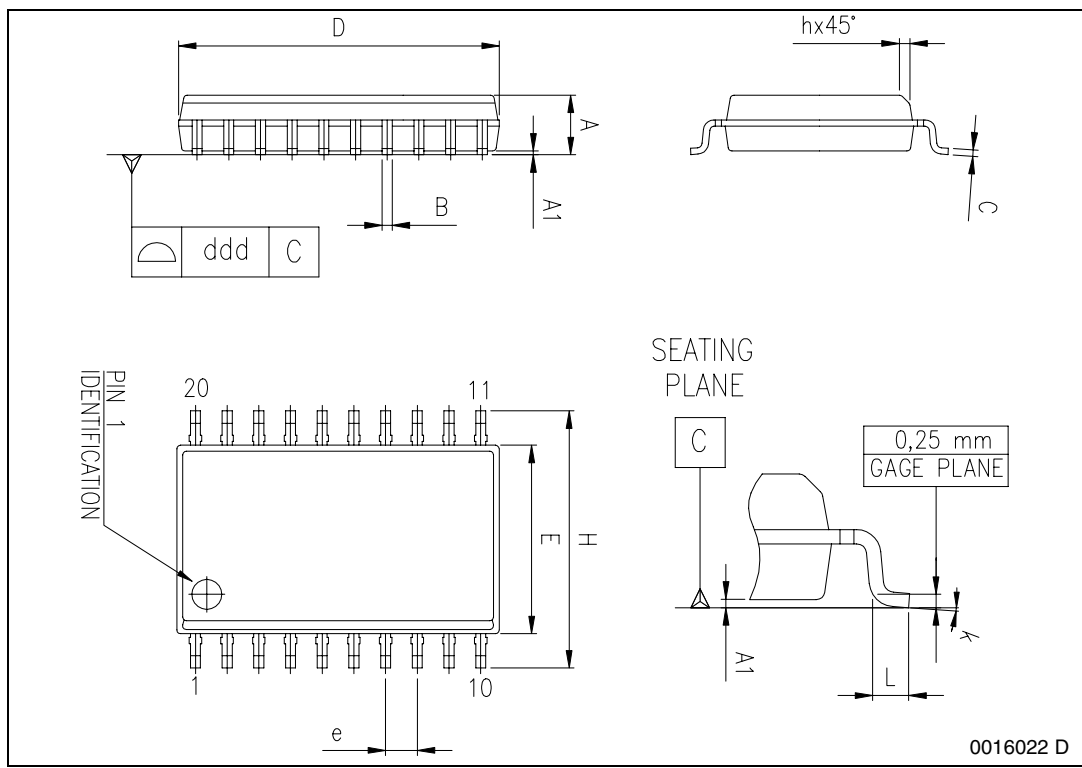
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

**OUTLINE AND MECHANICAL DATA**



**SO20**



0016022 D



**Table 6. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
June 2004	3	Changed the values of the parameter "Reset timing high/low threshold.
July 2004	4	Pin Connection SO-20 changed. Changed some textes in the Features and table 2. Changed some values in the tables 3, 4 and 5. Changed some textes in the sections 2, 3 and 4.
October 2004	5	Changed from Product Preview to final datasheet.
February 2006	6	Modified the orderable part numbers for Tape & Reel.

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