16-BIT, 600-kHz, FULLY DIFFERENTIAL PSEUDO-BIPOLAR INPUT, MICROPOWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH SERIAL INTERFACE AND REFERENCE

FEATURES

- **600-kHz Sample Rate**
- **±0.35 LSB Typ, ±0.75 LSB Max INL**
- **±0.25 LSB Typ, ±0.5 LSB Max DNL**
- **16-Bit NMC**
- **SINAD 93.5 dB, SFDR 120 dB at f_i = 1 kHz**
- **High-Speed Serial Interface up to 40 MHz**
- **Onboard Reference Buffer**
- **Onboard 4.096-V Reference**
- **Pseudo-Bipolar Input, up to ±4.2 V**
- **Onboard Conversion Clock**
- **Zero Latency**
- **Wide Digital Supply**
- **Low Power**
  - **110 mW at 600 kHz**
  - **15 mW During Nap Mode**
  - **10 µW During Power Down**
- **28-Pin 6 × 6 QFN Package**
- **Pin Compatible With 18-Bit ADS8382**

APPLICATIONS

- **Medical Instruments**
- **Optical Networking**
- **Transducer Interface**
- **High Accuracy Data Acquisition Systems**
- **Magnetometers**

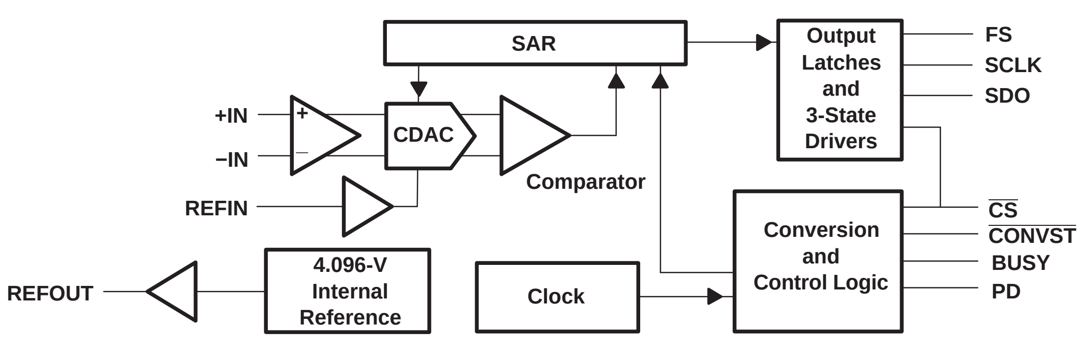
DESCRIPTION

The ADS8372 is a high performance 16-bit, 600-kHz A/D converter with fully differential, pseudo-bipolar input. The device includes an 16-bit capacitor-based SAR A/D converter with inherent sample and hold. The ADS8372 offers a high-speed CMOS serial interface with clock speeds up to 40 MHz.

The ADS8372 is available in a 28 lead 6 × 6 QFN package and is characterized over the industrial –40°C to 85°C temperature range.

High Speed SAR Converter Family

Type/Speed	500 kHz	~ 600 kHz	750 kHZ	1 MHz	1.25 MHz	2 MHz	3 MHz	4 MHz
18-Bit Pseudo-Diff	ADS8383	ADS8381						
		ADS8380 (S)						
18-Bit Pseudo-Bipolar, Fully Diff		ADS8382 (S)						
16-Bit Pseudo-Diff		ADS8370 (S)	ADS8371		ADS8401/05	ADS8411		
16-Bit Pseudo-Bipolar, Fully Diff		ADS8372 (S)			ADS8402/06	ADS8412		
14-Bit Pseudo-Diff					ADS7890 (S)		ADS7891	
12-Bit Pseudo-Diff				ADS7886				ADS7881



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8372I	±1.5	±1	16	28 Pin 6×6 QFN	RHP	-40°C to 85°C	ADS8372IRHPT	Small Tape and Reel 250
							ADS8372IRHPR	Tape and Reel 2500
ADS8372IB	±0.75	±0.5	16	28 Pin 6×6 QFN	RHP	-40°C to 85°C	ADS8372IBRHPT	Small Tape and Reel 250
							ADS8372IBRHPR	Tape and Reel 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Voltage	+IN to AGND	–0.3 V to +VA + 0.3 V
	–IN to AGND	–0.3 V to +VA + 0.3 V
	+VA to AGND	–0.3 V to 6 V
	+VBD to BDGND	–0.3 V to 6 V
Digital input voltage to BDGND		–0.3 V to +VBD + 0.3 V
Digital input voltage to +VA		+0.3 V
Operating free-air temperature range, T_A		–40°C to 85°C
Storage temperature range, T_{stg}		–65°C to 150°C
Junction temperature (T_J max)		150°C
QFN package	Power dissipation	$(T_J \max - T_A)/\theta_{JA}$
	θ_{JA} thermal impedance	86°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

At –40°C to 85°C, +VA = +5 V, +VBD = +5 V or +VBD = +2.7 V, using internal or external reference, f_{SAMPLE} = 600 kHz, unless otherwise noted. (All performance parameters are valid only after device has properly resumed from power down, Table 2.)

	PARAMETER	TEST CONDITIONS	ADS8372IB			ADS8372I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT									
	Full-scale input voltage(1)	+IN – (–IN)	$-V_{ref}$		V_{ref}	$-V_{ref}$		V_{ref}	V
	Absolute input voltage	+IN	–0.2		V_{ref} + 0.2	–0.2		V_{ref} + 0.2	V
		–IN	–0.2		V_{ref} + 0.2	–0.2		V_{ref} + 0.2	
	Input common mode range		(V_{ref}/2) –0.2		(V_{ref}/2) +0.2	(V_{ref}/2) –0.2		(V_{ref}/2) +0.2	V
	Sampling capacitance (measured between +IN to AGND and -IN to AGND)			40			40		pF
	Input leakage current			1			1		nA
SYSTEM PERFORMANCE									
	Resolution			16			16		Bits
	No missing codes		16			16			Bits
INL	Integral linearity(2)(3)(4)	Quiet zones observed	0.75	±0.35	0.75	–1.5		1.5	LSB (16 bit)
		Quiet zones not observed		±0.75					
DNL	Differential linearity(3)	Quiet zones observed	–0.5	±0.25	0.5	–1		1	LSB (16 bit)
		Quiet zones not observed		±0.5					
E_O	Offset error(3)		–0.75	±0.25	0.75	–1.5		1.5	mV
	Offset temperature drift (3)			±0.2			±0.2		ppm/°C
E_G	Gain error(3)(5)		–0.075		0.075	–0.15		0.15	%FS
	Gain error temperature drift(3)(5)			±1.5			±1.5		ppm/°C
CMRR	Common-mode rejection ratio	At DC		80			80		dB
		[+IN + (–IN)]/2 = 50 mV_{p-p} at 1 MHz + DC of V_{ref}/2		55			55		
	Noise	At 00000H output code		40			40		µV RMS
PSRR	DC Power supply rejection ratio	At 10000H output code		55			55		dB
SAMPLING DYNAMICS									
	Conversion time		1.0		1.16	1.0		1.16	µs
	Acquisition time		0.5			0.5			µs
	Throughput rate				600			600	kHz
	Aperture delay			10			10		ns
	Aperture jitter			12			12		ps RMS
	Step response	(6)		400			400		ns
	Overvoltage recovery			400			400		ns

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Measured using analog input circuit in Figure 52 and digital stimulus in Figure 56 and Figure 57 and reference voltage of 4.096 V.
(4) This is endpoint INL, not best fit.
(5) Measured using external reference source so does not include internal reference voltage error or drift.
(6) Defined as sampling time necessary to settle an initial error of 2Vref on the sampling capacitor to a final error of 1 LSB at 16-bit level. Measured using the input circuit in Figure 52.

SPECIFICATIONS (continued)

At –40°C to 85°C, +VA = +5 V, +VBD = +5 V or +VBD = +2.7 V, using internal or external reference, f_{SAMPLE} = 600 kHz, unless otherwise noted. (All performance parameters are valid only after device has properly resumed from power down, Table 2.)

PARAMETER		TEST CONDITIONS	ADS8372IB MIN	ADS8372IB TYP	ADS8372IB MAX	ADS8372I MIN	ADS8372I TYP	ADS8372I MAX	UNIT
DYNAMIC CHARACTERISTICS									
THD	Total harmonic distortion (7) (8)	VIN = 8 V_{p-p} at 1 kHz		–116	–106		–116		dB
		VIN = 8 V_{p-p} at 10 kHz		–115			–115		
		VIN = 8 V_{p-p} at 100 kHz		–98			–98		
SNR	Signal-to-noise ratio (7)	VIN = 8 V_{p-p} at 1 kHz	92	93.5			93.5		dB
		VIN = 8 V_{p-p} at 10 kHz		93.5			93.5		
		VIN = 8 V_{p-p} at 100 kHz		92			92		
SINAD	Signal-to-noise + distortion (7) (8)	VIN = 8 V_{p-p} at 1 kHz	92	93.5			93.5		dB
		VIN = 8 V_{p-p} at 10 kHz		93.5			93.5		
		VIN = 8 V_{p-p} at 100 kHz		91			91		
SFDR	Spurious free dynamic range (7)	VIN = 8 V_{p-p} at 1 kHz		120			120		dB
		VIN = 8 V_{p-p} at 10 kHz		120			120		
		VIN = 8 V_{p-p} at 100 kHz		99			99		
	–3dB Small signal bandwidth			75			75		MHz
REFERENCE INPUT									
V_{ref}	Reference voltage input range		2.5	4.096	4.2	2.5	4.096	4.2	V
	Resistance (9)			10			10		MΩ
INTERNAL REFERENCE OUTPUT									
V_{ref}	Reference voltage range	IOUT = 0 A, T_A = 30°C	4.088	4.096	4.104	4.088	4.096	4.104	V
	Source current	Static load			10			10	µA
	Line regulation	+VA = 4.75 V to 5.25 V		2.5			2.5		mV
	Drift	IOUT = 0 A		25			25		ppm/°C
DIGITAL INPUT/OUTPUT									
	Logic family CMOS								
V_{IH}	High level input voltage		+VBD – 1		+VBD + 0.3	+VBD – 1		+VBD + 0.3	V
V_{IL}	Low level input voltage		–0.3		0.8	–0.3		0.8	V
V_{OH}	High level output voltage	I_{OH} = 2 TTL loads	+VBD –0.6			+VBD –0.6			V
V_{OL}	Low level output voltage	I_{OL} = 2 TTL loads			0.4			0.4	V
	Data format 2's complement (MSB first)								
POWER SUPPLY REQUIREMENTS									
	Power supply voltage +VA		4.75	5	5.25	4.75	5	5.25	V
	Power supply voltage +VBD		2.7	3.3	5.25	2.7	3.3	5.25	V
I_{CC}	Supply current, 600-kHz sample rate (10)	+VA = 5 V		22	25		22	25	mA
POWER DOWN									
$I_{CC(PD)}$	Supply current, power down			2			2		µA
NAP MODE									
$I_{CC(NAP)}$	Supply current, nap mode			3			3		mA
	Power-up time from nap				300			300	ns
TEMPERATURE RANGE									
	Specified performance		–40		85	–40		85	°C

(7) Measured using analog input circuit in Figure 52 and digital stimulus in Figure 56 and Figure 57 and reference voltage of 4.096 V.
(8) Calculated on the first nine harmonics of the input frequency.
(9) Can vary +/-30%.
(10) This includes only +VA current. With +VBD = 5 V, +VBD current is typically 1 mA with a 10-pF load capacitance on the digital output pins.

TIMING REQUIREMENTS[(1)(2)(3)(4)(5)(6)]

PARAMETER		ADS8372I/ADS8372IB			UNIT	REF FIGURE
		MIN	TYP	MAX		
t_{conv}	Conversion time	1000		1160	ns	41– 44
t_{acq1}	Acquisition time in normal mode	0.5			µs	41,42,44
t_{acq2}	Acquisition time in nap mode ($t_{acq2} = t_{acq1} + t_{d18}$)	0.8			µs	43
CONVERSION AND SAMPLING						
t_{quiet1}	Quite sampling time (last toggle of interface signals to convert start command)[(6)]	30			ns	40 – 43, 45 – 47
t_{quiet2}	Quite sampling time (convert start command to first toggle of interface signals)[(6)]	10			ns	40 – 43, 45 – 47
t_{quiet3}	Quite conversion time (last toggle of interface signals to fall of BUSY)[(6)]	600			ns	40 – 43 45,47
t_{su1}	Setup time, $\overline{\text{CONVST}}$ before BUSY fall	15			ns	41
t_{su2}	Setup time, $\overline{\text{CS}}$ before BUSY fall (only for conversion/sampling control)	20			ns	40,41
t_{su4}	Setup time, $\overline{\text{CONVST}}$ before $\overline{\text{CS}}$ rise (so $\overline{\text{CONVST}}$ can be recognized)	5			ns	41,43,44
t_{h1}	Hold time, $\overline{\text{CS}}$ after BUSY fall (only for conversion/sampling control)	0			ns	41
t_{h3}	Hold time, $\overline{\text{CONVST}}$ after $\overline{\text{CS}}$ rise	7			ns	43
t_{h4}	Hold time, $\overline{\text{CONVST}}$ after $\overline{\text{CS}}$ fall (to ensure width of $\overline{\text{CONVST\_QUAL}}$)[(4)]	20			ns	42
t_{w1}	$\overline{\text{CONVST}}$ pulse duration	20			ns	43
t_{w2}	$\overline{\text{CS}}$ pulse duration	10			ns	41,42
t_{w5}	Pulse duration, time between conversion start command and conversion abort command to successfully abort the ongoing conversion			1000	ns	44
DATA READ OPERATION						
t_{cyc}	SCLK period	25			ns	45 – 47
	SCLK duty cycle	40%		60%		
t_{su5}	Setup time, $\overline{\text{CS}}$ fall before first SCLK fall	10			ns	45
t_{su6}	Setup time, $\overline{\text{CS}}$ fall before FS rise	7			ns	46,47
t_{su7}	Setup time, FS fall before first SCLK fall	7			ns	46,47
t_{h5}	Hold time, $\overline{\text{CS}}$ fall after SCLK fall	3			ns	45
t_{h6}	Hold time, FS fall after SCLK fall	7			ns	46,47
t_{su2}	Setup time, $\overline{\text{CS}}$ fall before BUSY fall (only for read control)	20			ns	40,45
t_{su3}	Setup time, FS fall before BUSY fall (only for read control)	20			ns	40,47
t_{h2}	Hold time, $\overline{\text{CS}}$ fall after BUSY fall (only for read control)	15			ns	40,45
t_{h8}	Hold time, FS fall after BUSY fall (only for read control)	15			ns	40,47
t_{w2}	$\overline{\text{CS}}$ pulse duration	10			ns	45
t_{w3}	FS pulse duration	10			ns	46,47
MISCELLANEOUS						
t_{w4}	PD pulse duration for reset and power down	60			ns	53,54
	All unspecified pulse durations	10			ns	

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) All specifications typical at –40°C to 85°C, +VA = +4.75 V to +5.25 V, +VBD = +2.7 V to +5.25 V.
(3) All digital output signals loaded with 10-pF capacitors.
(4) $\overline{\text{CONVST\_QUAL}}$ is $\overline{\text{CONVST}}$ latched by a low value on $\overline{\text{CS}}$ (see Figure 39).
(5) Reference figure indicated is only a representative of where the timing is applicable and is not exhaustive.
(6) Quiet time zones are for meeting performance and not functionality.

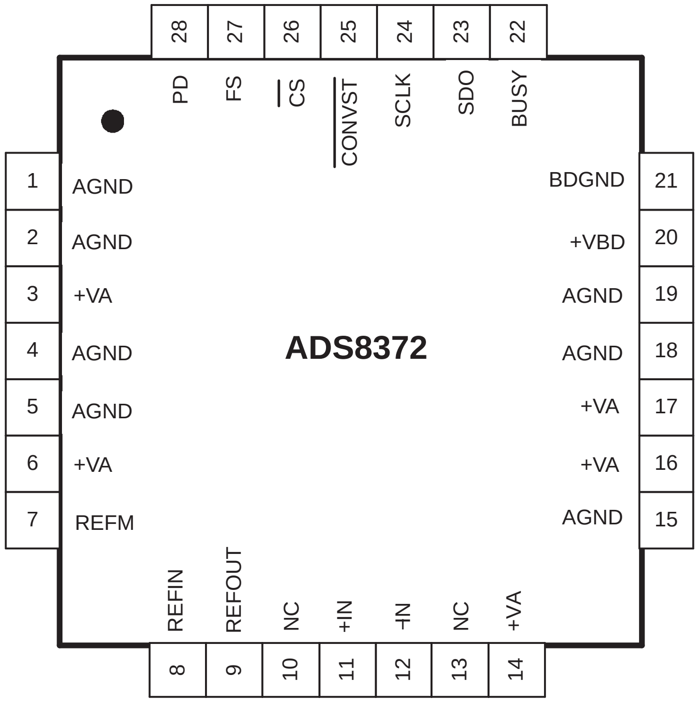
TIMING CHARACTERISTICS (1)(2)(3)(4)

Symbol	PARAMETER		ADS8372I/ADS8372IB MIN	TYP	MAX	UNIT	REF FIGURE
CONVERSION AND SAMPLING							
t_{d1}	Delay time, conversion start command to conversion start (aperture delay)				10	ns	41,43
t_{d2}	Delay time, conversion end to BUSY fall				5	ns	41 – 43
t_{d4}	Delay time, conversion start command to BUSY rise				20	ns	41
t_{d3}	Delay time, $\overline{\text{CONVST}}$ rise to sample start				5	ns	43
t_{d5}	Delay time, $\overline{\text{CS}}$ fall to sample start				10	ns	43
t_{d6}	Delay time, conversion abort command to BUSY fall				10	ns	44
DATA READ OPERATION							
t_{d12}	Delay time, $\overline{\text{CS}}$ fall to MSB valid		3		15	ns	45
t_{d15}	Delay time, FS rise to MSB valid		6		18	ns	46,47
t_{d7}	Delay time, BUSY fall to MSB valid (if FS is high when BUSY falls)				18	ns	47
t_{d13}	Delay time, SCLK rise to bit valid		2		10	ns	45 – 47
t_{d14}	Delay time, $\overline{\text{CS}}$ rise to SDO 3-state				6	ns	45
MISCELLANEOUS							
t_{d10}	Delay time, PD rise to SDO 3-state				55	ns	53,54
t_{d18}	Delay time, total device resume time	Nap mode			300	ns	55
		Full power down (external reference used with or without 1-µF‖0.1-µF capacitor on REFOUT)			t_{d11} + 2x conversions		54
		Full power down (internal reference used with or without 1-µF‖0.1-µF capacitor on REFOUT)			25 (4)	ms	53
t_{d11}	Delay time, untrimmed circuit full power-down resume time				1	ms	53,54
t_{d16}	Delay time, device power-down time	Nap		200		ns	55
		Full power down (internal/external reference used)		10		µs	53,54
t_{d17}	Delay time, trimmed internal reference settling (either by turning on supply or resuming from full power-down mode), with 1-µF‖0.1-µF capacitor on REFOUT				4	ms	53

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) All specifications typical at –40°C to 85°C, +VA = +4.75 V to +5.25 V, +VBD = +2.7 V to +5.25 V.
(3) All digital output signals loaded with 10-pF capacitors.
(4) Including t_{d11}, two conversions (time to cycle $\overline{\text{CONVST}}$ twice), and t_{d17}.

PIN ASSIGNMENTS

TOP VIEW



Note: The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

TERMINAL FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	1, 2, 4, 5, 15, 18, 19	–	Analog ground pins. AGND must be shorted to analog ground plane below the device.
BDGND	21	–	Digital ground for all digital inputs and outputs. BDGND must be shorted to the analog ground plane below the device.
BUSY	22	O	Status output. This pin is high when conversion is in progress.
$\overline{\text{CONVST}}$	25	I	Convert start. This signal is qualified with $\overline{\text{CS}}$ internally.
$\overline{\text{CS}}$	26	I	Chip select
FS	27	I	Frame sync. This signal is qualified with $\overline{\text{CS}}$ internally.
+IN	11	I	Noninverting analog input channel
–IN	12	I	Inverting analog input channel
NC	10, 13	–	No connection
PD	28	I	Power down. Device resets and powers down when this signal is high.
REFIN	8	I	Reference (positive) input. REFIN must be decoupled with REFM pin using 0.1-µF bypass capacitor and 1-µF storage capacitor.
REFM	7	I	Reference ground. To be connected to analog ground plane.
REFOUT	9	O	Internal reference output. Shorted to REFIN pin only when internal reference is used.
SCLK	24	I	Serial clock. Data is shifted onto SDO with the rising edge of this clock. This signal is qualified with $\overline{\text{CS}}$ internally.
SDO	23	O	Serial data out. All bits except MSB are shifted out at the rising edge of SCLK.
+VA	3, 6, 14, 16, 17	–	Analog power supplies
+VBD	20	–	Digital power supply for all digital inputs and outputs.

TYPICAL CHARACTERISTICS

SIGNAL-TO-NOISE RATIO
vs
REFERENCE VOLTAGE

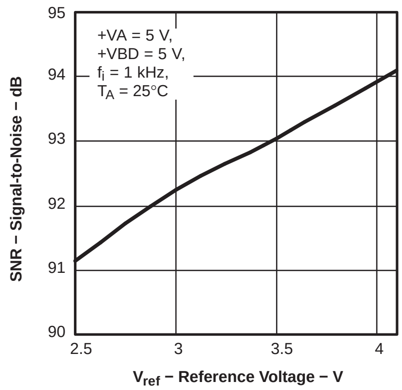


Figure 1.

SIGNAL-TO-NOISE
AND DISTORTION
vs
REFERENCE VOLTAGE

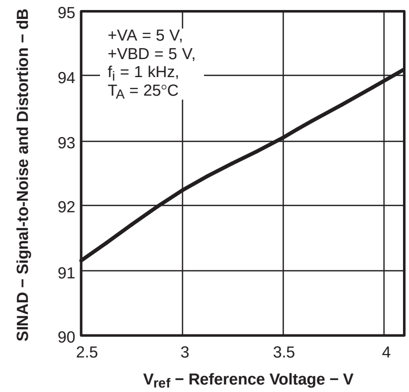


Figure 2.

SPURIOUS FREE DYNAMIC RANGE
vs
REFERENCE VOLTAGE

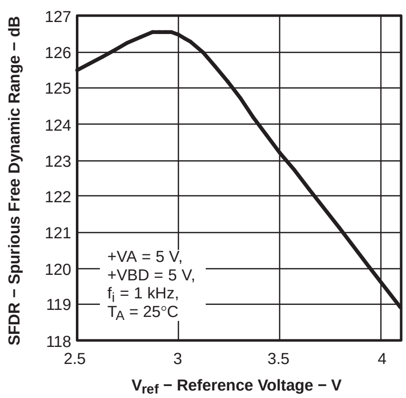


Figure 3.

TOTAL HARMONIC DISTORTION
vs
REFERENCE VOLTAGE

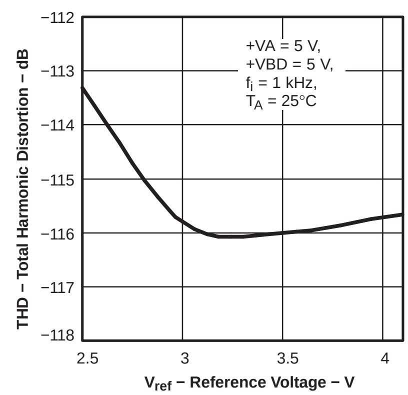


Figure 4.

EFFECTIVE NUMBER OF BITS
vs
REFERENCE VOLTAGE

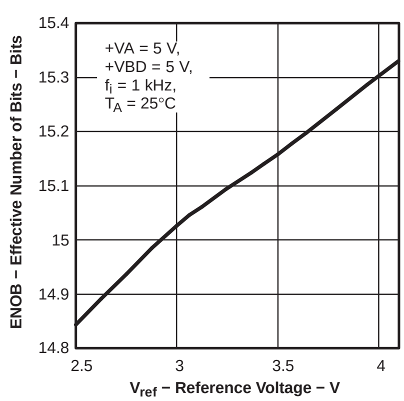


Figure 5.

EFFECTIVE NUMBER OF BITS
vs
FREE-AIR TEMPERATURE

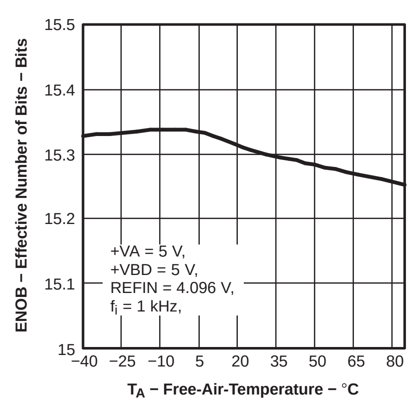


Figure 6.

TYPICAL CHARACTERISTICS (continued)

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

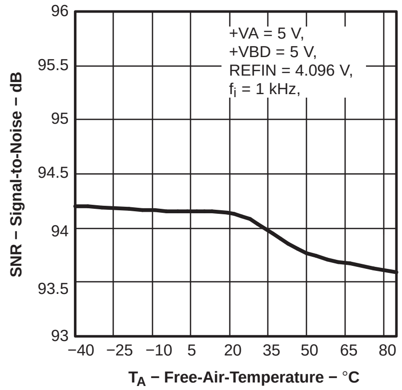


Figure 7.

SIGNAL-TO-NOISE AND DISTORTION vs FREE-AIR TEMPERATURE

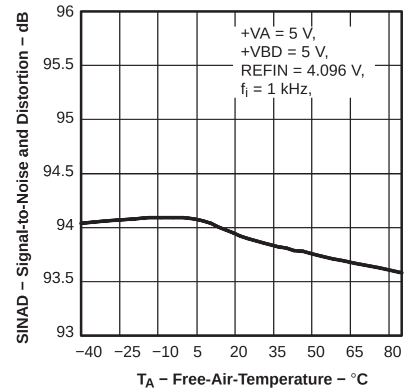


Figure 8.

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

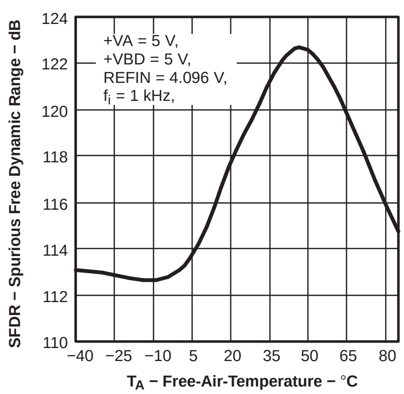


Figure 9.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

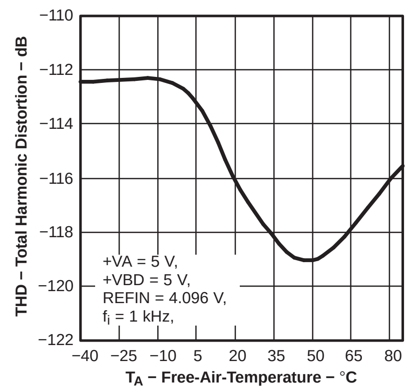


Figure 10.

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

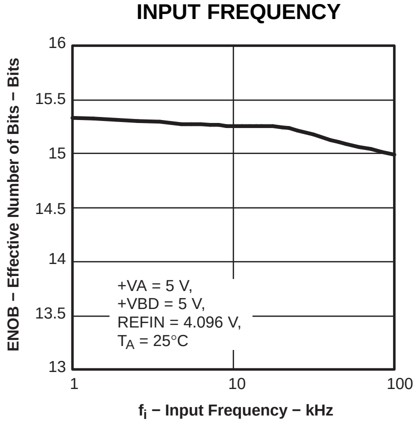


Figure 11.

SIGNAL-TO-NOISE AND DISTORTION vs INPUT FREQUENCY

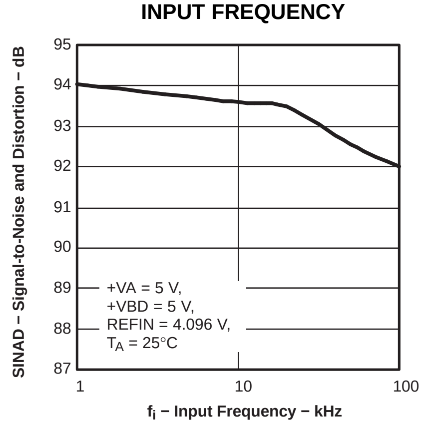


Figure 12.

TYPICAL CHARACTERISTICS (continued)

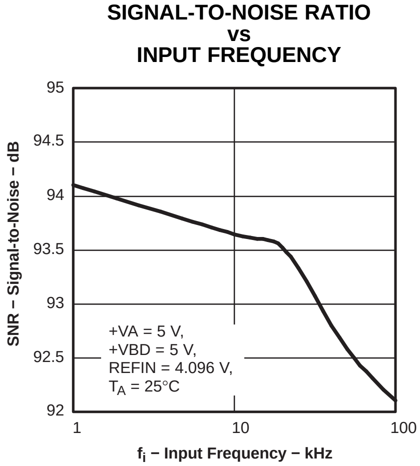


Figure 13.

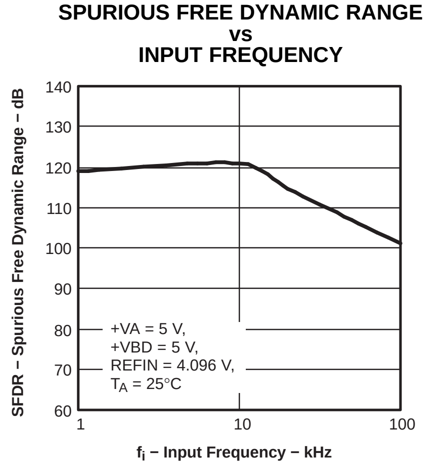


Figure 14.

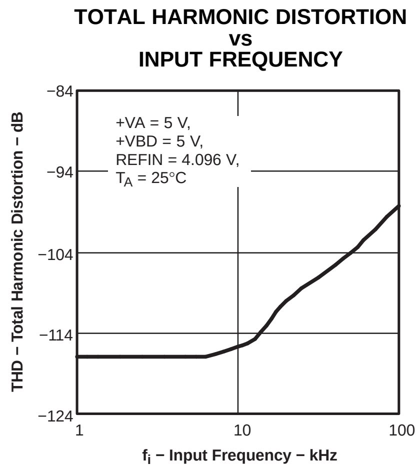


Figure 15.

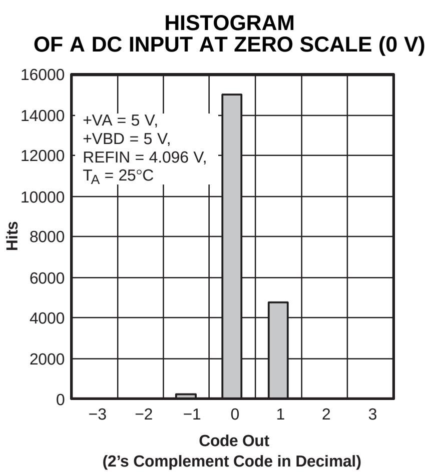


Figure 16.

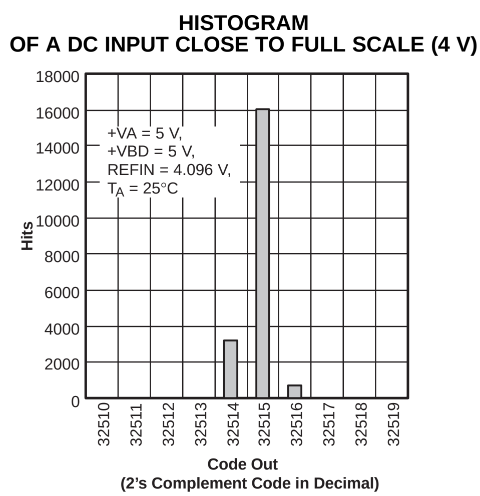


Figure 17.

TYPICAL CHARACTERISTICS (continued)

GAIN ERROR vs REFERENCE VOLTAGE

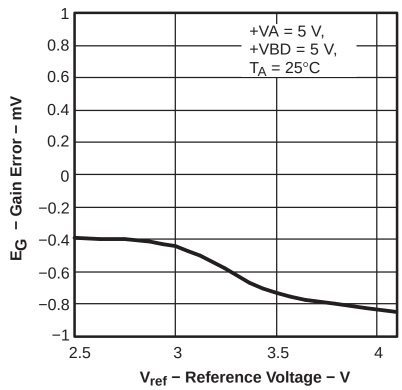


Figure 18.

GAIN ERROR vs ANALOG SUPPLY VOLTAGE

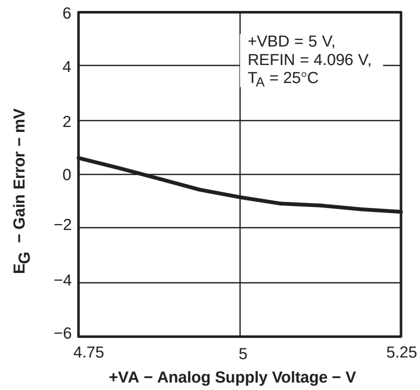


Figure 19.

GAIN ERROR vs FREE-AIR TEMPERATURE

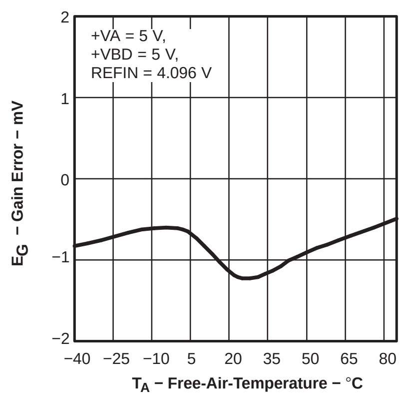


Figure 20.

OFFSET ERROR vs REFERENCE VOLTAGE

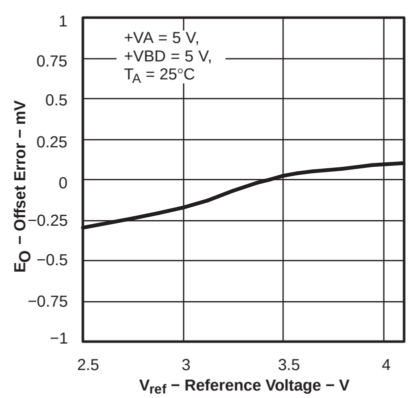


Figure 21.

OFFSET ERROR vs FREE-AIR TEMPERATURE

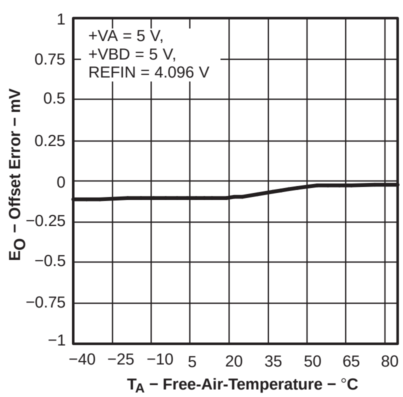


Figure 22.

OFFSET ERROR vs SUPPLY VOLTAGE

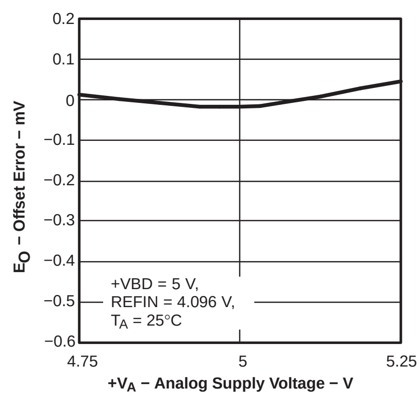


Figure 23.

TYPICAL CHARACTERISTICS (continued)

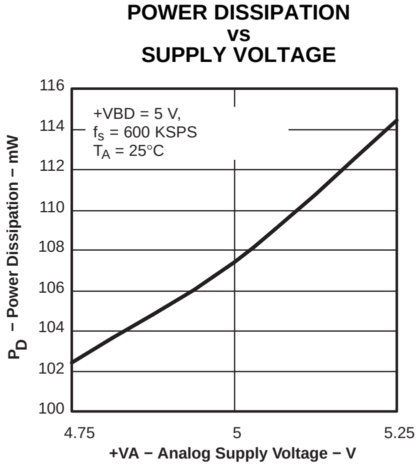


Figure 24.

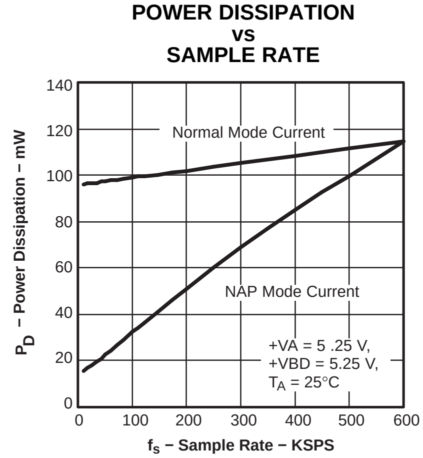


Figure 25.

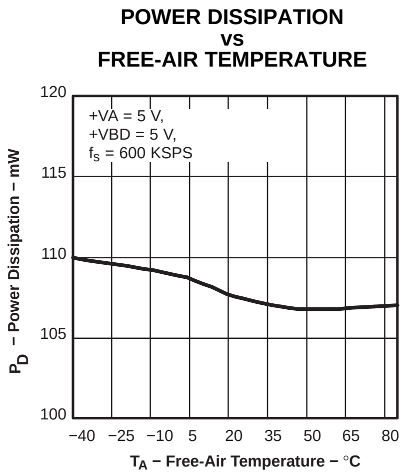


Figure 26.

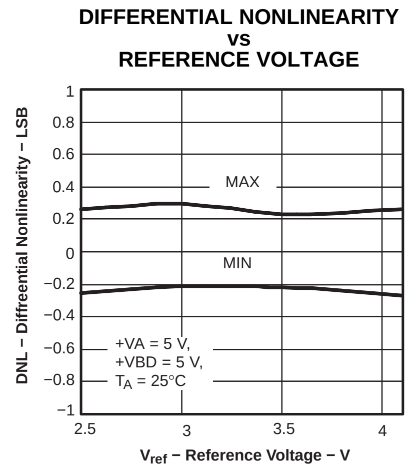


Figure 27.

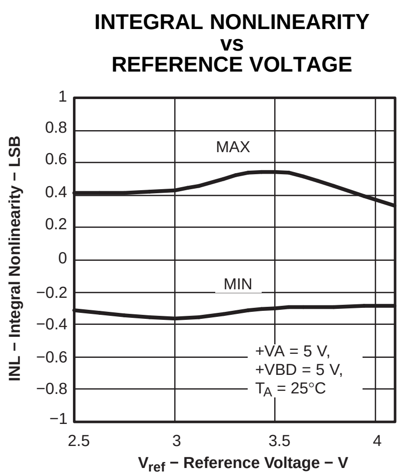


Figure 28.

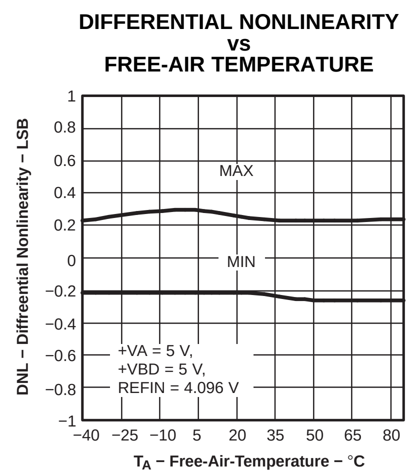


Figure 29.

TYPICAL CHARACTERISTICS (continued)

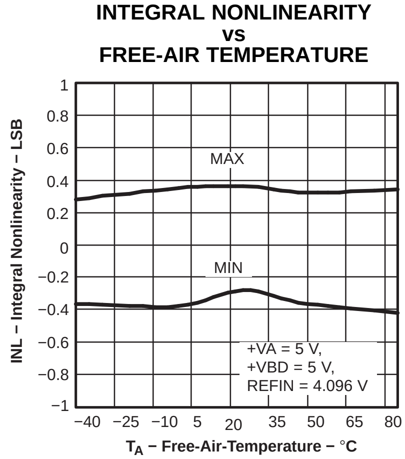


Figure 30.

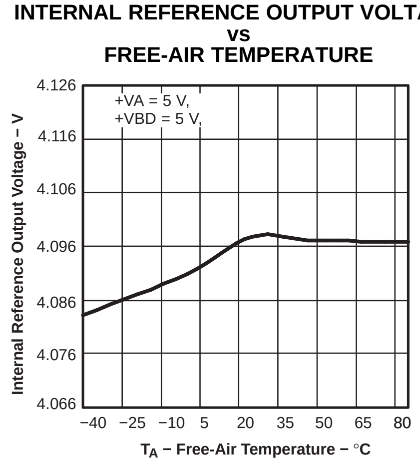


Figure 31.

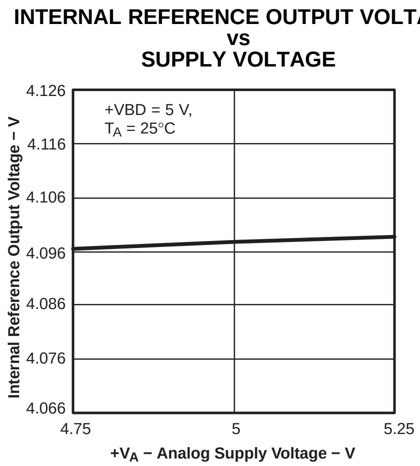


Figure 32.

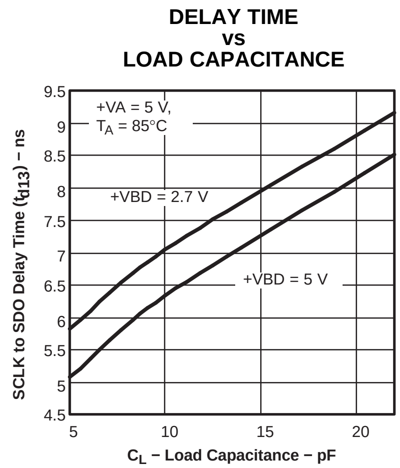


Figure 33.

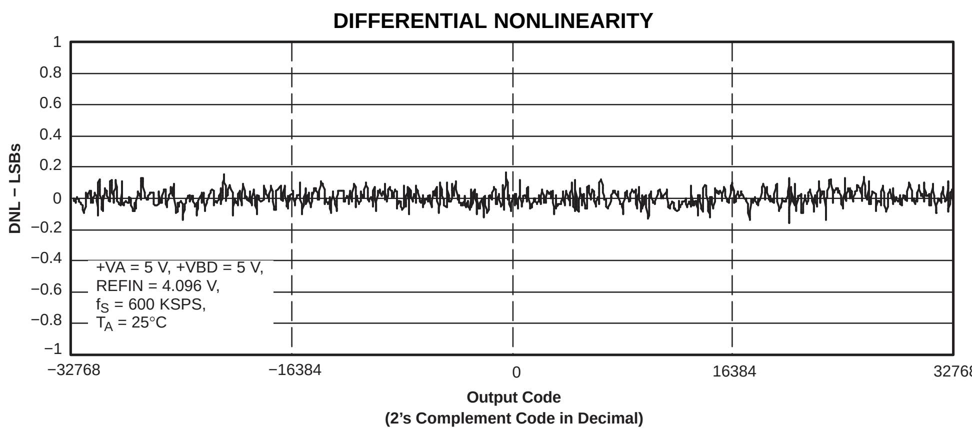


Figure 34.

TYPICAL CHARACTERISTICS (continued)

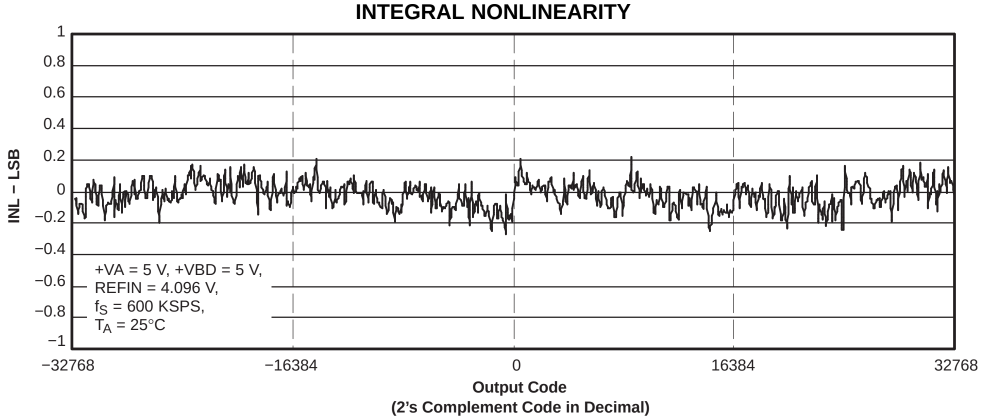


Figure 35.

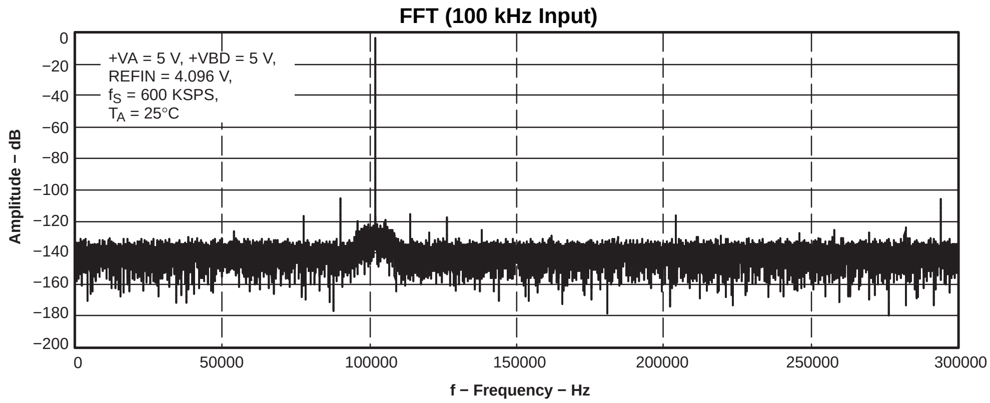


Figure 36.

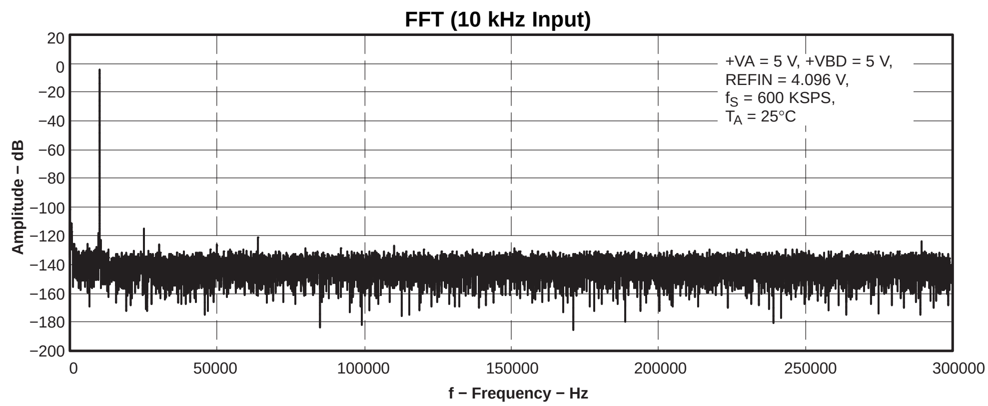
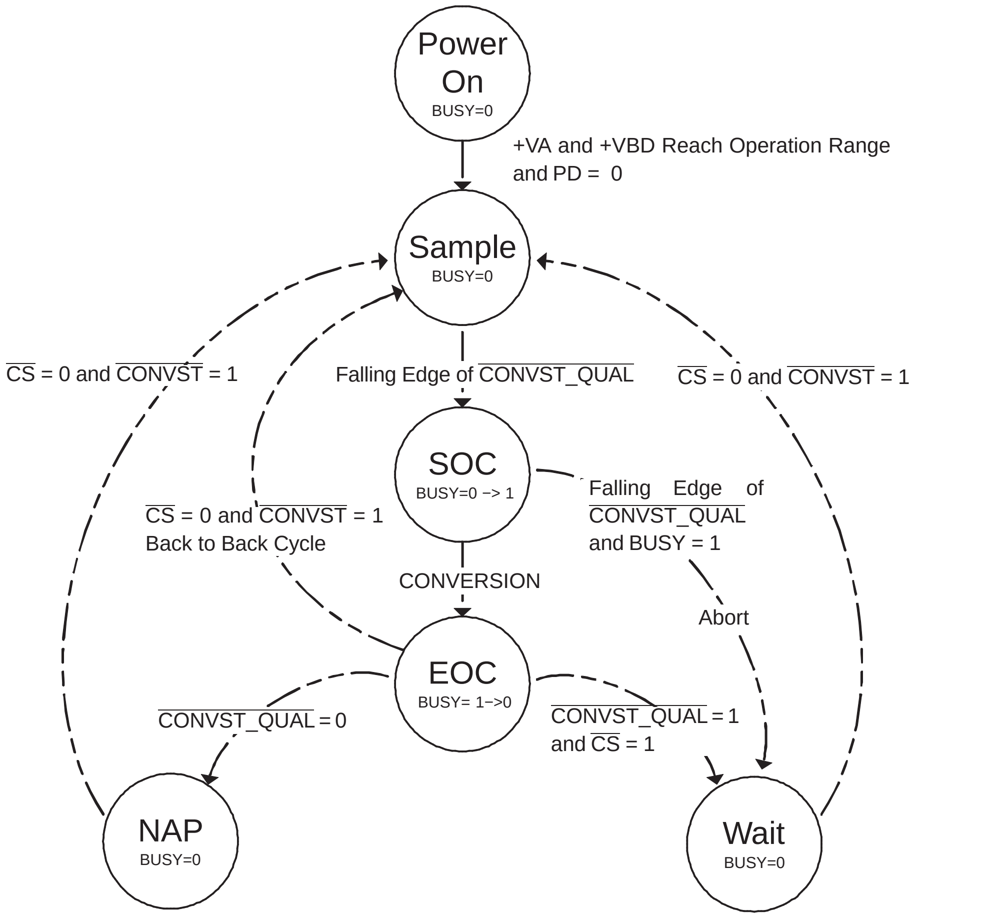


Figure 37.



A. EOC = End of conversion, SOC = Start of conversion, $\overline{\text{CONVST\_QUAL}}$ is $\overline{\text{CONVST}}$ latched by $\overline{\text{CS}}$ = 0, see Figure 39.

Figure 38. Device States and Ideal Transitions

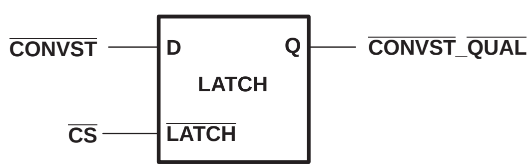


Figure 39. Relationship Between $\overline{\text{CONVST\_QUAL}}$, $\overline{\text{CS}}$, and $\overline{\text{CONVST}}$

TIMING DIAGRAMS

In the following descriptions, the signal $\overline{\text{CONVST\_QUAL}}$ represents $\overline{\text{CONVST}}$ latched by a low value on $\overline{\text{CS}}$ (see Figure 39).

To avoid performance degradation, there are three quiet zones to be observed (t_{quiet1} and t_{quiet2} are zones before and after the falling edge of $\overline{\text{CONVST\_QUAL}}$ while t_{quiet3} is a time zone before the falling edge of BUSY) where there should be no I/O activities. Interface control signals, including the serial clock should remain steady. Typical degradation in performance if these quiet zones are not observed is depicted in the specifications section.

To avoid data loss a read operation should not start around the BUSY falling edge. This is constrained by t_{su2}, t_{su3}, t_{h2}, and t_{h8}.

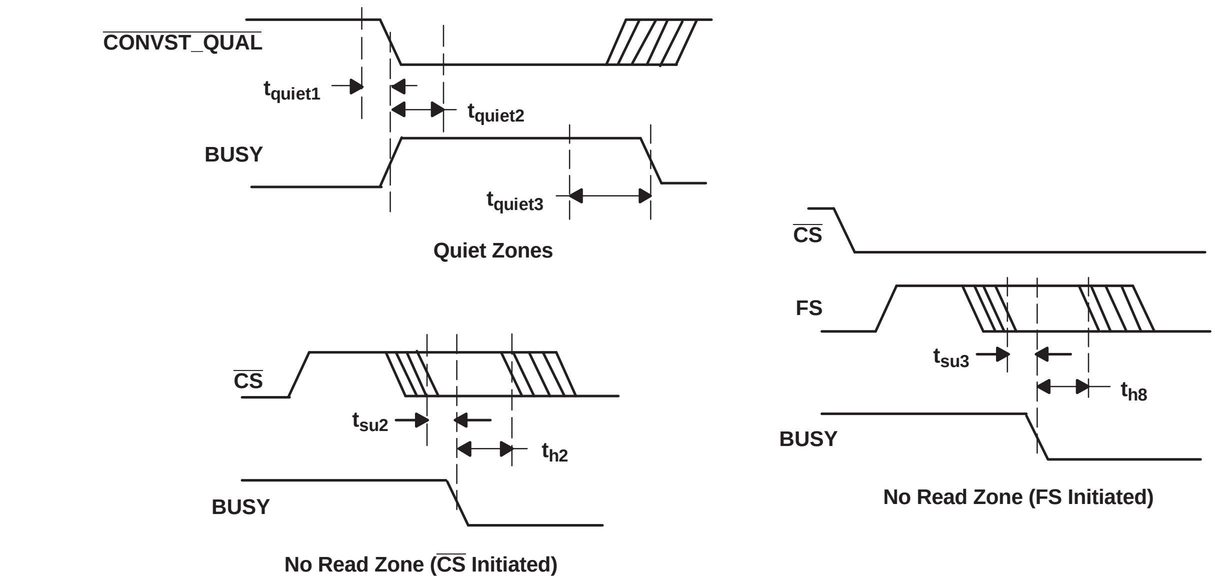


Figure 40. Quiet Zones and No-Read Zones

CONVERSION AND SAMPLING

1. Convert start command:

   The device enters the conversion phase from the sampling phase when a falling edge is detected on CONVST_QUAL. This is shown in Figure 41, Figure 42, and Figure 43.

2. Sample (acquisition) start command:

   The device starts sampling from the wait/nap state or at the end of a conversion if CONVST is detected as high and CS as low. This is shown in Figure 41, Figure 42, and Figure 43.

   Maintaining this condition (holding CS low) when the device has just finished a conversion (as shown in Figure 41) takes the device immediately into the sampling phase after the conversion phase (back-to-back conversion) and hence achieves the maximum throughput. Otherwise, the device enters the wait state or the nap state.

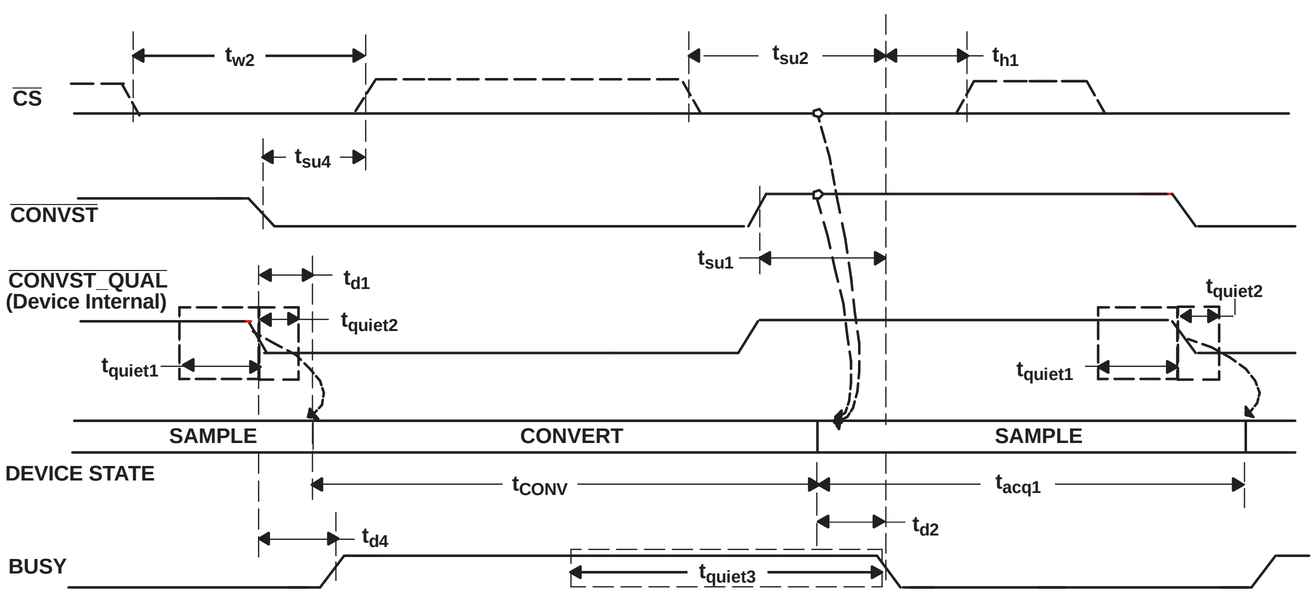


Figure 41. Back-to-Back Conversion and Sample

3. Wait/Nap entry stimulus:

   The device enters the wait or nap phase at the end of the conversion if the sample start command is not given. This is shown in Figure 42.

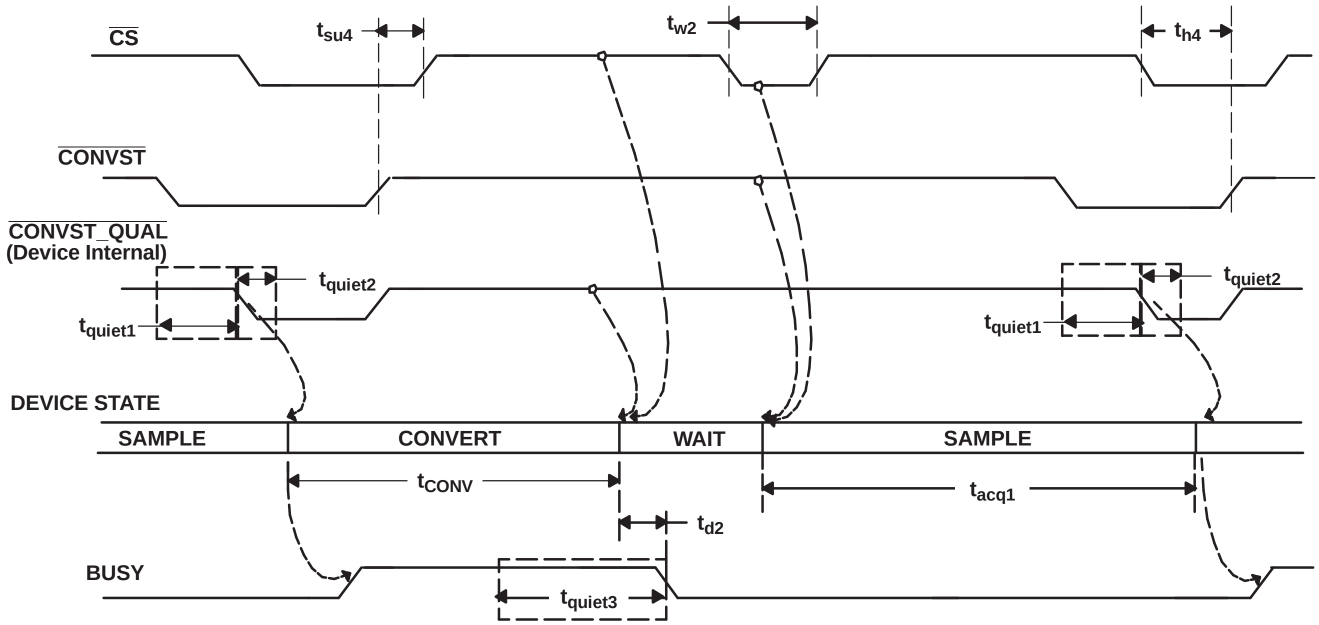


Figure 42. Convert and Sample with Wait

If lower power dissipation is desired and throughput can be compromised, a nap state can be inserted in between cycles (as shown in Figure 43). The device enters a low power (3 mA) state called nap if the end of the conversion happens when $\overline{\text{CONVST\_QUAL}}$ is low. The cost for using this special wait state is a longer sampling time (t_{acq2}) plus the nap time.

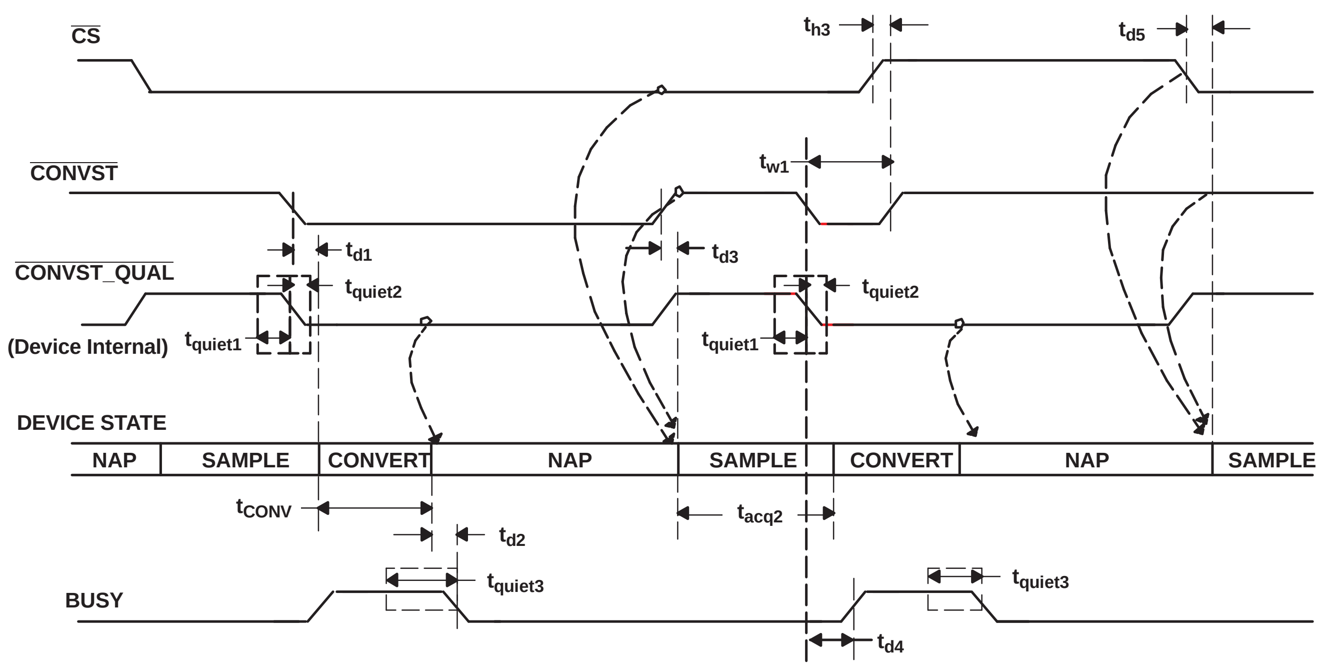


Figure 43. Convert and Sample with Nap

4. Conversion abort command:

An ongoing conversion can be aborted by using the conversion abort command. This is done by forcing another start of conversion (a valid $\overline{\text{CONVST\_QUAL}}$ falling edge) onto an ongoing conversion as shown in Figure 44. The device enters the wait state after an aborted conversion. If the previous conversion was successfully aborted, the device output reads 0xFF00 on SDO.

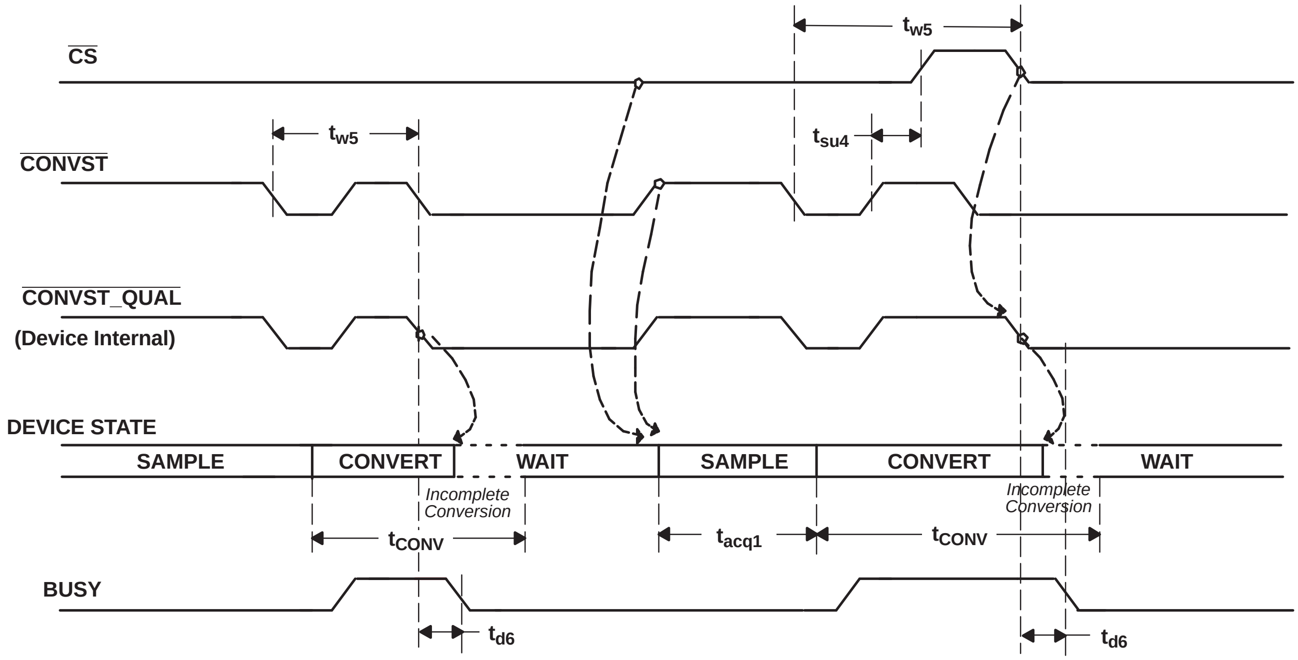


Figure 44. Conversion Abort

DATA READ OPERATION

Data read control is independent of conversion control. Data can be read either during conversion or during sampling. Data that is read during a conversion involves latency of one sample. The start of a new data frame around the fall of BUSY is constrained by t_{su2}, t_{su3}, t_{h2}, and t_{h8}.

1. SPI interface:

   A data read operation in SPI interface mode is shown in Figure 45. FS must be tied high for operating in this mode. The MSB of the output data is available at the falling edge of $\overline{\text{CS}}$. MSB – 1 is shifted out at the first rising edge after the first falling edge of SCLK after $\overline{\text{CS}}$ falling edge. Subsequent bits are shifted at the subsequent rising edges of SCLK. If another data frame is attempted (by pulling $\overline{\text{CS}}$ high and subsequently low) during an active data frame, then the ongoing frame is aborted and a new frame is started.

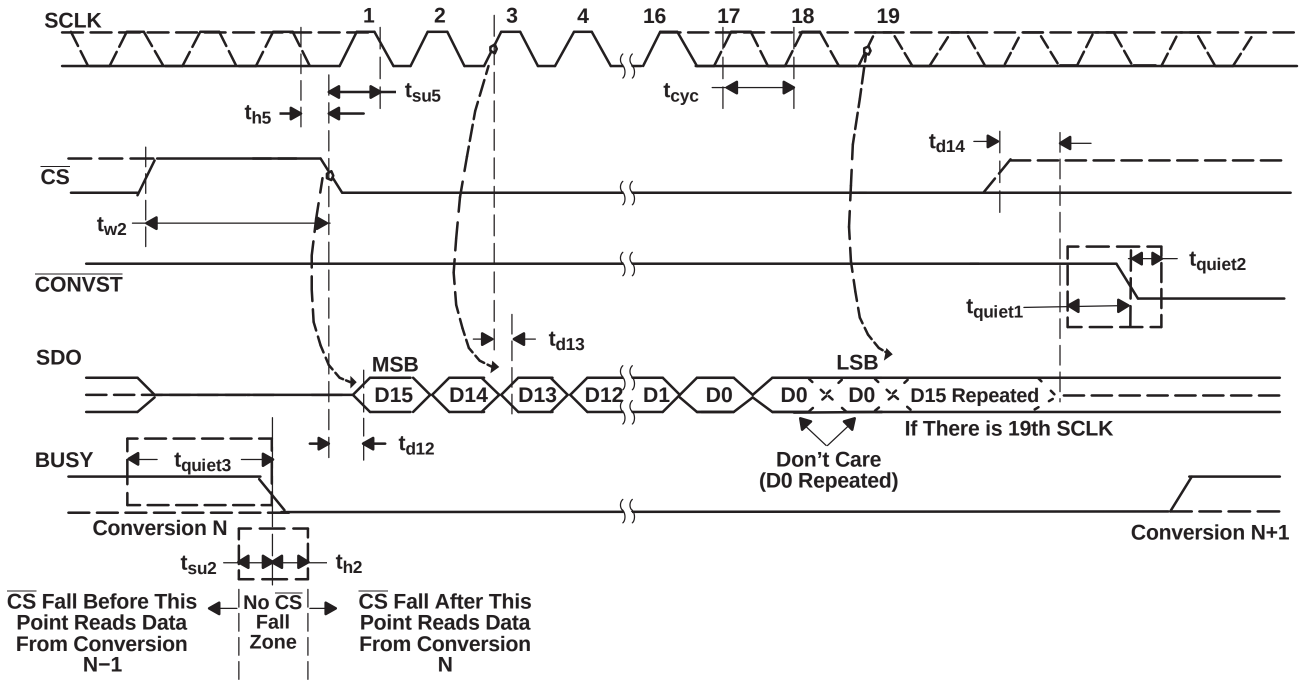


Figure 45. Read Frame Controlled via $\overline{CS}$ (FS = 1)

If another data frame is attempted (by pulling $\overline{CS}$ high and then low) during an active data frame, then the ongoing frame is aborted and a new frame is started.

2. Serial interface using FS:

   A data read operation in this mode is shown in Figure 46 and Figure 47. The MSB of the output data is available at the rising edge of FS. MSB – 1 is shifted out at the first rising edge after the first falling edge of SCLK after the FS falling edge. Subsequent bits are shifted at the subsequent rising edges of SCLK.

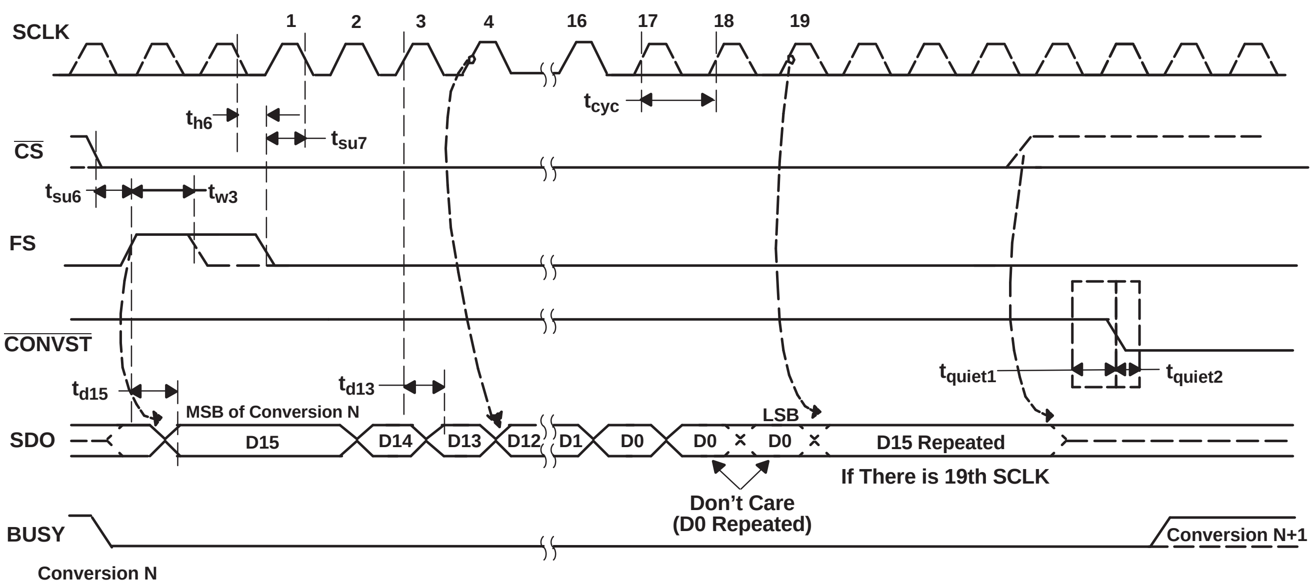


Figure 46. Read Frame Controlled via FS (FS is Low When BUSY Falls)

If FS is high when BUSY falls, the SDO is updated again with the new MSB when BUSY falls. This is shown in Figure 47.

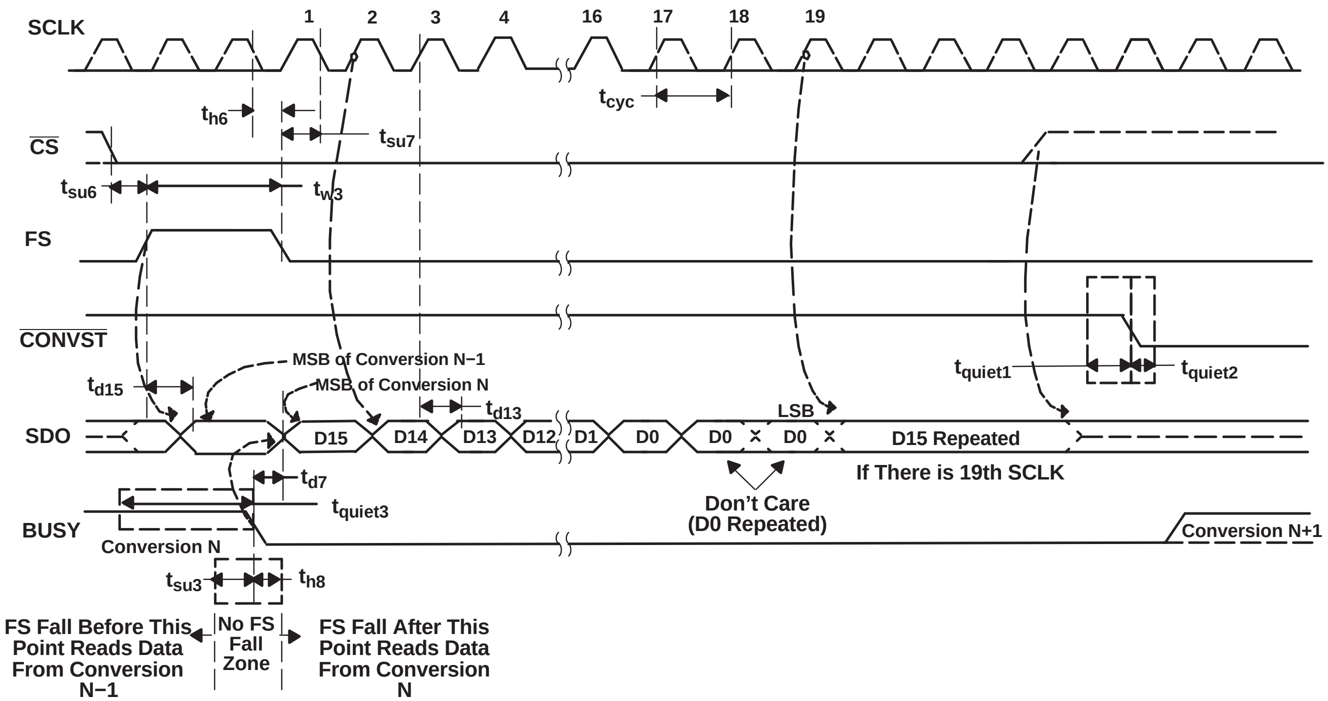


Figure 47. Read Frame Controlled via FS (FS is High When BUSY Falls)

If another data frame is attempted by pulling up FS during an active data frame, then the ongoing frame is aborted and a new frame is started.

THEORY OF OPERATION

The ADS8372 is a high-speed successive approximation register (SAR) analog-to-digital converter (ADC). The architecture is based on charge redistribution, which inherently includes a sample/hold function.

The device includes a built-in conversion clock, internal reference, and 40-MHz SPI compatible serial interface. The maximum conversion time is 1.1 µs which is capable of sustaining a 600-kHz throughput.

The analog input is provided to the two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8372 has a built-in 4.096-V (nominal value) reference but can operate with an external reference also. When the internal reference is used, pin 9 (REFOUT) should be shorted to pin 8 (REFIN) and a 0.1-µF decoupling capacitor and a 1-µF storage capacitor must be connected between pin 8 (REFIN) and pin 7 (REFM) (see Figure 48). The internal reference of the converter is buffered.

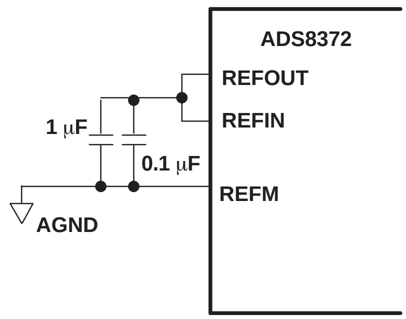


Figure 48. ADS8372 Using Internal Reference

The REFIN pin is also internally buffered. This eliminates the need to put a high bandwidth buffer on the board to drive the ADC reference and saves system area and power. When an external reference is used, the reference must be of low noise, which may be achieved by the addition of bypass capacitors from the REFIN pin to the REFM pin. See Figure 49 for operation of the ADS8372 with an external reference. REFM must be connected to the analog ground plane.

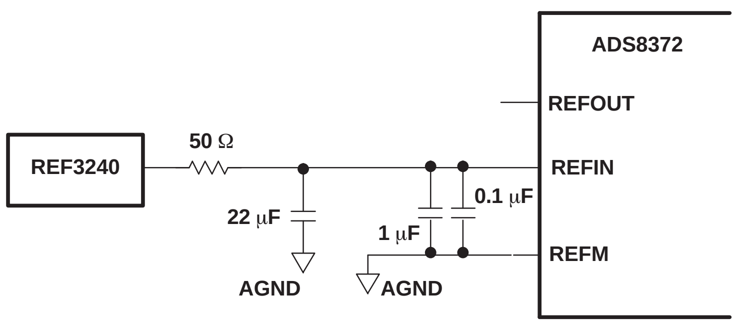


Figure 49. ADS8372 Using External Reference

THEORY OF OPERATION (continued)

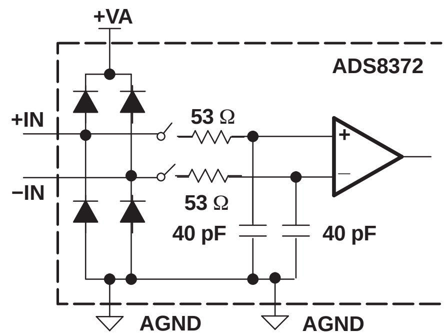


Figure 50. Simplified Analog Input

ANALOG INPUT

When the converter enters hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. Both the +IN and –IN inputs have a range of –0.2 V to (+V_{REF} + 0.2 V). The input span (+IN – (–IN)) is limited from –V_{REF} to V_{REF}.

The input current on the analog inputs depends upon throughput and the frequency content of the analog input signals. Essentially, the current into the ADS8372 charges the internal capacitor array during the sampling (acquisition) time. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the device sampling capacitance (40 pF each from +IN/–IN to AGND) to an 16-bit settling level within the sampling (acquisition) time of the device. When the converter goes into hold mode, the input resistance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the +IN, –IN inputs and the span (+IN – (–IN)) should be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications.

Care should be taken to ensure that the output impedance of the sources driving +IN and –IN inputs are matched. If this is not observed, the two inputs can have different settling times. This can result in offset error, gain error, and linearity error which vary with temperature and input voltage.

A typical input circuit using TI's THS4031 is shown in Figure 51. In the figure, input from a single-ended source is converted into a differential signal for the ADS8372. In the case where the source is differential, the circuit in Figure 52 may be used. Most of the specified performance figure were measured using the circuit in Figure 52.

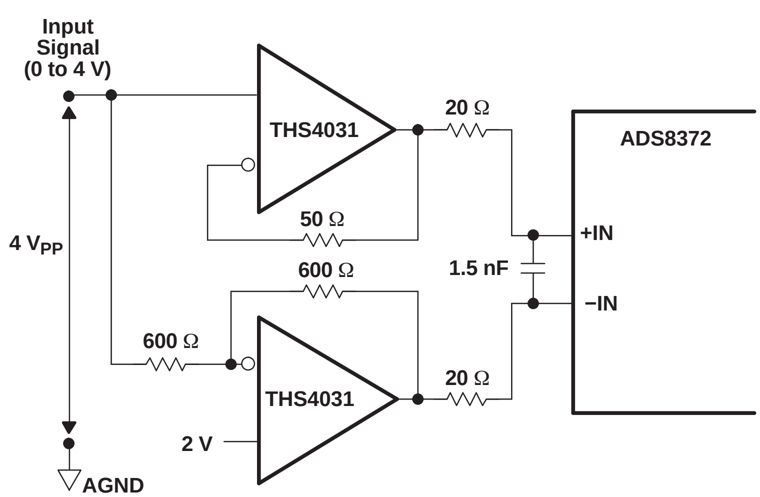


Figure 51. Single-Ended Input, Differential Output Configuration

THEORY OF OPERATION (continued)

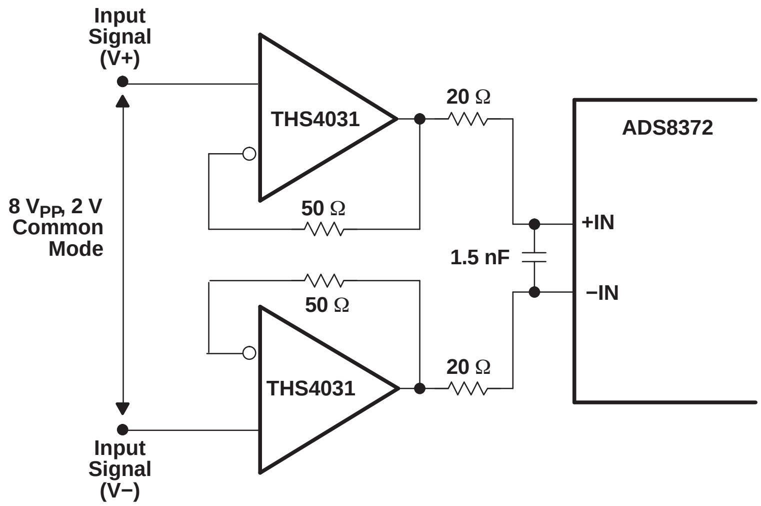


Figure 52. Differential Input, Differential Output Configuration

DIGITAL INTERFACE

TIMING AND CONTROL

Conversion and sampling are controlled by the $\overline{\text{CONVST}}$ and $\overline{\text{CS}}$ pins. See the timing diagrams for detailed information on timing signals and their requirements. The ADS8372 uses an internally generated clock to control the conversion rate and in turn the throughput of the converter. SCLK is used for reading converted data only. A clean and low jitter conversion start command is important for the performance of the converter. There is a minimal quiet zone requirement around the conversion start command as mentioned in the timing requirements table.

READING DATA

The ADS8372 offers a high speed serial interface that is compatible with the SPI protocol. The device outputs the data in 2's complement format. Refer to Table 1 for the ideal output codes.

Table 1. Input Voltages and Ideal Output Codes

DESCRIPTION	ANALOG VALUE +IN – (–IN)	DIGITAL OUTPUT (HEXADECIMAL)
Full-scale range	$2(+V_{REF})$	2's Complement
Least significant bit (LSB)	$2(+V_{REF})/2^{16}$	
Full scale	V_{REF} – 1 LSB	7FFF
Mid scale	0	0000
Mid scale – 1 LSB	0 V – 1 LSB	FFFF
–Full scale	$-V_{REF}$	8000

To avoid performance degradation due to the toggling of device buffers, read operation must not be performed in the specified quiet zones (t_{quiet1}, t_{quiet2}, and t_{quiet3}). Internal to the device, the previously converted data is updated with the new data near the fall of BUSY. Hence, the fall of $\overline{\text{CS}}$ and the fall of FS around the fall of BUSY is constrained. This is specified by t_{su2}, t_{su3}, t_{h2}, and t_{h8} in the timing requirements table.

POWER SAVING

The converter provides two power saving modes, full power down and nap. Refer to Table 2 for information on activation/deactivation and resumption time for both modes.

Table 2. Power Save

TYPE OF POWER DOWN	SDO	POWER CONSUMPTION	ACTIVATED BY	ACTIVATION TIME (t_{d16})	RESUME POWER BY
Normal operation	Not 3 stated	22 mA	NA	NA	NA
Full power down (Int Ref, 1-µF capacitor on REFOUT pin)	3 Stated (t_{d10} timing)	2 µA	PD = 1	10 µs	PD = 0
Full power down (Ext Ref, 1-µF capacitor on REFOUT pin)	3 Stated (t_{d10} timing)	2 µA	PD = 1	10 µs	PD = 0
Nap power down	Not 3 stated	3 mA	At EOC and $\overline{\text{CONVST\_QUAL}}$ = 0	200 ns	Sample Start command

FULL POWER-DOWN MODE

Full power-down mode is activated by turning off the supply or by asserting PD to 1. See Figure 53 and Figure 54. The device can be resumed from full power down by either turning on the power supply or by de-asserting the PD pin. The first two conversions produce inaccurate results because during this period the device loads its trim values to ensure the specified accuracy.

If an internal reference is used (with a 1-µF capacitor installed between the REFOUT and REFM pins), the total resume time (t_{d18}) is 25 ms. After the first two conversions, t_{d17} (4 ms) is required for the trimmed internal reference voltage to settle to the specified accuracy. Only then the converted results match the specified accuracy.

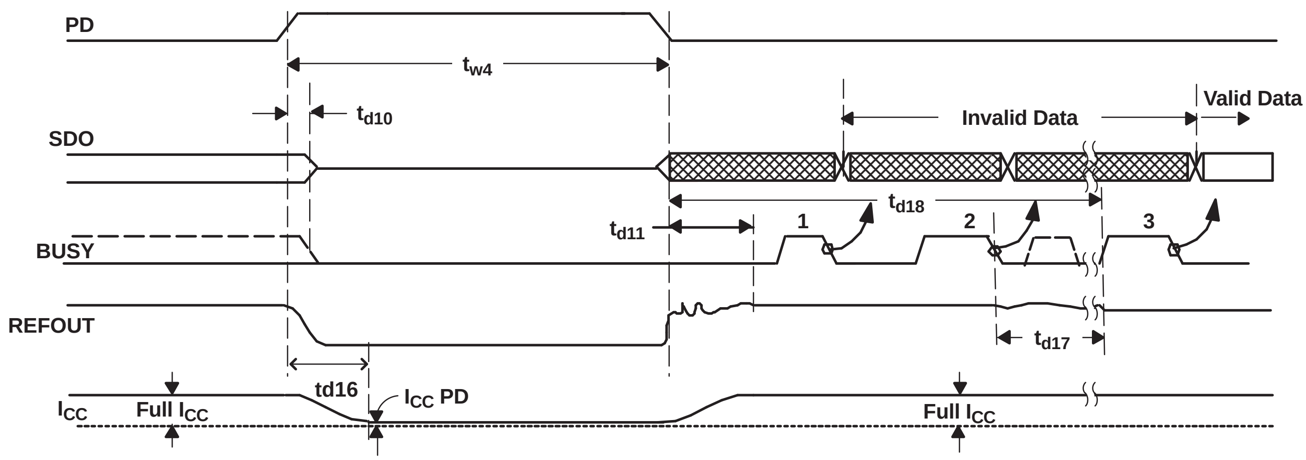


Figure 53. Device Full Power Down/Resume (Internal Reference Used)

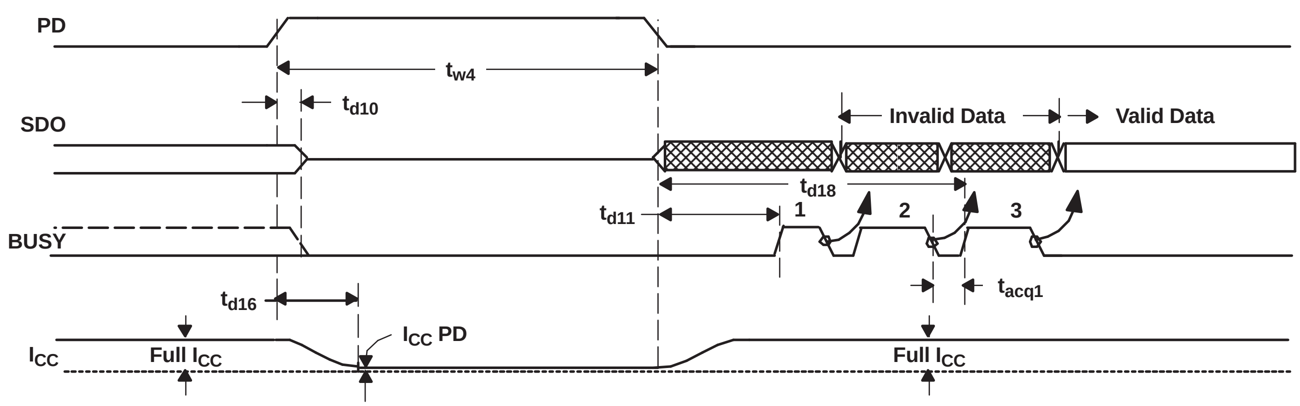


Figure 54. Device Full Power Down/Resume (External Reference Used)

NAP MODE

Nap mode is automatically inserted at the end of a conversion if $\overline{\text{CONVST\_QUAL}}$ is held low at EOC. The device can be operated in nap mode at the end of every conversion for saving power at lower throughputs. Another way to use this mode is to convert multiple times and then enter nap mode. The minimum sampling time after a nap state is $t_{acq1} + t_{d18} = t_{acq2}$.

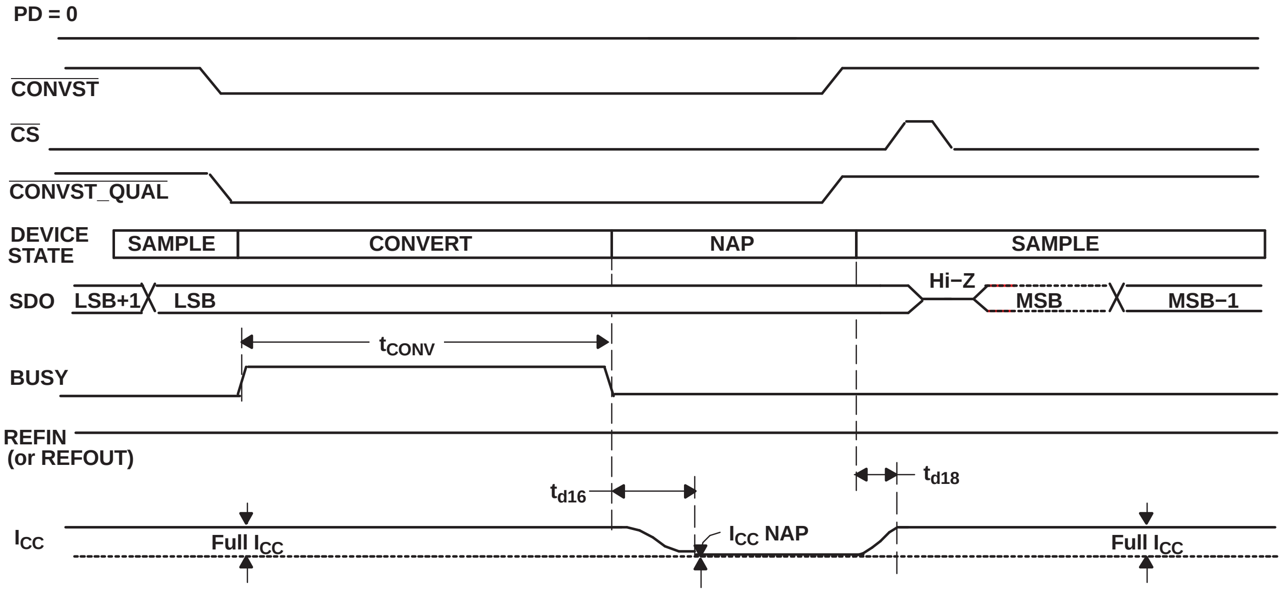


Figure 55. Device Nap Power Down/Resume

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8372 circuitry.

Since the ADS8372 offers single-supply operation, it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more the digital logic in the design and the higher the switching speed, the greater the need for better layout and isolation of the critical analog signals from these switching digital signals.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to the end of sampling and just prior to the latching of the analog comparator. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices. Noise during the end of sampling and the latter half of the conversion must be kept to a minimum (the former half of the conversion is not very sensitive since the device uses a proprietary error correction algorithm to correct for the transient errors made here).

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing and degree of the external event.

On average, the ADS8372 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external, it must be ensured that the reference source can drive the bypass capacitor without oscillation. A 0.1-µF bypass capacitor is recommended from pin 8 directly to pin 7 (REFM).

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the *analog* ground. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

LAYOUT (continued)

As with the AGND connections, +VA should be connected to a +5-V power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8372 should be clean and well bypassed. A 0.1-μF ceramic bypass capacitor should be placed as close to the device as possible. See Table 3 for the placement of these capacitors. In addition, a 1-μF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-μF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the +5-V supply, removing the high frequency noise.

Table 3. Power Supply Decoupling Capacitor Placement

SUPPLY PINS	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
Pair of pins requiring a shortest path to decoupling capacitors	(2,3); (5,6); (15,16); (17,18)	(20,21)
Pins requiring no decoupling	1, 4, 14, 19	

When using the internal reference, ensure a shortest path from REFOUT (pin 9) to REFIN (pin 8) with the bypass capacitor directly between pins 8 and 7.

APPLICATION INFORMATION

EXAMPLE DIGITAL STIMULUS

The use of the ADS8372 is very straightforward. The following timing diagram shows one example of how to achieve a 600-KSPS throughput using a SPI compatible serial interface.

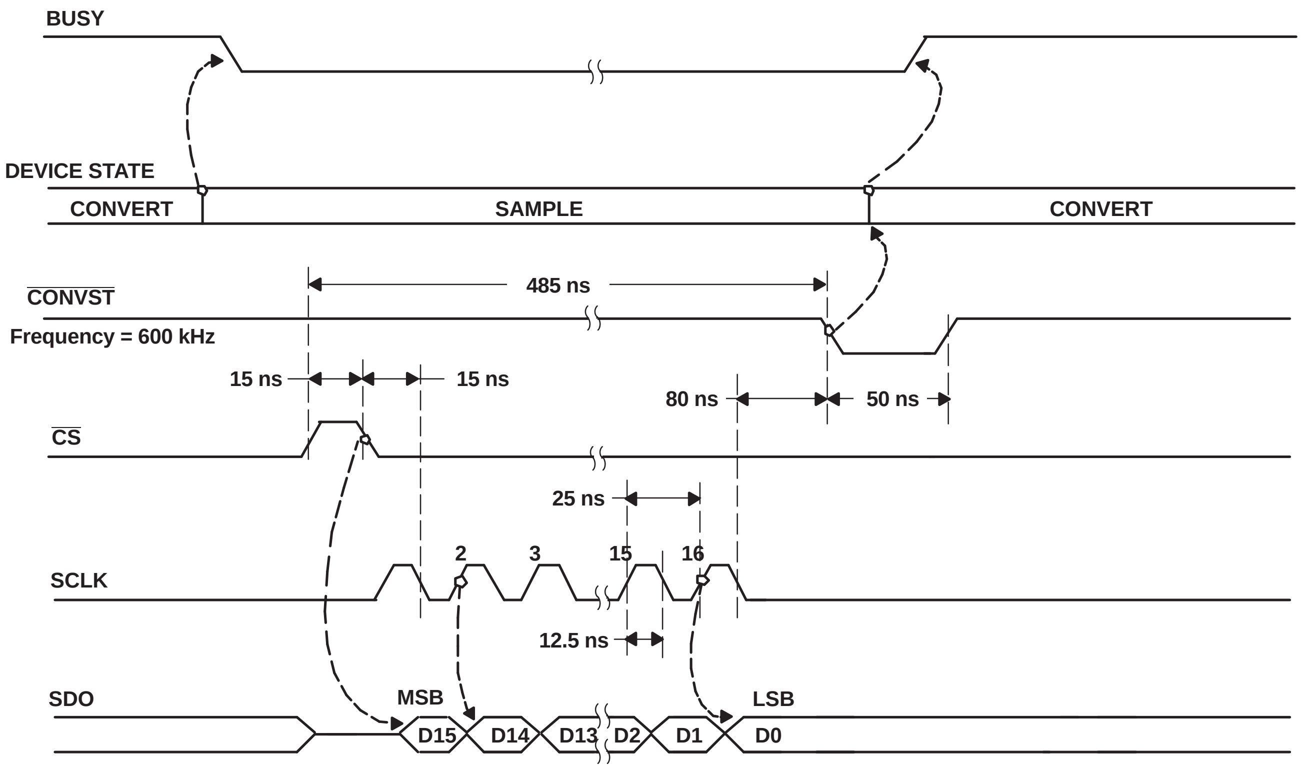


Figure 56. Example Stimulus in SPI Mode (FS = 1), Back-To-Back Conversion that Achieves 600 KSPS

It is also possible to use the frame sync signal, FS. The following timing diagram shows how to achieve a 600-KSPS throughput using a modified serial interface with FS active.

APPLICATION INFORMATION (continued)

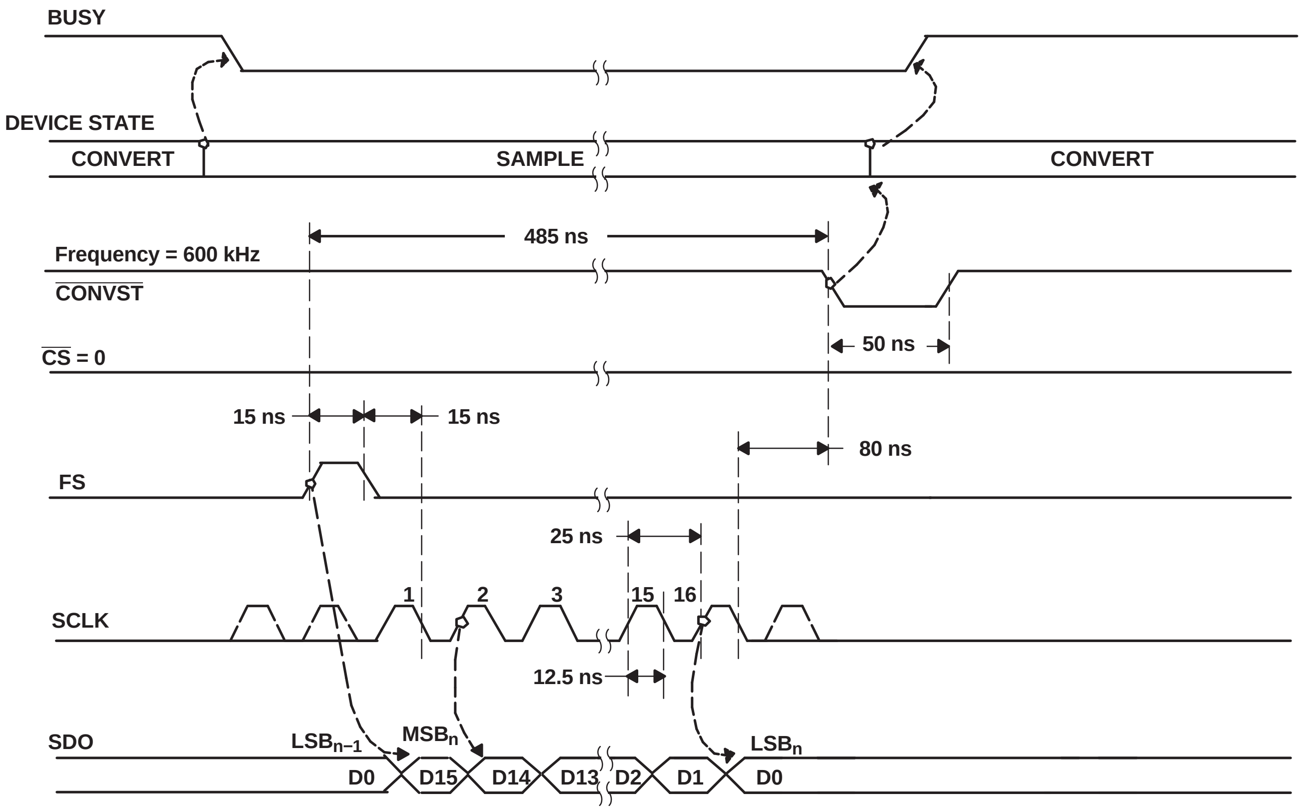


Figure 57. Example Stimulus in Serial Interface With FS Active, Back-To-Back Conversion that Achieves 600 KSPS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS8372IBRHPR	ACTIVE	QFN	RHP	28	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8372IBRHPRG4	ACTIVE	QFN	RHP	28	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8372IBRHPT	ACTIVE	QFN	RHP	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8372IBRHPTG4	ACTIVE	QFN	RHP	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8372IRHPR	ACTIVE	QFN	RHP	28	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8372IRHPRG4	ACTIVE	QFN	RHP	28	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8372IRHPT	ACTIVE	QFN	RHP	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8372IRHPTG4	ACTIVE	QFN	RHP	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

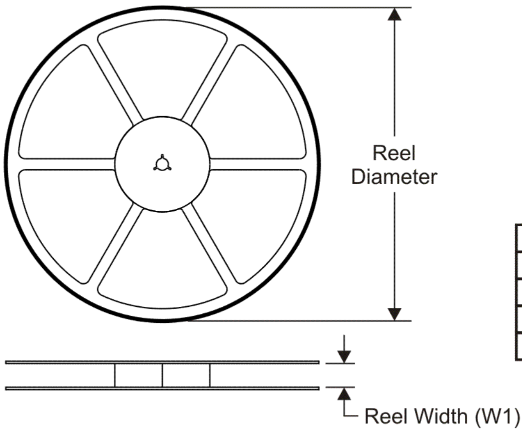
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

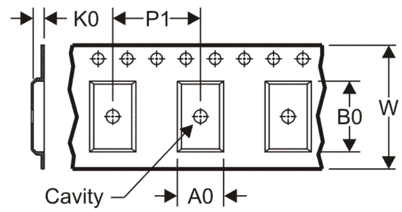
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

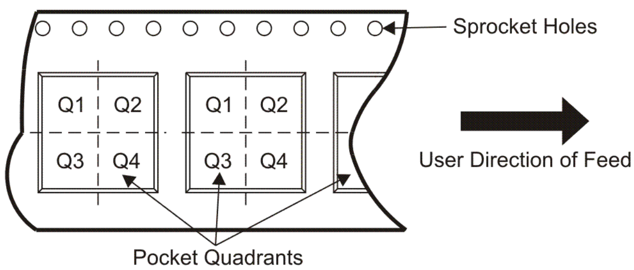
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





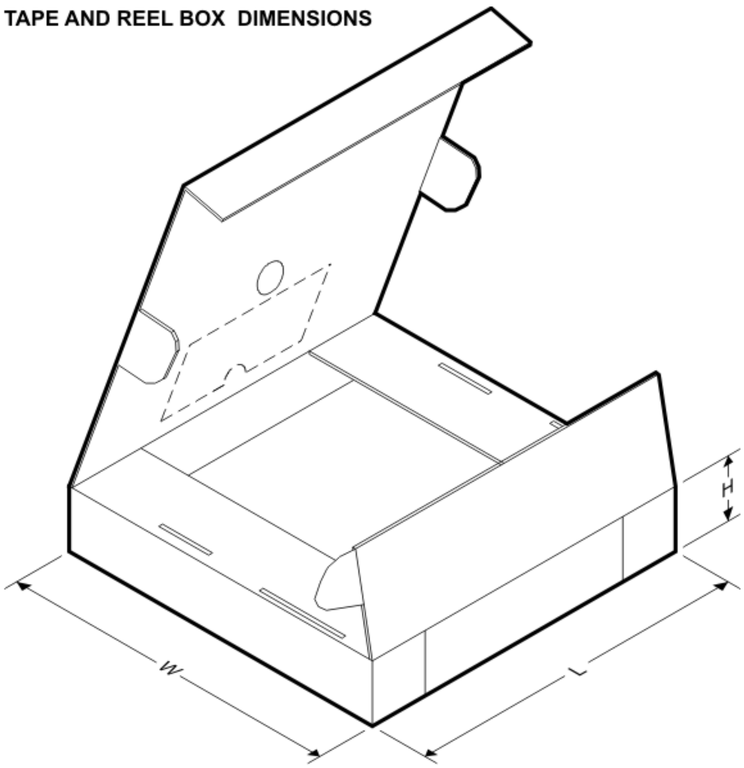
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8372IBRHPR	QFN	RHP	28	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
ADS8372IBRHPT	QFN	RHP	28	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
ADS8372IRHPR	QFN	RHP	28	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2
ADS8372IRHPT	QFN	RHP	28	250	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

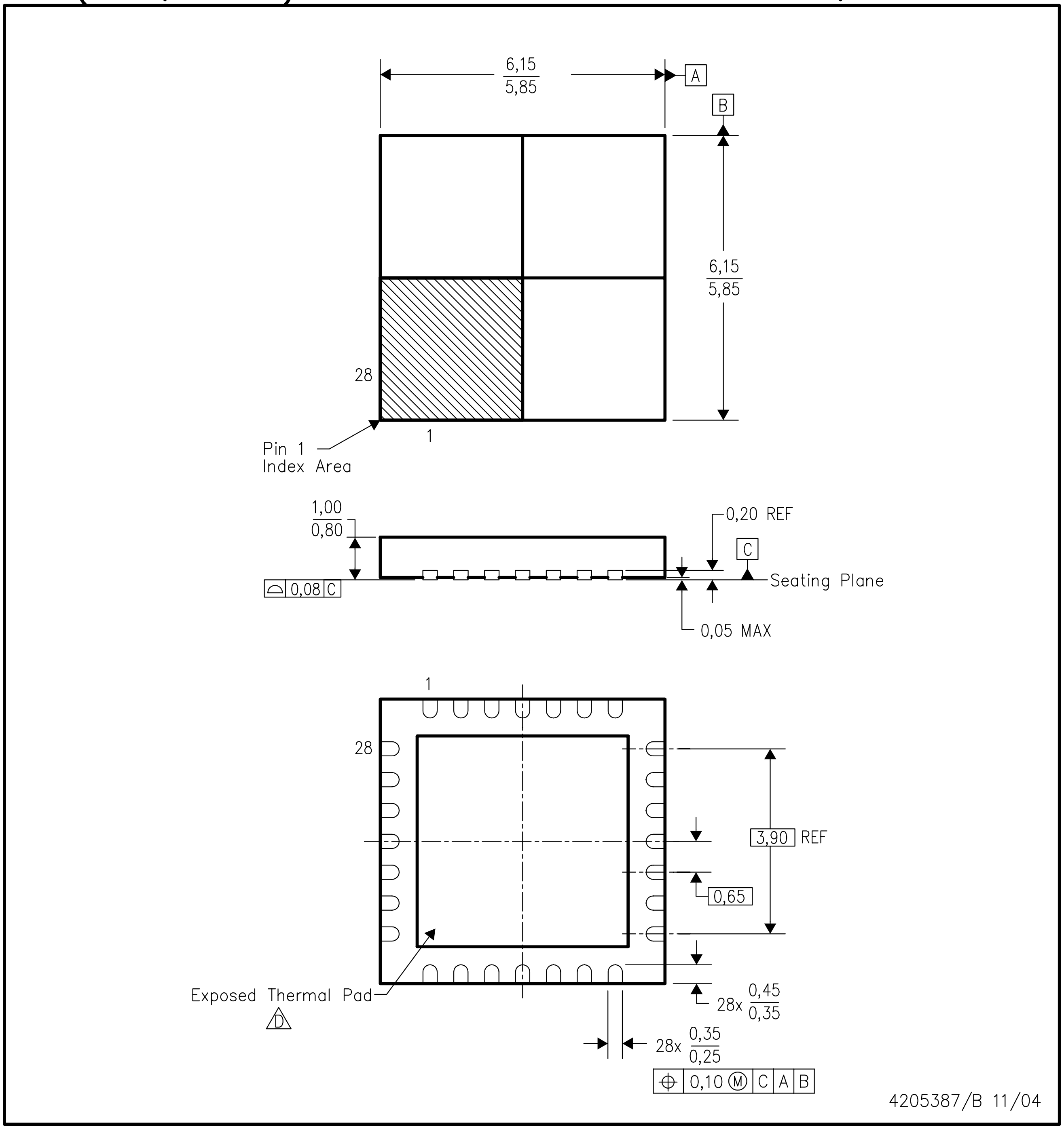
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8372IBRHPR	QFN	RHP	28	2500	333.2	345.9	28.6
ADS8372IBRHPT	QFN	RHP	28	250	333.2	345.9	28.6
ADS8372IRHPR	QFN	RHP	28	2500	333.2	345.9	28.6
ADS8372IRHPT	QFN	RHP	28	250	333.2	345.9	28.6

RHP (S-PQFP-N28) PLASTIC QUAD FLATPACK



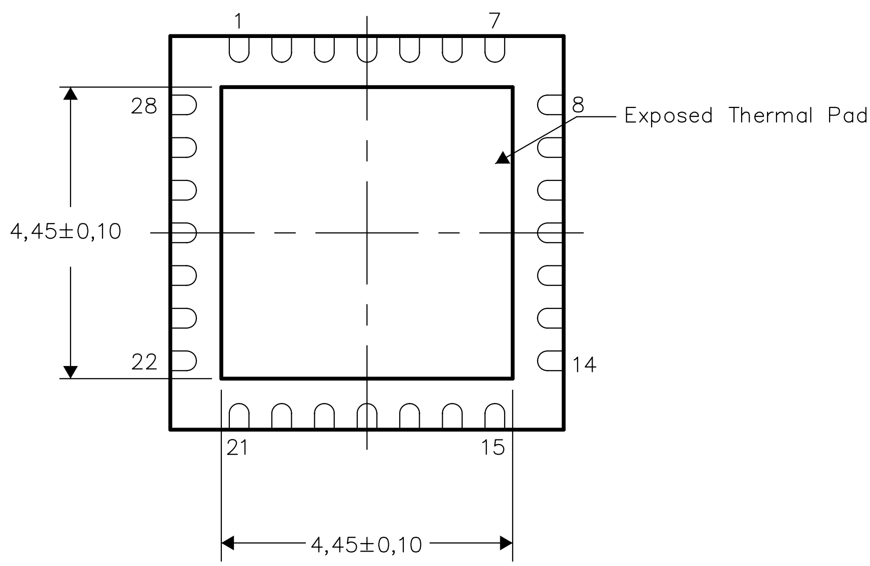
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

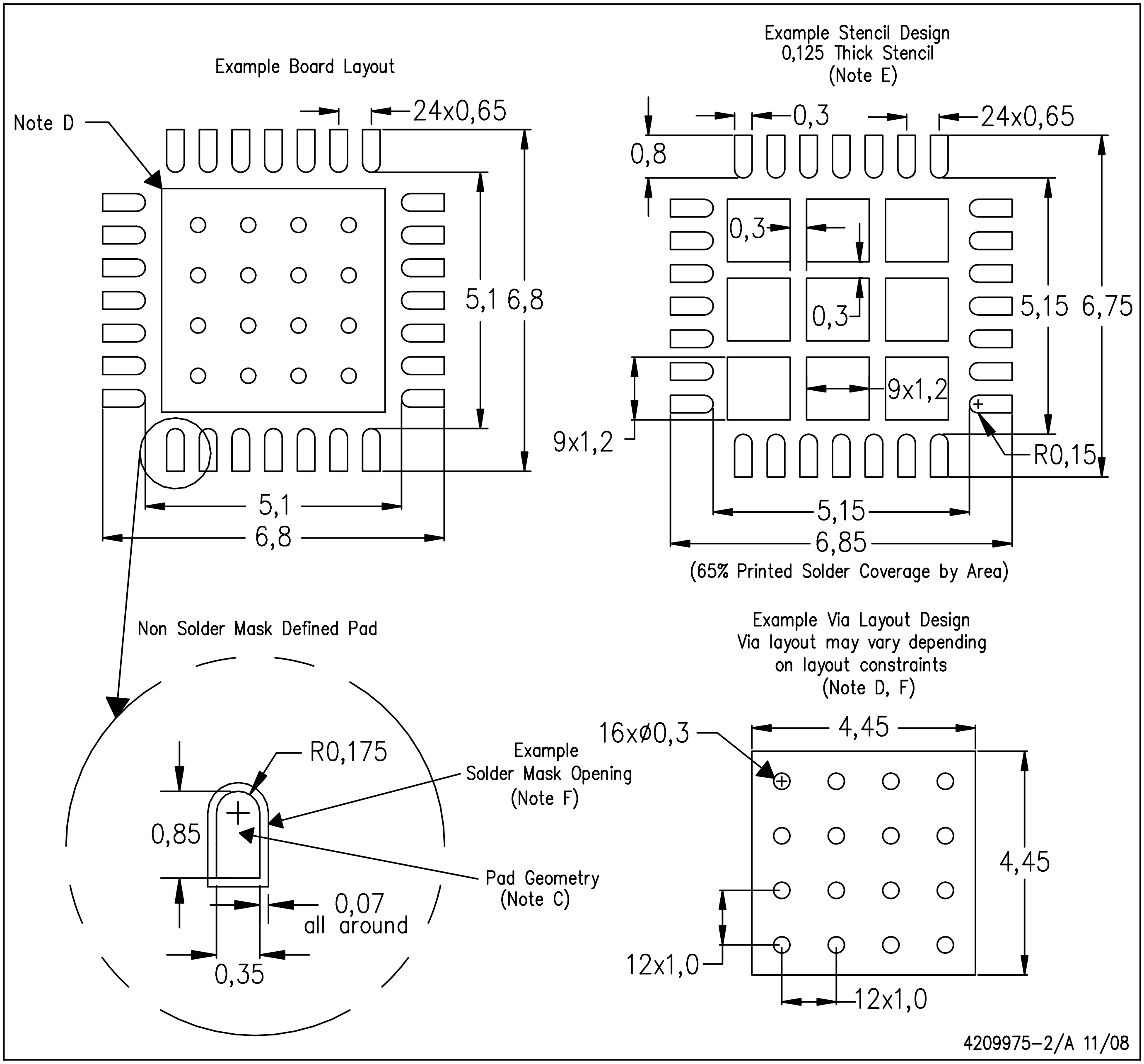


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHP (S–PQFP–N28)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265