

IS66WV51216ALL IS66WV51216BLL



8Mb LOW VOLTAGE, ULTRA LOW POWER PSEUDO CMOS STATIC RAM

PRELIMINARY INFORMATION
AUGUST 2008

FEATURES

- High-speed access time: 55ns
- CMOS low power operation
 - mW (typical) operating
 - μ W (typical) CMOS standby
- Single power supply
 - 1.7V--1.95V V_{DD} (66WV51216ALL) (70ns)
 - 2.5V--3.6V V_{DD} (66WV51216BLL) (55ns)
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

DESCRIPTION

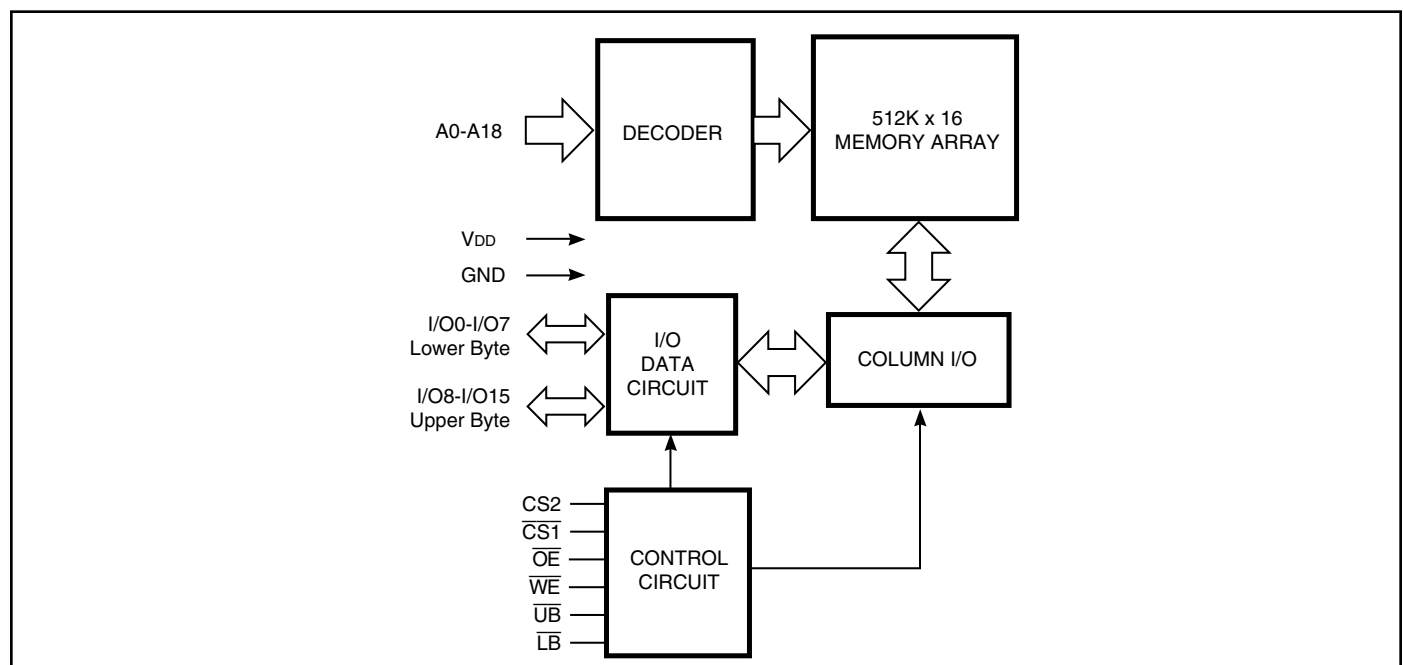
The ISSI IS66WV51216ALL/BLL is a high-speed, 8M bit static RAMs organized as 512K words by 16 bits. It is fabricated using ISSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when $\overline{CS2}$ is LOW (deselected) or when $\overline{CS1}$ is LOW, $\overline{CS2}$ is HIGH and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS66WV51216ALL/BLL is packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II). The device is also available for die sales.

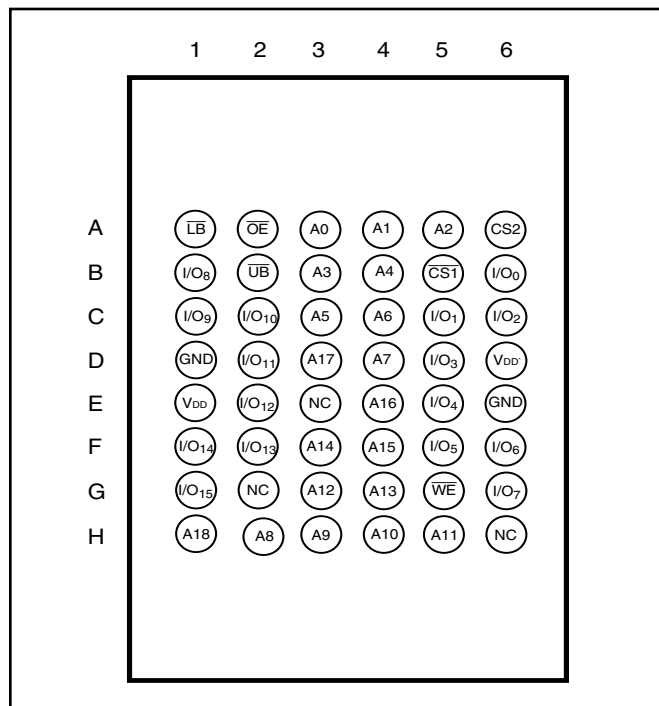
FUNCTIONAL BLOCK DIAGRAM



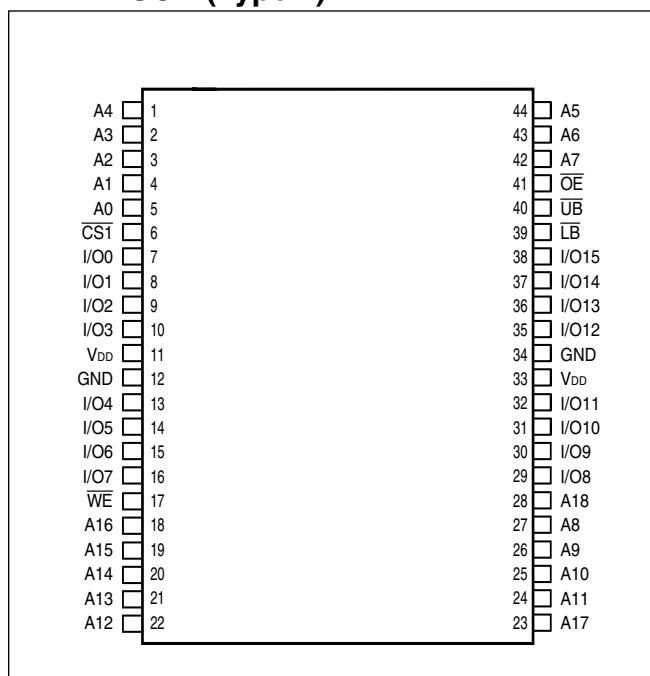
Copyright © 2006 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.

PIN CONFIGURATIONS: 512K x 16

48-Pin mini BGA (6mm x 8mm)



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
CS1, CS2	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
LB	Lower-byte Control (I/O0-I/O7)
UB	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V _{DD} Current
							I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I _{SB1} , I _{SB2}
	X	X	L	X	X	X	High-Z	High-Z	I _{SB1} , I _{SB2}
	X	X	X	X	H	H	High-Z	High-Z	I _{SB1} , I _{SB2}
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I _{CC}
	H	L	H	H	X	L	High-Z	High-Z	I _{CC}
Read	H	L	H	L	L	H	DOUT	High-Z	I _{CC}
	H	L	H	L	H	L	High-Z	DOUT	
	H	L	H	L	L	L	DOUT	DOUT	
Write	L	L	H	X	L	H	DIN	High-Z	I _{CC}
	L	L	H	X	H	L	High-Z	DIN	
	L	L	H	X	L	L	DIN	DIN	

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	(70ns)	(55ns)	(70ns)
Commercial	0°C to +70°C	1.7V - 1.95V	2.5V - 3.6V	
Industrial	-40°C to +85°C	1.7V - 1.95V	2.5V - 3.6V	
Automotive	-40°C to +105°C			2.5V-3.6V

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	−0.2 to V _{DD} +0.3	V
T _{BIAS}	Temperature Under Bias	−40 to +85	°C
V _{DD}	V _{DD} Related to GND	−0.2 to +3.8	V
T _{STG}	Storage Temperature	−65 to +150	°C
P _T	Power Dissipation	1.0	W

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	V _{DD}	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	I _{OH} = −0.1 mA	1.7-1.95V	1.4	—	V
		I _{OH} = −1 mA	2.5-3.6V	2.2	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	1.7-1.95V	—	0.2	V
		I _{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V _{IH}	Input HIGH Voltage		1.7-1.95V	1.4	V _{DD} + 0.2	V
			2.5-3.6V	2.2	V _{DD} + 0.3	V
V _{IL} ⁽¹⁾	Input LOW Voltage		1.7-1.95V	−0.2	0.4	V
			2.5-3.6V	−0.2	0.6	V
I _{LI}	Input Leakage	GND ≤ V _{IN} ≤ V _{DD}		−1	1	μA
I _{LO}	Output Leakage	GND ≤ V _{OUT} ≤ V _{DD} , Outputs Disabled		−1	1	μA

Notes:

1. V_{IL} (min.) = −1.0V for pulse width less than 10 ns.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	10	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	1.7V-1.95V (Unit)	2.5V-3.6V (Unit)
Input Pulse Level	0.4V to V _{DD} -0.2	0.4V to V _{DD} -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V _{REF}	V _{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.7V - 1.95V	2.5V - 3.6V
R1(Ω)	3070	1029
R2(Ω)	3150	1728
V _{REF}	0.9V	1.4V
V _{TM}	1.8V	2.8V

AC TEST LOADS

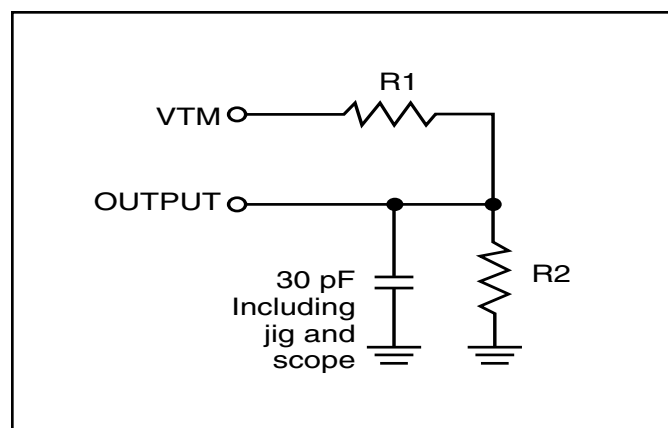


Figure 1

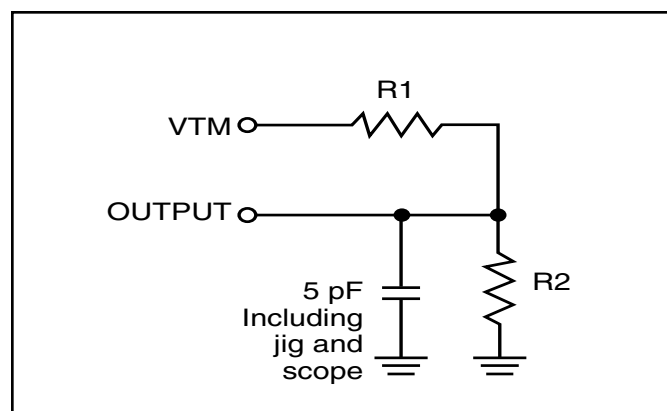


Figure 2

1.7V-1.95V POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 70ns	Unit
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} All Inputs 0.4V or V _{DD} - 0.2V	Com. Ind. Auto. typ. ⁽¹⁾	20 25 30	mA
I _{CC1}	Operating Supply Current	V _{DD} = Max., $\overline{CS1}$ = 0.2V $\overline{WE}$ = V _{DD} - 0.2V CS2 = V _{DD} - 0.2V, f = 1 MHz	Com. Ind. Auto.	4 4 10	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CS1}$ = V _{IH} , CS2 = V _{IL} , f = 1 MHz	Com. Ind. AUTO.	0.6 0.6 1	mA
OR					
	ULB Control	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CS1}$ = V _{IL} , f = 0, $\overline{UB}$ = V _{IH} , $\overline{LB}$ = V _{IH}			
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., $\overline{CS1}$ ≥ V _{DD} - 0.2V, CS2 ≤ 0.2V, V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com. Ind. Auto. typ. ⁽¹⁾	100 120 150	μA
OR					
	ULB Control	V _{DD} = Max., $\overline{CS1}$ = V _{IL} , CS2 = V _{IH} V _{IN} ≥ V _{DD} - 0.2V, or V _{IN} ≤ 0.2V, f = 0; $\overline{UB}$ / $\overline{LB}$ = V _{DD} - 0.2V			

Note:

1. Typical values are measured at V_{DD} = 1.8V, T_A = 25°C and not 100% tested.

2.5V-3.6V POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55ns	Unit
I _{CC}	V _{DD} Dynamic Operating Supply Current	V _{DD} = Max., I _{OUT} = 0 mA, f = f _{MAX} All Inputs 0.4V or V _{DD} – 0.3V	Com. Ind. Auto. typ. ⁽²⁾	25 28 35 15	mA
I _{CC1}	Operating Supply Current	V _{DD} = Max., $\overline{CS1} = 0.2V$ $\overline{WE} = V_{DD} - 0.2V$ CS2 = V _{DD} – 0.2V, f = 1MHz	Com. Ind. Auto.	5 5 10	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CS1} = V_{IH}$, CS2 = V _{IL} , f = 1 MHz	Com. Ind. Auto.	0.6 0.6 1	mA
OR					
	ULB Control	V _{DD} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CS1} = V_{IL}$, f = 0, $\overline{UB} = V_{IH}$, $\overline{LB} = V_{IH}$			
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{DD} = Max., $\overline{CS1} \geq V_{DD} - 0.2V$, CS2 ≤ 0.2V, V _{IN} ≥ V _{DD} – 0.2V, or V _{IN} ≤ 0.2V, f = 0	Com. Ind. Auto. typ. ⁽²⁾	100 130 150 75	μA
OR					
	ULB Control	V _{DD} = Max., $\overline{CS1} = V_{IL}$, CS2=V _{IH} V _{IN} ≥ V _{DD} – 0.2V, or V _{IN} ≤ 0.2V, f = 0; $\overline{UB} / \overline{LB} = V_{DD} - 0.2V$			

Note:

- At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

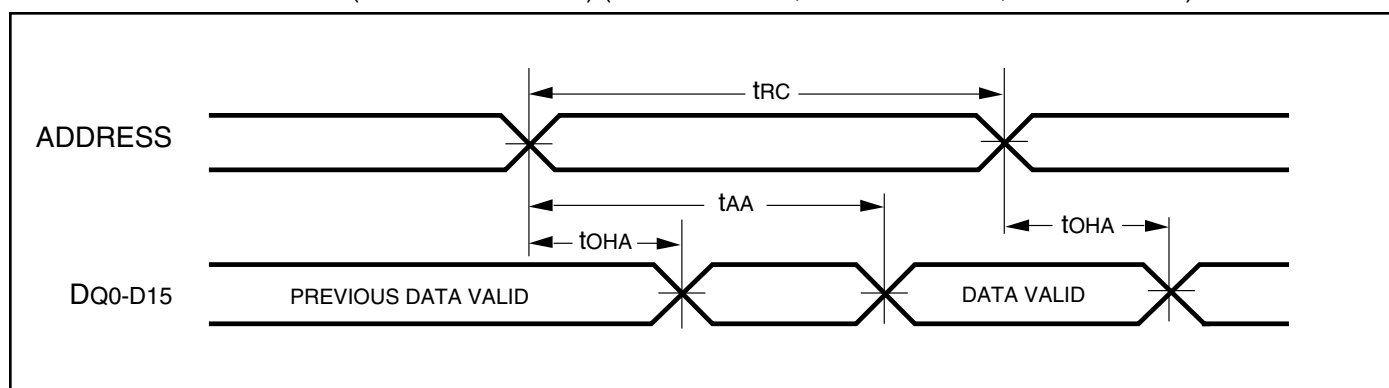
Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}/\overline{CS2}$ Access Time	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
$t_{HZOE}^{(2)}$	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
$t_{LZOE}^{(2)}$	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
$t_{HZCS1}/t_{HZCS2}^{(2)}$	$\overline{CS1}/\overline{CS2}$ to High-Z Output	0	20	0	25	ns
$t_{LZCS1}/t_{LZCS2}^{(2)}$	$\overline{CS1}/\overline{CS2}$ to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}, \overline{UB}$ Access Time	—	55	—	70	ns
t_{HZB}	$\overline{LB}, \overline{UB}$ to High-Z Output	0	20	0	25	ns
t_{LZB}	$\overline{LB}, \overline{UB}$ to Low-Z Output	0	—	0	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to $V_{DD}-0.2V/0.4V$ to $V_{DD}-0.3V$ and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 100 mV from steady-state voltage. Not 100% tested.

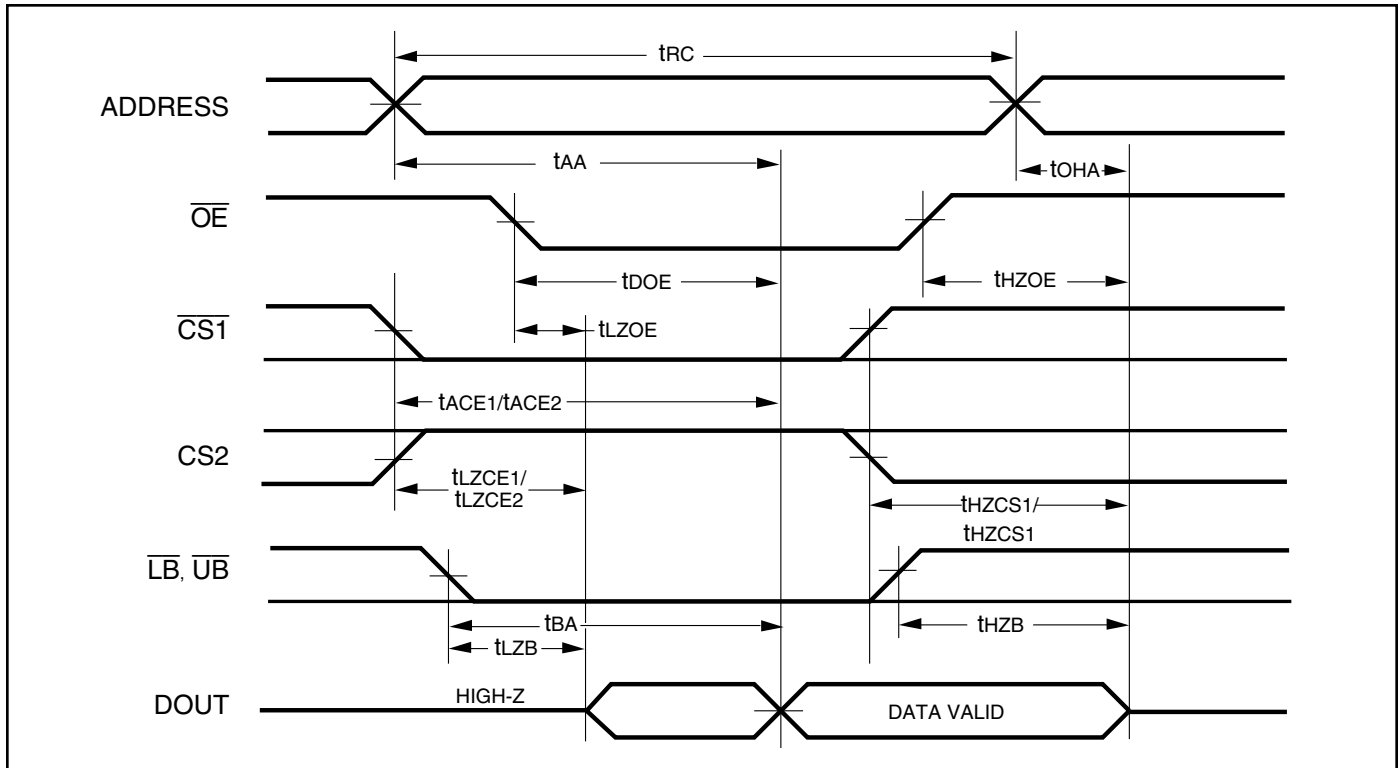
AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CS1} = \overline{OE} = V_{IL}$, $CS2 = \overline{WE} = V_{IH}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$)



AC WAVEFORMS

READ CYCLE NO. 2^(1,3) ($\overline{CS1}$, $CS2$, $\overline{OE}$, AND $\overline{UB}/\overline{LB}$ Controlled)



Notes:

1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB} = V_{IL}$. $CS2 = \overline{WE} = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,2) (Over Operating Range)

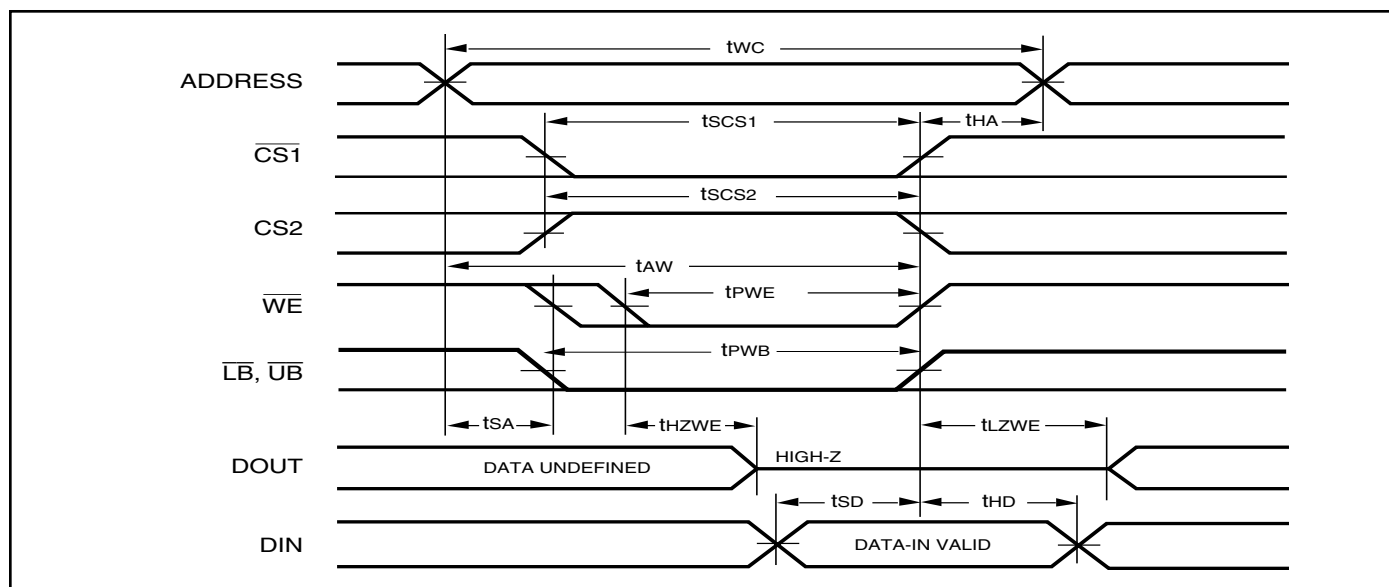
Symbol	Parameter	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	55	—	70	—	ns
t _{SCS1} /t _{SCS2}	$\overline{CS1}/CS2$ to Write End	45	—	60	—	ns
t _{AW}	Address Setup Time to Write End	45	—	60	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	ns
t _{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	45	—	60	—	ns
t _{PWE} ⁽⁴⁾	$\overline{WE}$ Pulse Width	45	—	60	—	ns
t _{SD}	Data Setup to Write End	25	—	30	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	ns
t _{HZWE} ⁽³⁾	$\overline{WE}$ LOW to High-Z Output	—	20	—	30	ns
t _{LZWE} ⁽³⁾	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ± 100 mV from steady-state voltage. Not 100% tested.
4. t_{PWE} > t_{HZWE} + t_{SD} when $\overline{OE}$ is LOW.

AC WAVEFORMS

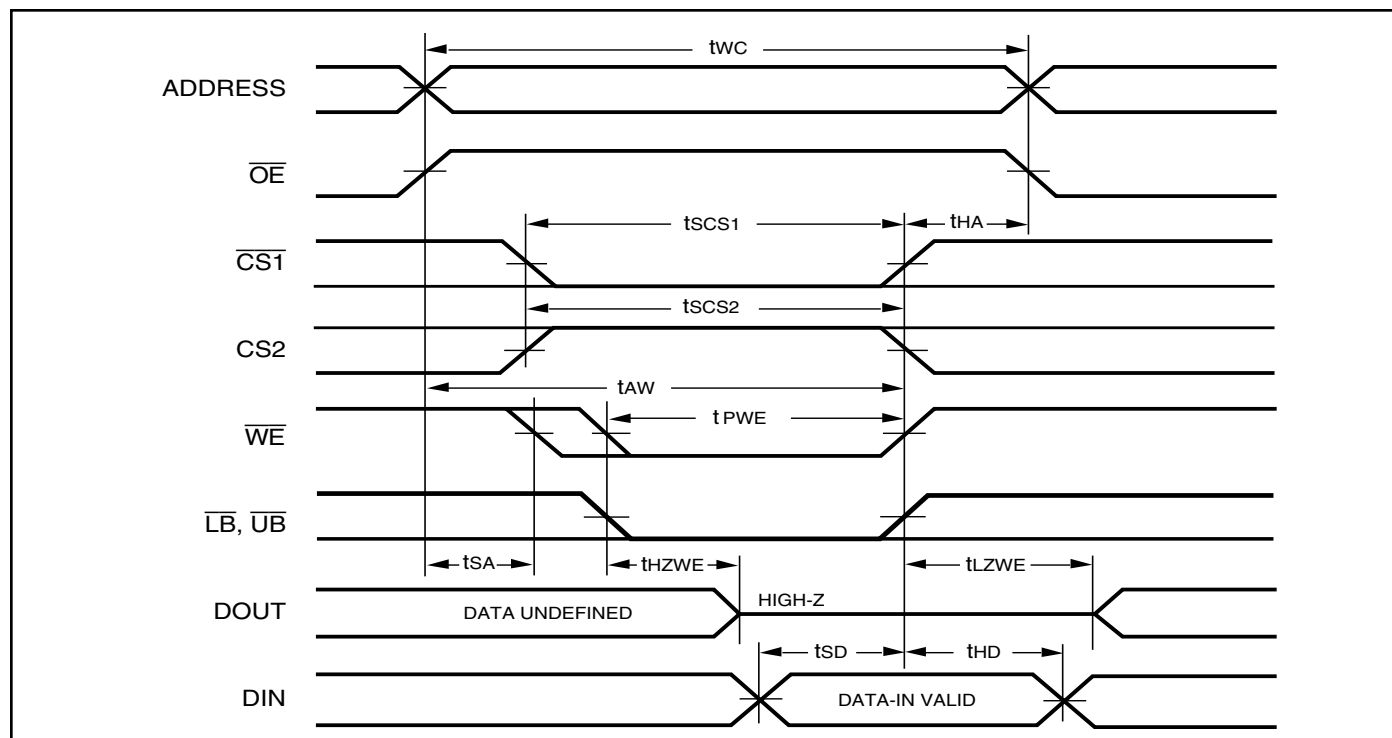
WRITE CYCLE NO. 1^(1,2) ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)



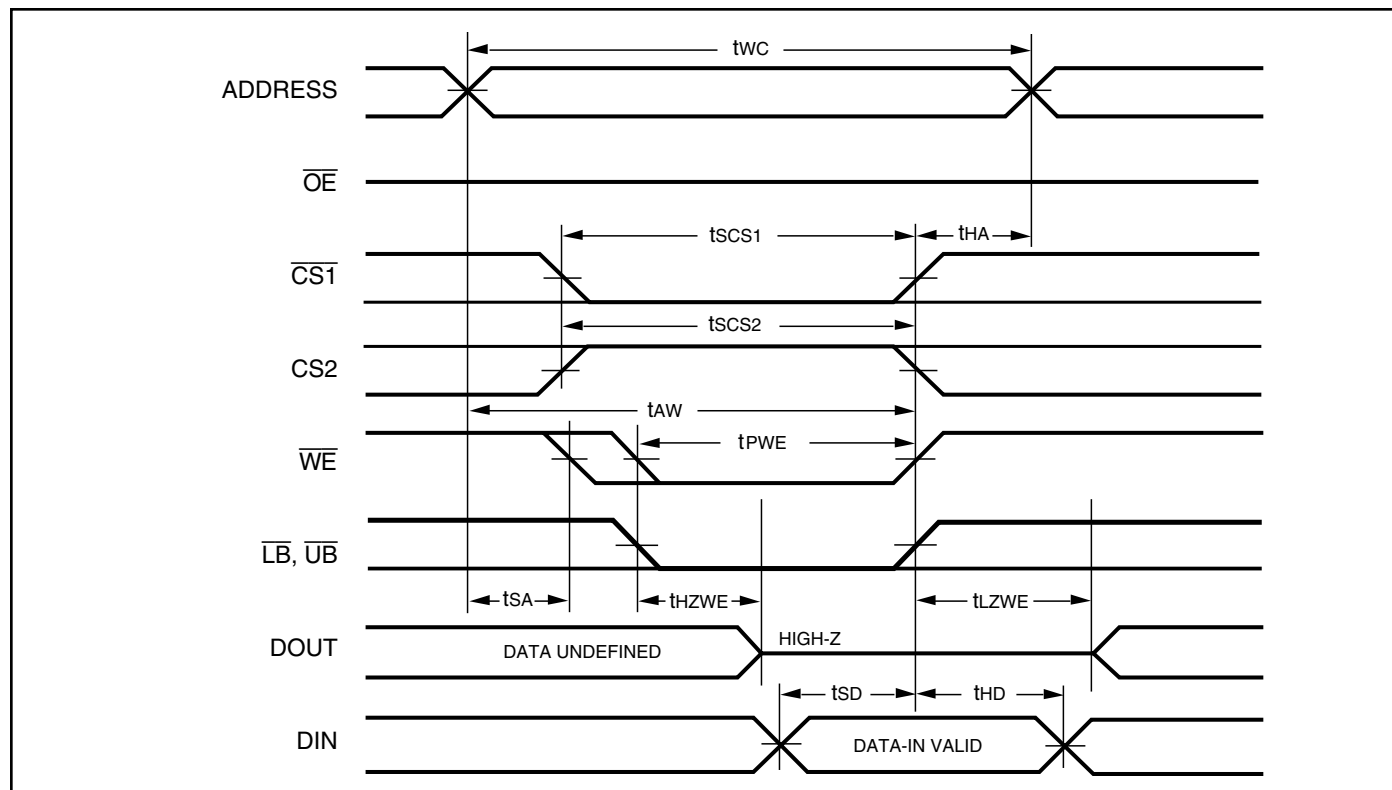
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, CS2 and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = (CS1) [(LB) = (UB)] (WE).

WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{UB}/\overline{LB}$ Controlled)

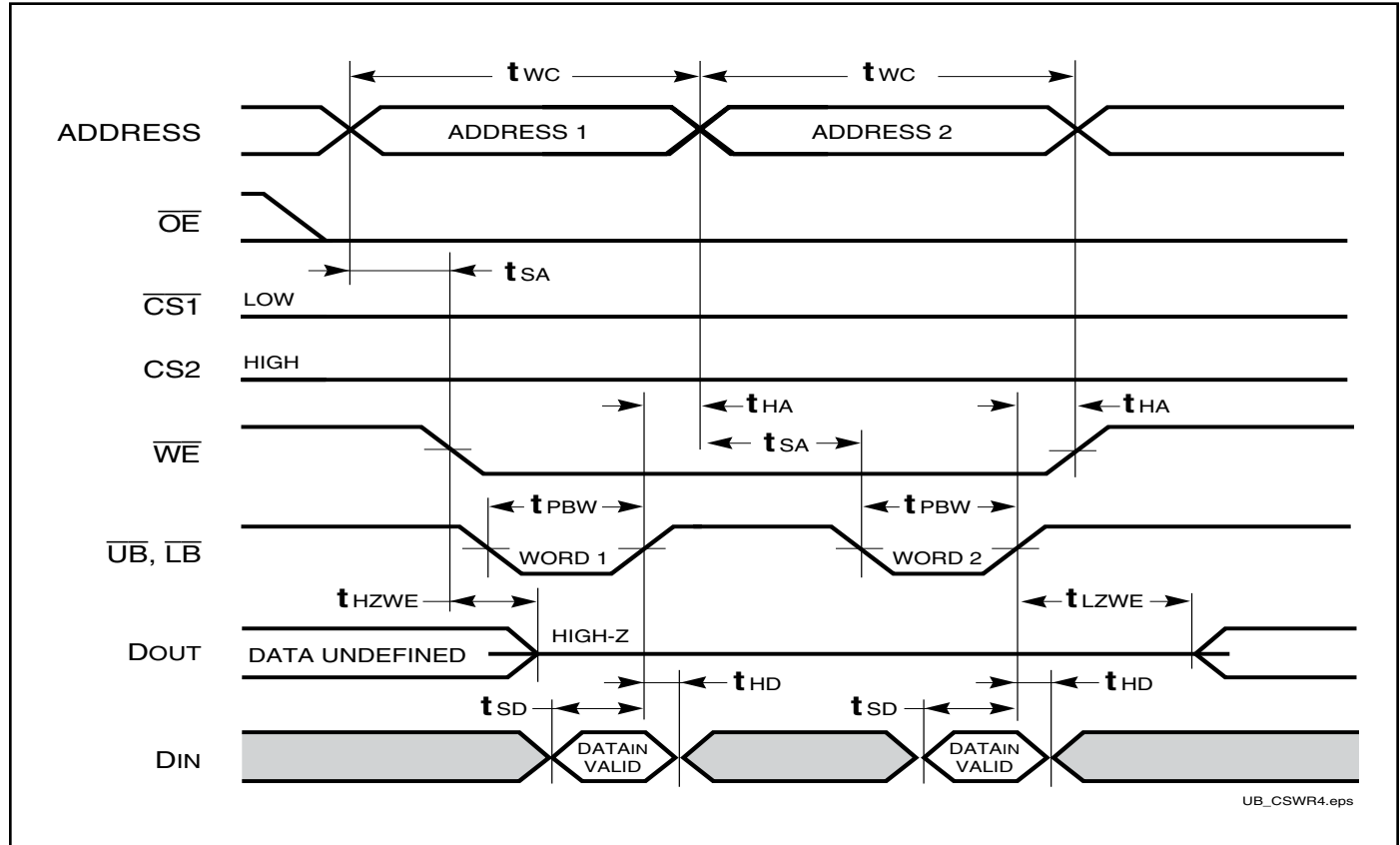


Figure 1: Avoidable Timing

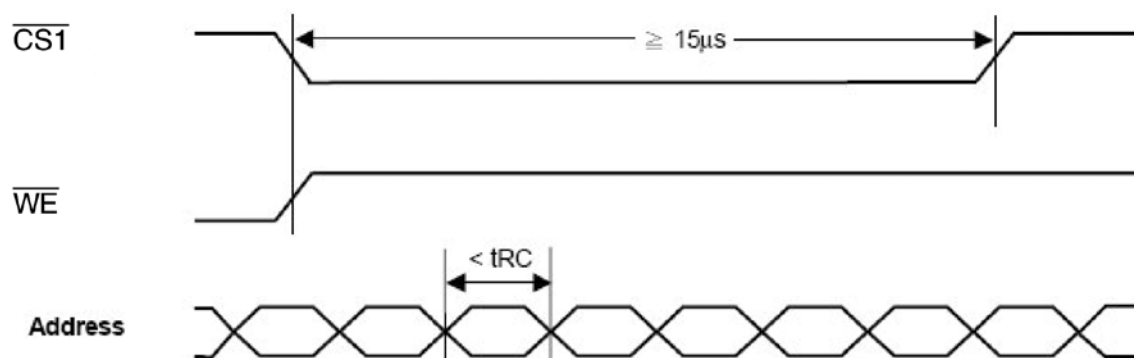


Figure 2:

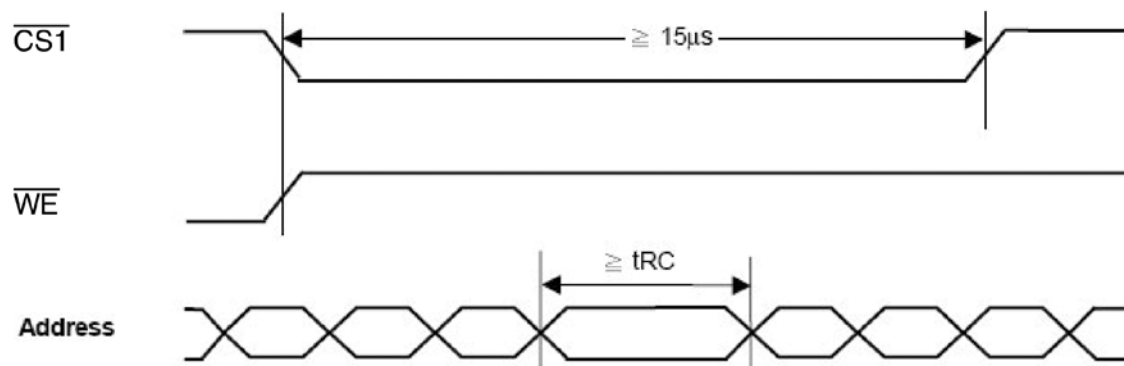
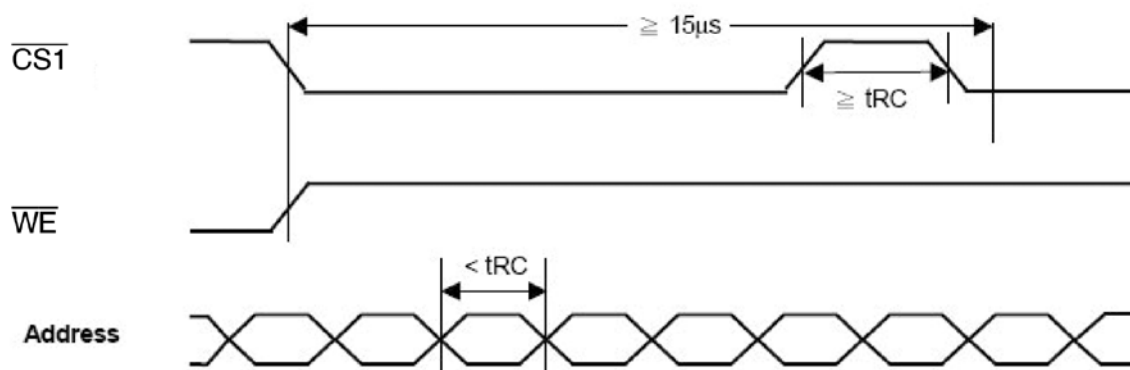


Figure 3:



Please avoid address change for less than t_{RC} during the cycle time longer than $15\mu\text{s}$ (Figure 1). Figure 2 & 3 provide work around solution for this issue.

IS66WV51216ALL

Industrial Range: -40°C to +85°C

Voltage Range: 1.7V to 1.95V

Speed (ns)	Order Part No.	Package
70	IS66WV51216ALL-70TLI	TSOP-II, Lead-free
	IS66WV51216ALL-70BLI	mini BGA (6mm x 8mm), Lead-free

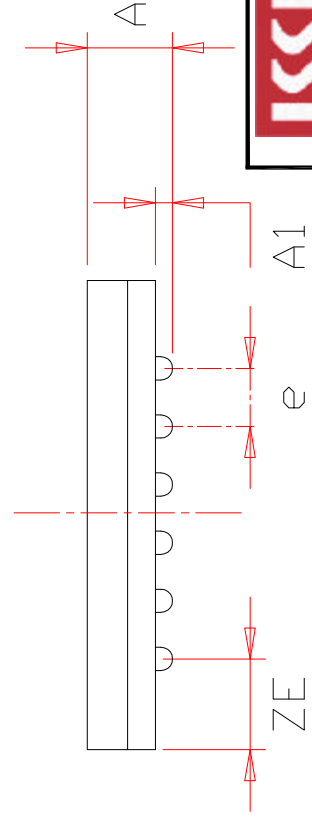
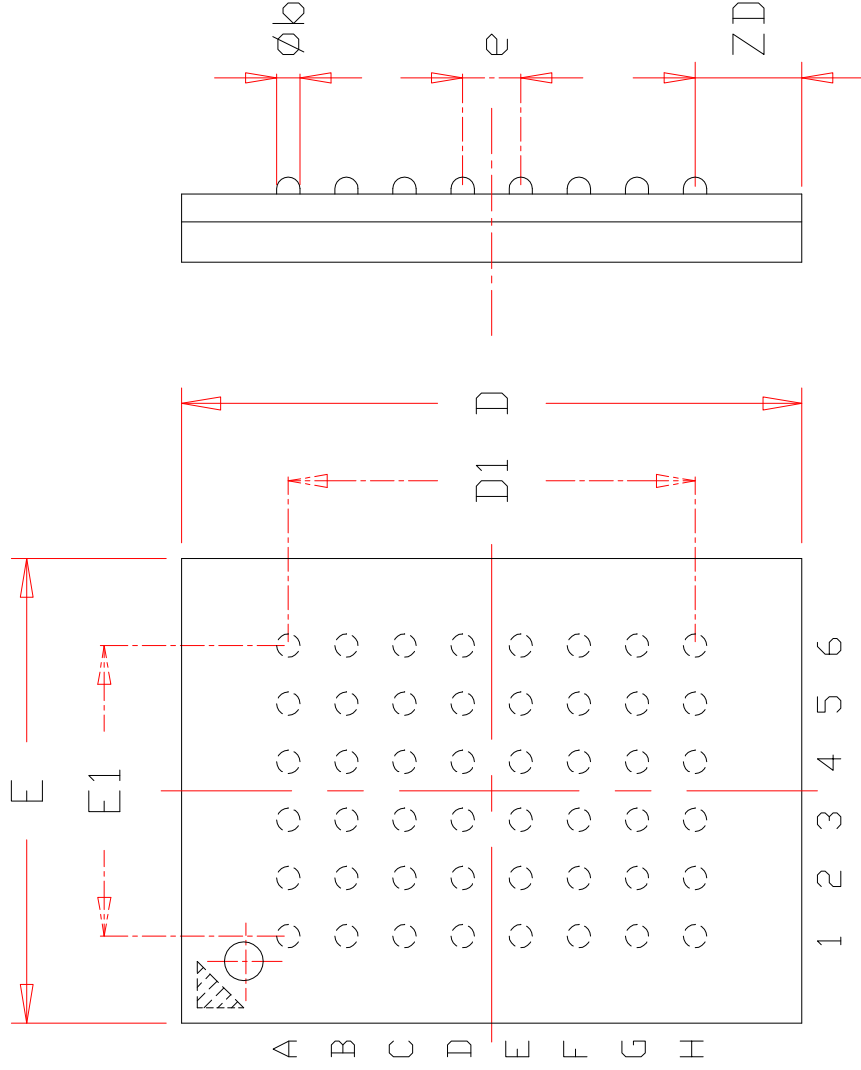
IS66WV51216BLL

Industrial Range: -40°C to +85°C

Voltage Range: 2.5V to 3.6V

Speed (ns)	Order Part No.	Package
55	IS66WV51216BLL-55TLI	TSOP-II, Lead-free
	IS66WV51216BLL-55BLI	mini BGA (6mm x 8mm), Lead-free

TOP VIEW



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH	
	MIN.	NOM.	MAX.	MIN.	NOM. MAX.
A			1,20		0,047
A1	0,20		0,30	0,008	0,012
øb	0,30	0,35	0,40	0,012	0,014 0,016
D	7,90	8,00	8,10	0,311	0,315 0,319
D1	5,25 BSC			0,207 BSC	
E	5,90	6,00	6,10	0,232	0,236 0,240
E1	3,75 BSC			0,148 BSC	
e	0,75 BSC.			0,030 BSC.	
ZD	1,375 REF.			0,054 REF.	
ZE	1,125 REF.			0,044 REF.	

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



TITLE

48L 6x8mm TF-BGA
Package Outline

REV.

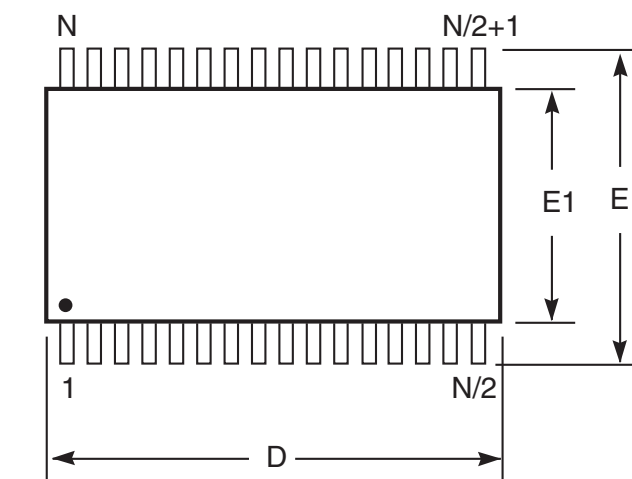
C

DATE

08/12/2008

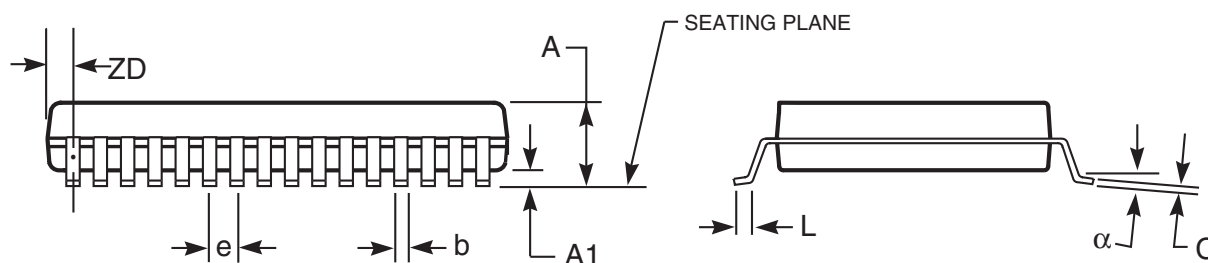
PACKAGING INFORMATION

Plastic TSOP Package Code: T (Type II)



Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

Copyright © 2003 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products.