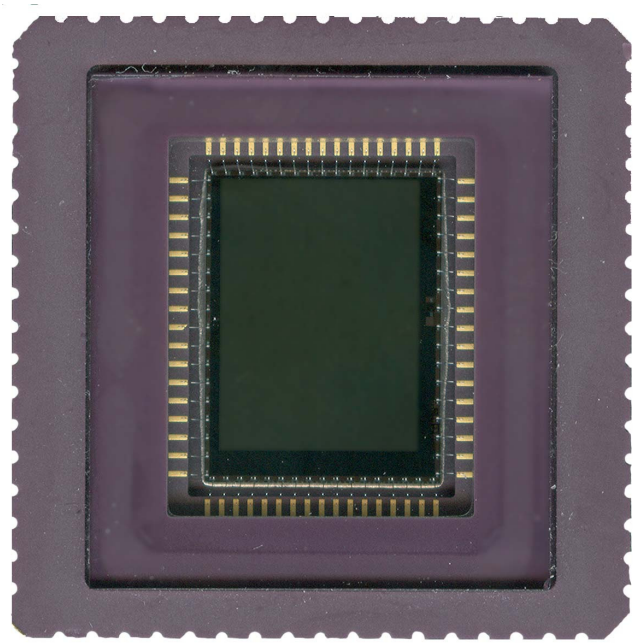
ADVANCE INFORMATION

IBIS4-A-6600
CYII4SM6600AB

6.6 MP CMOS Image Sensor



Features

Table 1. Key Performance Parameters

Parameter	Typical Value
Active Pixels	2210 (H) x 3002 (V)
Pixel Size	3.5 µm x 3.5 µm
Optical format	1 inch
Active Imager Size	7.74 mm x 10.51 mm
Shutter Type	Electronic Rolling Shutter
Maximum Data Rate/Master Clock	40 MPS/40 MHz
Frame rate	5 fps (2210 x 3002) 89 fps (640 x 480)
ADC resolution	ADC resolution
Sensitivity (@ 650 nm)	411 V.m2/W.s, 4.83 V/lux.s
Dynamic Range	59 dB
Full Well Charge	Full Well Charge
Temporal Noise	24 e-
Dark current	3.37 mV/s
High Dynamic Range Modes	Double Slope, Non Destructive Read out (NDR).
Supply Voltage	Analog: 2.5V-3.3V, Digital: 2.5V, I/O: 2.5V
Power consumption	190 mWatt

Table 1. Key Performance Parameters (continued)

Parameter	Typical Value
Operating temperature	–30 °C to +65 °C
Color Filter Array	Mono, RGB Bayer Pattern
Packaging	68-pins LCC

Description

The IBIS4-6600 is a solid -state CMOS image sensor that integrates the functionality of complete analog image acquisition, digitizer and digital signal processing system on a single chip. The image sensor compromises a 6.6 MPixel resolution with 2210x3002 active pixels. The image size is fully programmable to user-defined windows of interest. The pixels are on a 3.5-µm pitch. The sensor is available in a Monochrome version or Bayer (RGB) patterned color filter array.

User-programmable row and column start/stop positions allow windowing down to 2x1 pixel window for digital zoom. Sub sampling reduces resolution while maintaining the constant field of view. The analog video output of the pixel array is processed by an on-chip analog signal pipeline. Double Sampling (DS) eliminates the fixed pattern noise. The programmable gain and offset amplifier maps the signal swing to the ADC input range. A 10-bit ADC converts the analog data to a 10-bit digital word stream. The sensor uses a 3-wire Serial-Parallel (SPI) interface. It operates with a single 2.5V power supply and requires only one master clock for operation up to 40 MHz. It is housed in a 68-pin ceramic LCC package.

This data sheet allows the user to develop a camera system based on the described timing and interfacing.

Applications

- Machine vision
- Biometry
- Document scanning

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Specifications

General Specifications

Table 2. General Specifications.

Parameter	Specification	Remarks
Pixel architecture	3T-pixel	
Pixel size	3.5 m x 3.5 m	The resolution and pixel size results in a 7.74 mm x 10.51 mm optical active area.
Resolution	2210 x3002	
Pixel rate	40 MHz	Using a 40- MHz system clock and 1 or 2 parallel outputs.
Shutter type	Electronic rolling shutter	
Full frame rate	5 frames/second	Increases with ROI read out and/or sub sampling.

Electro-optical specifications

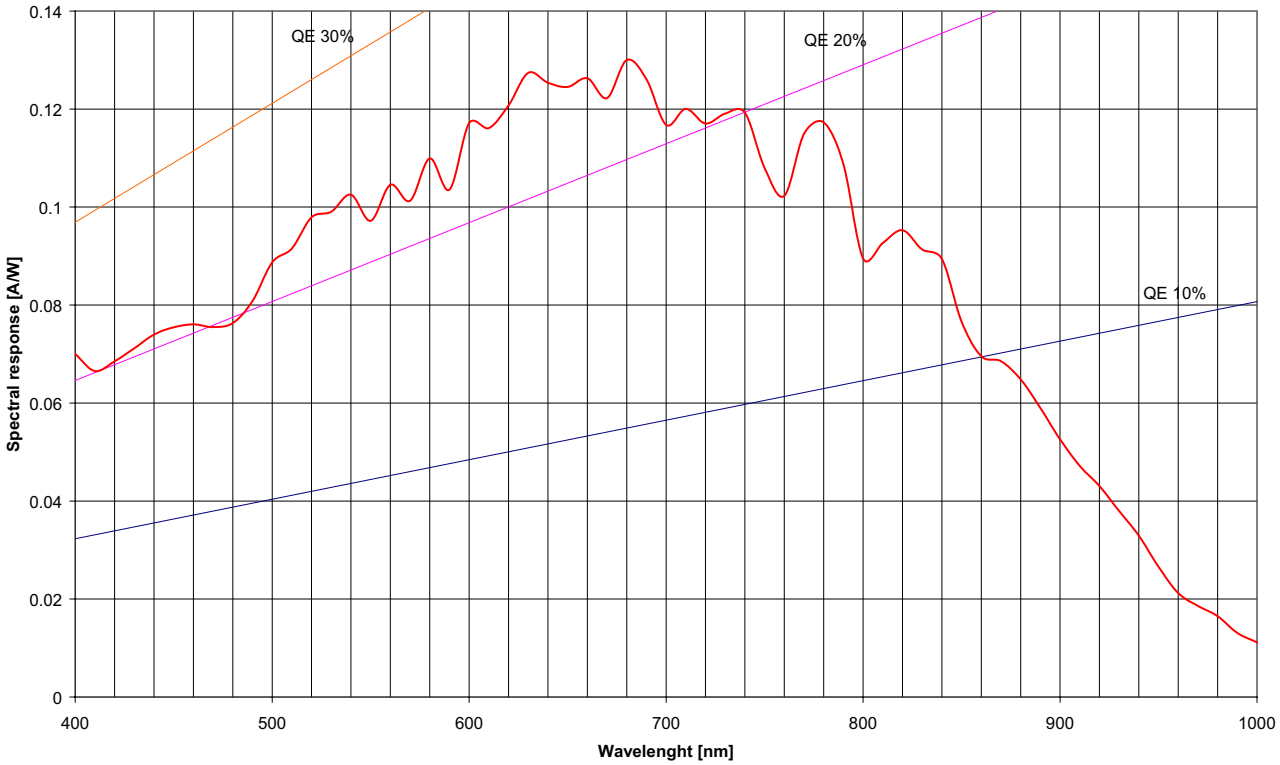
Overview

Table 3. Electro-optical Specifications

Parameter	Specification	Remarks
FPN (local)	<0.20%	RMS% of saturation signal.
PRNU (local)	<1.5%	RMS of signal level.
Conversion gain	Conversion gain	@ output (measured).
Output signal amplitude	0.6V	At nominal conditions.
Saturation charge	21.500 e-	
Sensitivity (peak)	411V.m2/W.s 4.83 V/lux.s	@ 650 nm (85 lux = 1 W/m2).
Sensitivity (visible)	328 V.m2/W.s 2.01 V/lux.s	400-700 nm (163 lux = 1 W/m2).
Peak QE * FF Peak Spectral Resp.	25% 0.13 A/W	Average QE*FF = 22% (visible range). Average SR*FF = 0.1 A/W (visible range). See spectral response curve.
Fill factor	35%	Light sensitive part of pixel (measured).
Dark current	3.37 mV/s 78 e-/s	Typical value of average dark current of the whole pixel array (@ 21 °C).
Dark Signal Non Uniformity	8.28 mV/s 191 e-/s	Dark current RMS value (@ 21 °C).
Temporal noise	24 RMS e-	Measured at digital output (in the dark).
S/N Ratio	895:1 (59 dB)	Measured at digital output (in the dark).
Spectral sensitivity range	400 - 1000 nm	
Optical cross talk	15% 4%	To the first neighboring pixel. To the second neighboring pixel.
Power dissipation	190 mWatt	Typical (including ADCs).

Spectral Response Curve

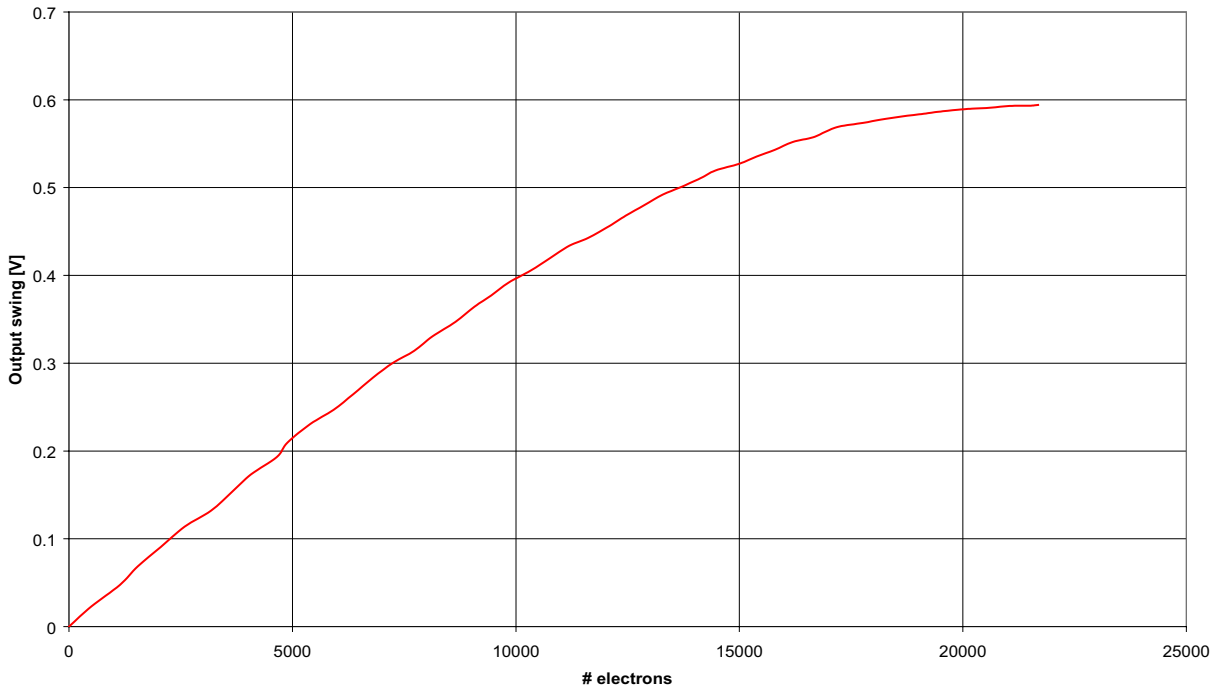
Figure 1. Spectral Response Curve



Spectral Response Curve on page 6 shows the spectral response characteristic. The curve is measured directly on the pixels. It includes effects of non-sensitive areas in the pixel, e.g., interconnection lines. The sensor is light sensitive between 400 and 1000 nm. The peak QE * FF is 25% approximately around 650 nm. In view of a fill factor of 35%, the QE is thus close to 70% between 500 and 700 nm.

Electro-voltaic Response Curve

Figure 2. Electro-voltaic Response Curve



Electro-voltaic Response Curve on page 7 shows the pixel response curve in linear response mode. This curve is the relation between the electrons detected in the pixel and the output signal. The resulting voltage-electron curve is independent of any parameters (integration time, etc). The voltage to electrons conversion gain is 43 µV/electron.

Features and General Specifications

Table 4. Features and General Specifications

Feature	Specification/Description
Electronic shutter type	Rolling shutter.
Integration time control	60 µs - 1/frame period.
Windowing (ROI)	Randomly programmable ROI read out.
Sub-sampling modes:	Several sub sample modes can be programmed (see 2.6).
Extended dynamic range	Dual slope (up to 90 dB optical dynamic range) and non-destructive read out mode.
Analog output	The output rate of 40 Mpixels/s can be achieved with 2 analog outputs each working at 20 Mpixel/s.
Digital output	2 on-chip 10-bit ADCs @ 20 Msamples/s are multiplexed to 1 digital 10 bit output @ 40 Msamples/s.
Supply voltage VDD	Nominal 2.5V (some supplies require 3.3V for extended dynamic range).
Logic levels	2.5V.
Interface	Serial-to Parallel Interface (SPI).
Package	68-pins LCC.

Electrical Specifications

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VDD	DC supply voltage	–0.5 to 3.3	V
VIN	DC input voltage	–0.5 to (VDD + 0.5)	V
VOUT	DC output voltage	–0.5 to (VDD + 0.5)	V
IIO	DC current drain per pin; any single input or output.	± 50	mA
TL	Lead temperature (5 seconds soldering).	350	°C
TST	Storage temperature	–30 to +85	°C
H	Humidity (relative)	85% at 85 °C	
ESD	ESD susceptibility	2000	V

VDD = VDDD = VDDA (VDDD is supply to digital circuit, VDDA to analog circuit).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Max.
VDD	DC supply voltage	2.5	2.5	3.3	V
TA	Commercial operating temperature.	–30	24	+65	°C

All parameters are characterized for DC conditions after thermal equilibrium has been established.

Unused inputs must always be tied to an appropriate logic level, e.g., either VDD or GND.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high-impedance circuit.

DC Electrical Conditions

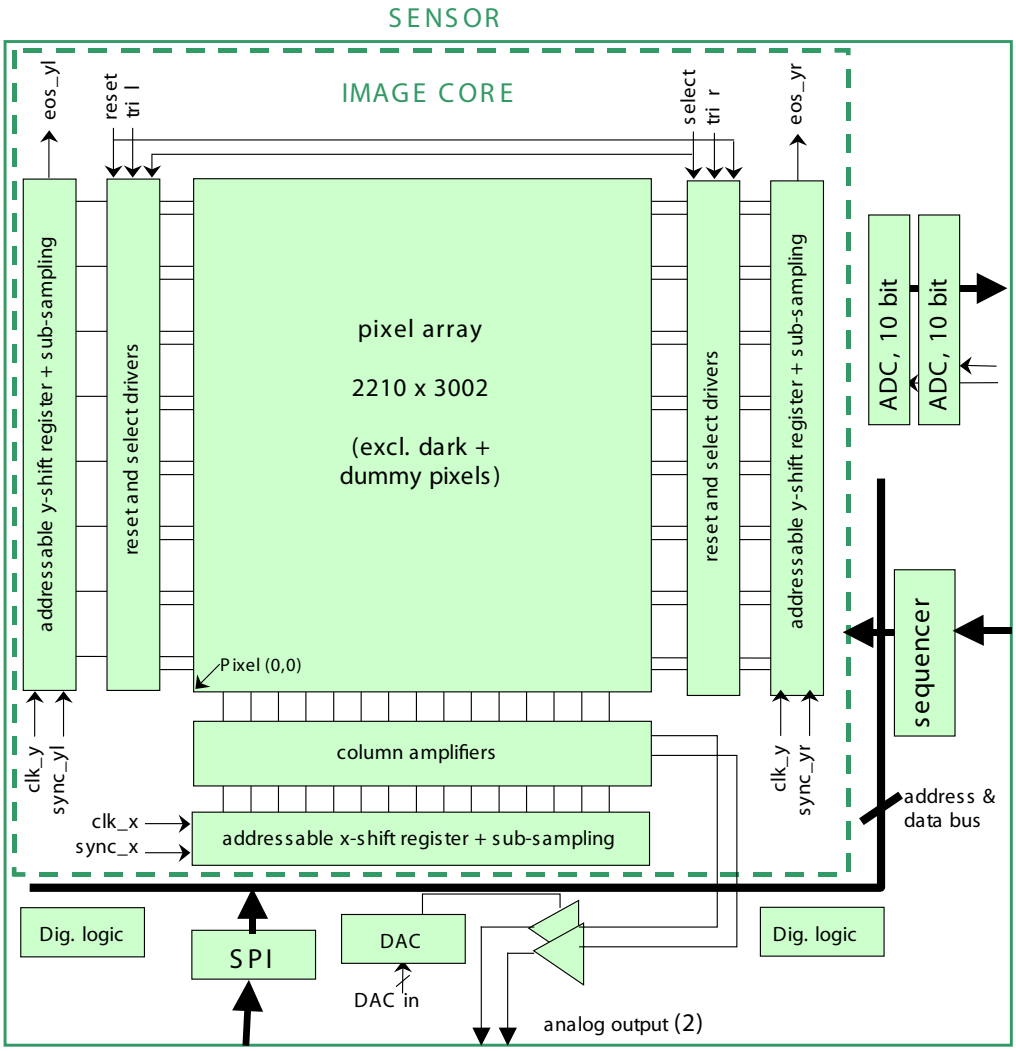
Table 7. DC Electrical Conditions

Symbol	Characteristic	Condition	Min.	Max.	Unit
VIH	Input high voltage		VDD-0.5		V
VIL	Input low voltage		–0.6	0.6	V
IIN	Input leakage current	VIN = VDD or GND	–10	+10	?A
VOH	Output high voltage	VDD=min; IOH= –100 mA	VDD-0.5		V
VOL	Output low voltage	VDD=min; IOH= 100 mA		0.5	V
IDD	Operating current	System clock <= 40 MHz	70	80	mA

Sensor Architecture and Operation

Floor Plan

Figure 3. Floor Plan



Floor Plan on page 9 shows the architecture of the image sensor that has been designed. It consists basically of the pixel array, shift registers for the readout in x and y direction, parallel analog output amplifiers, and column amplifiers that correct for the fixed pattern noise caused by threshold voltage non-uniformities. Reading out the pixel array starts by applying a y clock pulse to select a new row, followed by a calibration sequence to calibrate the column amplifiers (row blanking time). Depending on external bias resistors and timing, typically this sequence takes about 7 s per line (baseline). This sequence is necessary to remove the Fixed Pattern Noise of the pixel and of the column amplifiers themselves (by means of a Double Sampling technique). Pixels can also be read out in a non-destructive manner. Two DACs have been added to make the offset level of the pixel values adjustable and equal for the two output busses. A third DAC is used to connect the busses to a stable voltage during the row blanking period (or to the reset busses continuously in case of non-destructive readout). Two 10-bit ADCs running at 20 Msamples/s will convert the analog pixel values. The digital outputs will be multiplexed to 1 digital 10-bit output at 40 Msamples/s. Note that these blocks are electrically completely isolated from the sensor part (except for the multiplexer for which the settings are uploaded through the shared address and data bus).

The x and y shift registers do have a programmable starting point. The starting point's possibilities are limited due to limitations imposed by sub-sampling requirements. The upload of the start address is done through the serial to parallel interface.

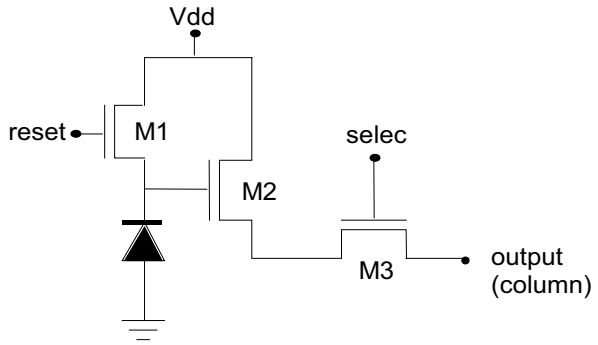
Most of the signals for the image core in Floor Plan on page 9 are generated on chip by the sequencer. This sequencer also allows running the sensor in basic modes, not fully autonomously.

Pixel

Architecture

The pixel architecture is the classical three-transistor pixel as shown in 3T Pixel Architecture on page 10 The pixel has been implemented using the high fill factor technique as patented by FillFactory (US patent No. 6,225,670 and others).

Figure 4. 3T Pixel Architecture



FPN and PRNU

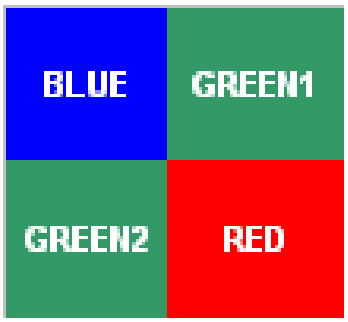
Fixed Pattern Noise correction is done on-chip. Raw images taken by the sensor typically feature a residual (local) FPN of 0.35% RMS of the saturation voltage.

The Photo Response Non Uniformity (PRNU), caused by mismatch of photodiode node capacitances, is not corrected on chip. Measurements indicate that the typical PRNU is about 1.5% RMS of the signal level.

Color filter array

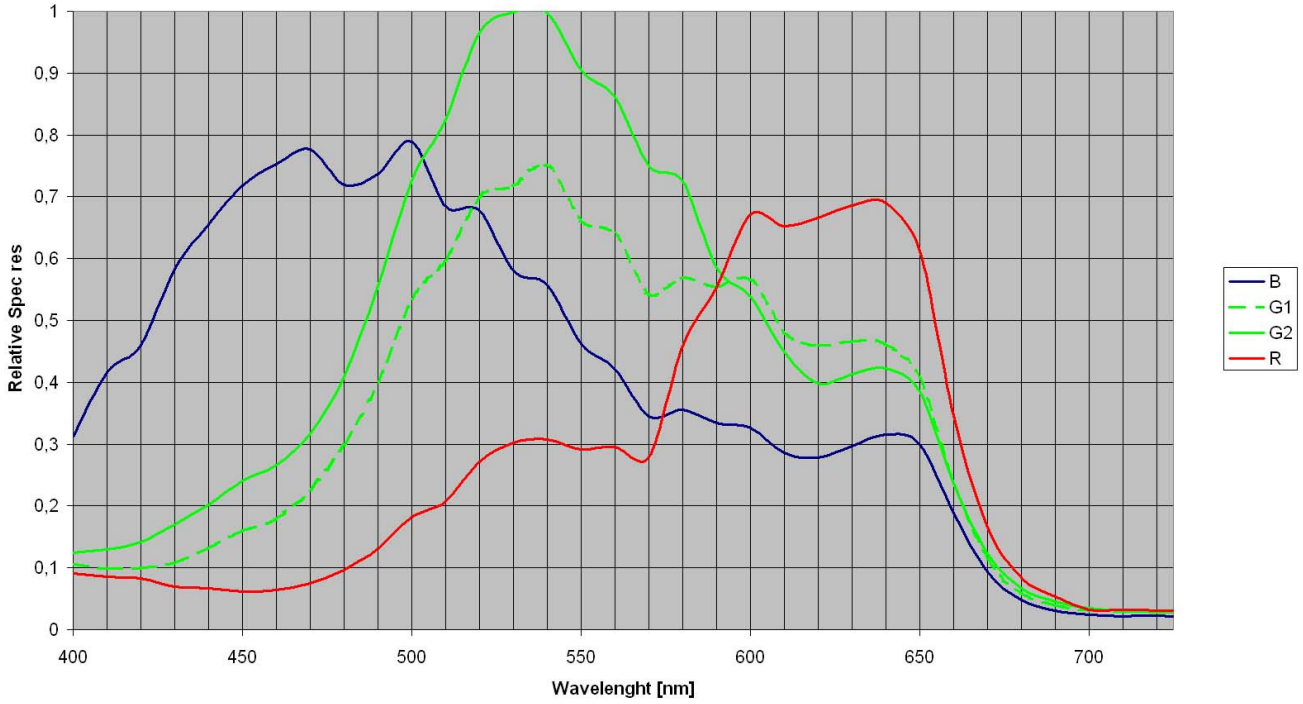
The IBIS4-6600 can also be processed with a Bayer RGB color pattern. Pixel (0,0) has a green filter and is situated on a green-red row. Green1 and green2 are separately processed color filters and have a different spectral response. Green1 pixels are located on a blue-green row, green2 pixels are located on a green-red row.

Figure 5. RGB Bayer Alignment



Typical Response Curve of the RGB Filters on page 10 below shows the response of the color filter array as function of the wavelength. Note that this response curve includes the optical cross talk and the NIR filter of the color glass lid as well (see

Figure 6. Typical Response Curve of the RGB Filters

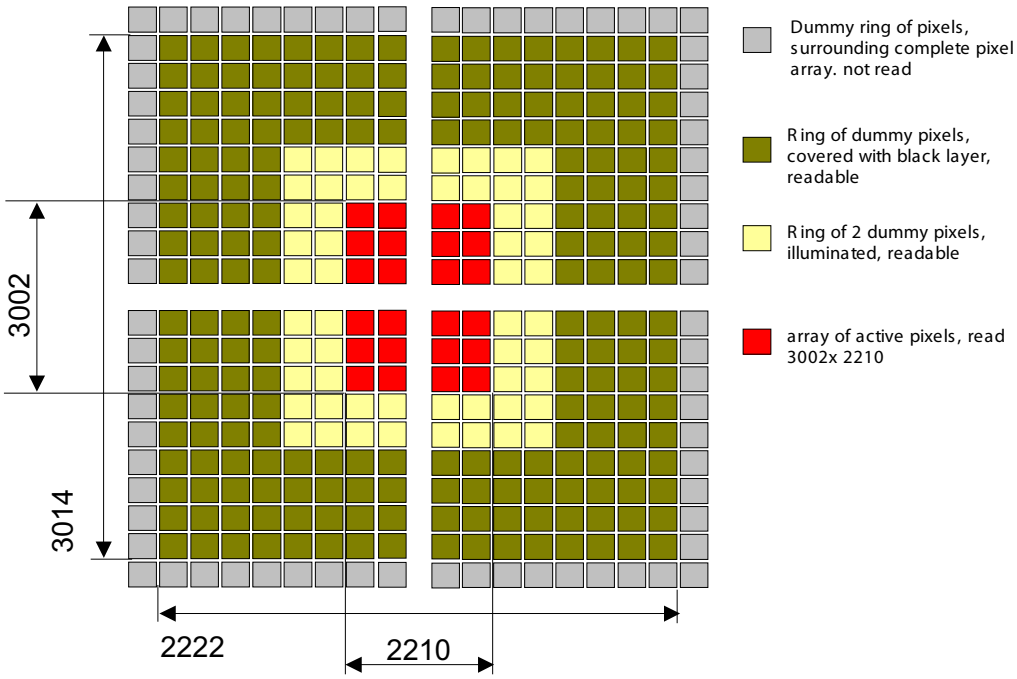


Dark and Dummy Pixels

Floor Plan Pixel Array on page 11 shows a plan of the pixel array. The sensor has been designed in "portrait" orientation. A ring of dummy pixels surrounds the active pixels.

Black pixels are implemented as "optical" black pixels.

Figure 7. Floor Plan Pixel Array



Pixel Rate

The pixel rate for this sensor is high enough to support a frame rate of >75 Hz for a window size of 640 x 480 pixels (VGA format) + 23 pixels over scan in both directions. Taking into account a row blanking time of 7.2 s (as baseline, see also 2.10.2.1.g.), this requires a minimum pixel rate of nearly 40 MHz. The final bandwidth of the column amplifiers, output stage etc. is determined by external bias resistors. Taken into account a pixel rate of 40 MHz a full frame rate of a little more than 5 frames/s will be obtained.

The frame period of the IBIS4-6600 sensor can be calculated as follows:

=> Frame period = (Nr. Lines * (RBT + pixel period * Nr. Pixels))

With:

Nr. Lines: Number of Lines read out each frame (Y).

Nr. Pixels: Number of pixels read out each line (X).

RBT: Row Blanking Time = 7.2 us (typical).

Pixel period: 1/40 MHz = 25 ns.

Example: read out time of the full resolution at nominal speed (40 MHz pixel rate):

=> Frame period = (3002 * (7.2 us + 25 ns * 2210)) = 187.5 ms => 5.33 fps.

Region of Interest (ROI) Read Out

Windowing can easily be achieved by uploading the starting point of the x- and y-shift registers in the sensor registers (see 2.9.1). This downloaded starting point initiates the shift register in the x- and y-direction triggered by the Y_START (initiates the Y-shift register) and the Y_CLK (initiates the X-shift register) pulse. The minimum step size for the x-address is 24 (only even start addresses can be chosen) and 1 for the Y-address (every line can be addressed). The frame rate increases almost linearly when fewer pixels are read out. Table 8. gives an overview of the achievable frame rates with ROI read out.

Table 8. Frame Rate vs. Resolution

Image Resolution (Y*X)	Frame rate [frames/s]	Frame readout time [ms]	Comment
3002 x 2210	5	187.5	Full resolution.
1501 x 1104	14	67	ROI read out.
640 x 480	89	11	11

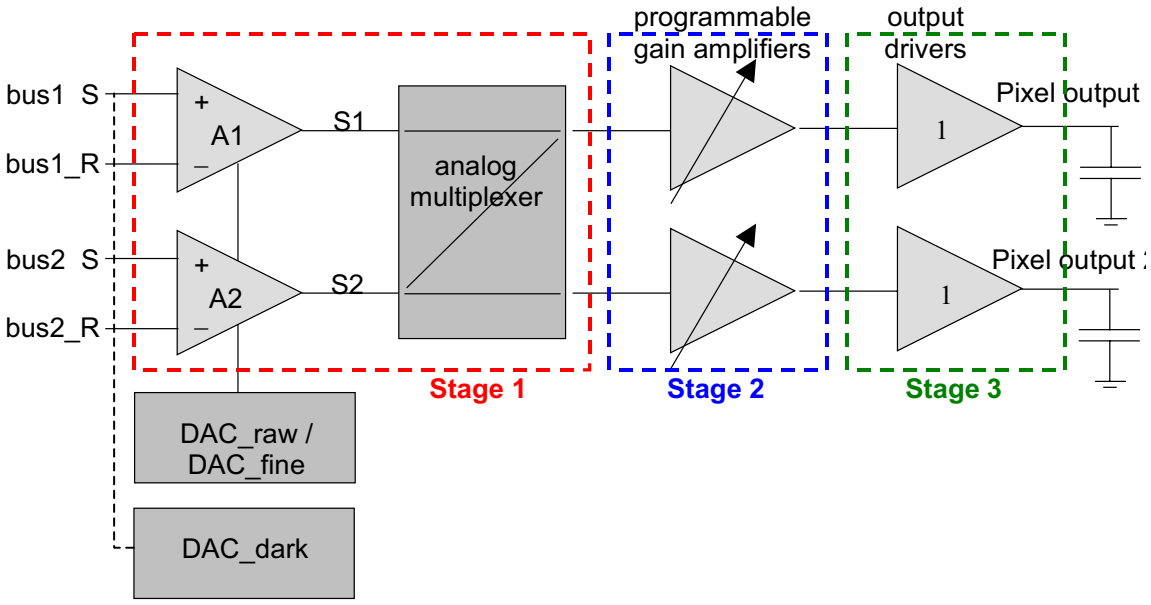
Output Amplifier

The output amplifier subtracts the reset and signal voltages from each other to cancel FPN as much as possible (Figure 8.). The DAC that is used for offset adjustment consists of 2 DACs. One is used for the main offset (DAC_raw) and the other allows for fine tuning to compensate the offset difference between the signal paths arriving at the two amplifiers A1 and A2 (DAC_fine). With the analog multiplexer the signals S1 and S2 from the two busses can be combined to one pixel output at full pixel rate (40 MHz). The two analog signals S1 and S2 can, however, also be available on two separate output pins to allow a higher pixel rate.

The third DAC (DAC_dark) puts its value on the busses during the calibration of the output amplifier. In case of non-destructive readout (no double sampling), bus1_R and bus2_R are continuously connected to the output of the DAC_fine to provide a reference for the signals on bus1_S and bus2_S.

The complete output amplifier can be put in standby by setting the corresponding bit in the AMPLIFIER register.

Figure 8. Output Amplifier Architecture



Stage 1: Offset, FPN Correction and Multiplexing

In the first stage, the signals from the busses are subtracted and the offset from the DACs is added. After a system reset, the analog multiplexer is configured for two outputs (see bit settings of the AMPLIFIER register). In case ONE_OUT is set to 1, the two signals S1 and S2 are multiplexed to one output (output 1). The amplifiers of stage 2 and stage 3 of the second output path are then put in standby. The speed and power consumption of the first stage is controllable through the resistor connected to CMD_OUT_1.

Stage 2: Programmable Gain Amplifier

The second stage provides the gain, which will be adjustable between 1.36 and 17.38 in steps of roughly 20.25 (~1.2). An overview of the gain settings is given in Table 9. . The speed and power consumption of the second stage is controllable through the resistor connected to CMD_OUT_2.

Table 9. PGA Gain Settings

Bits	DC Gain	Bits	DC Gain
0000	1.36	1000	5.40
0001	1.64	1001	6.35
0010	1.95	1010	7.44
0011	2.35	1011	8.79
0100	2.82	1100	10.31
0101	3.32	1101	12.36
0110	3.93	1110	14.67
0111	4.63	1111	17.38

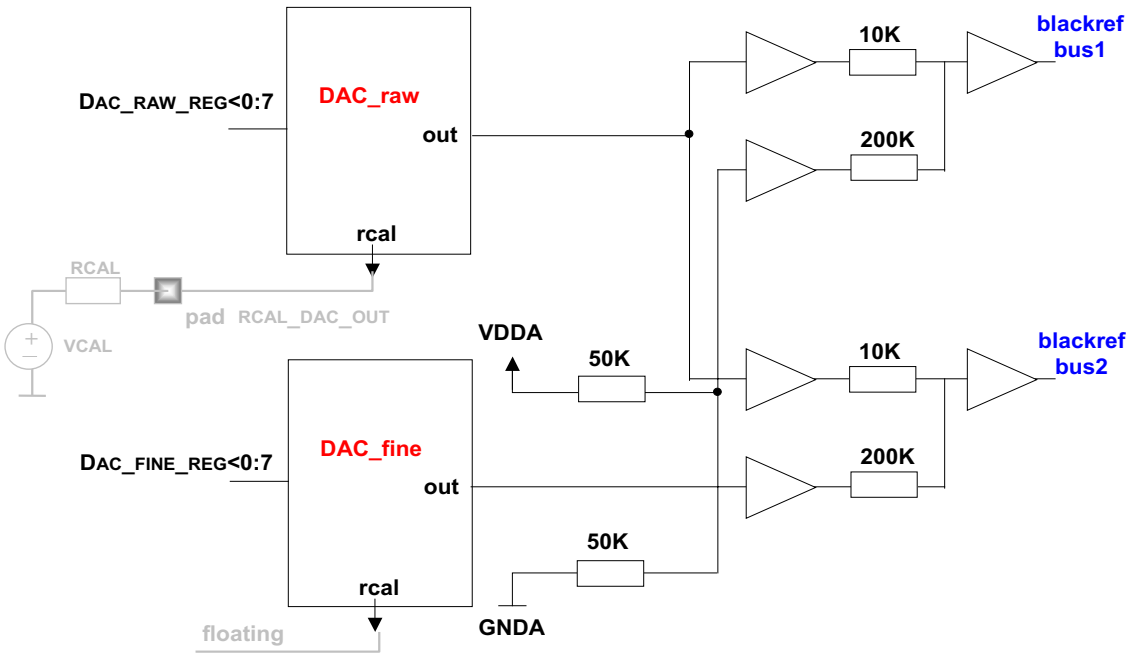
Stage 3: Output Drivers

The speed and power consumption of the third stage is controllable through the resistor connected to CMD_OUT_3. The output drivers are designed to drive a 20-pF output load at 40 Msamples/s with a bias resistor of 100 k?.

Offset DACs

Figure 9. shows how the DAC registers influence the black reference voltages of the two different channels. The offset is mainly given through DAC_raw. DAC_fine can be used to shift the reference voltage of bus 2 up or down to compensate for different offsets in the two channels.

Figure 9. Offset for the Two Channels through DAC_RAW and DAC_FINE



Assume that Voutfull is the voltage that depends on the bit values that are applied to the DAC and ranges from

$$V_{outfull} : 0 \ (bit\ values\ 00000000\ ) \ \rightarrow \ VDDA\ (1-\frac{1}{2^8})\ (bit\ values\ 11111111\ )$$

Externally, the output range of DAC_raw can be changed by connecting a resistor Rcal to RCAL_DAC_OUT and applying a voltage Vcal. The output voltage Vout of DAC_raw follows relation (R = 10 kΩ)

$$V_{out} = \frac{R + R_{cal}}{2R + R_{cal}} V_{outfull} + \frac{R}{2R + R_{cal}} V_{cal}$$

Special case:

Rcal = then Vout = Voutfull (e.g. for DAC_fine)

Rcal = 0, Vcal = GND..... then Vout = Voutfull/2

A similar relation holds for the output range of DAC_DARK (RCAL_DAC_DARK can be used to tune the output range of this DAC).

Analog to Digital Converter

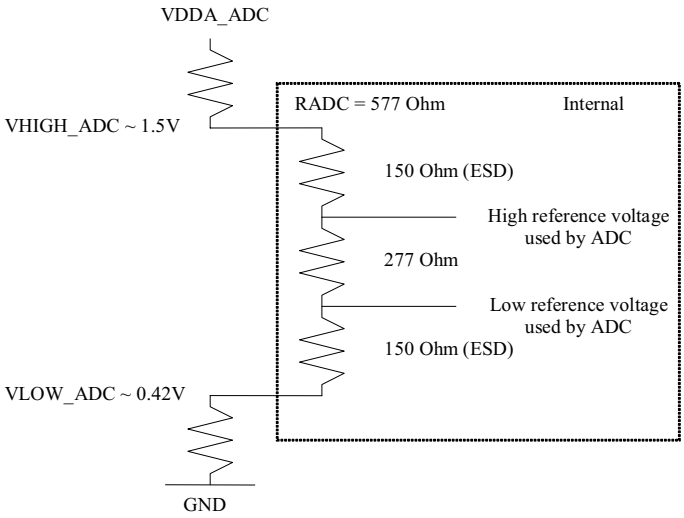
The IBIS4-6600 has a two 10 bit flash analog digital converters. The ADC's are electrically separated from the image sensor. The inputs of the ADC should be tied externally to the outputs of the output amplifiers. One ADC will sample the even columns and the other one will sample the odd columns. Alternatively, one ADC can sample all the pixels as well.

Table 10. ADC specifications

Parameter	Specification
Input range	Set by external resistors (see next section)
Quantization	10 Bits
Nominal data rate	20Msamples/s
DNL(Linear conversion mode)	Typ. < 0.4LSB RMS
INL (linear conversion mode)	Typ. < 3.5 LSB
Input capacitance	< 2 pF
Conversion law	Linear/Gamma-corrected

Setting of the ADC reference voltages

Figure 10. ADC resistor ladder



The internal resistance has a value of approximately 577 Ω. Only 277 Ω of this internal resistance is actually used as reference for the internal ADC. This causes the actual ADC voltage range to be half of the voltage difference between VHIGH_ADC and VLOW_ADC. This results in the following values for the external resistors:

Table 11. ADC resistor values

Resistor	Value (Ω)
RVHIGH_ADC	560
RInternal	577
RVLOWADC	220

Subsample Modes

To increase the frame rate for lower resolution and/or regions of interest, a number of sub sampling modes have been implemented. The possible sub sample modes are listed in Table 12. . The bits can be programmed in the IMAGE_CORE register (see 2.9.2.8). To preserve the color information, 2 adjacent pixels are read in any mode, while the number of pixels that is not read, varies from mode to mode. This will be designed as a repeated block of 24 pixels wide, which is the lowest common multiple of the modes described above. Including the dummy pixels and the two additional rows/columns, the number of starting coordinates for the x and y shift register is thus 99 in the X and 138 in the Y direction. The total number of pixels, excluding dummy pixels, is a multiple of 24, and two additional pixels to have the same window edges independently of the sub-sampling mode. In the X direction, two columns are always addressed at the same moment since the signals from the odd and even columns must be put simultaneously on the corresponding bus. In the Y direction, the rows are addressed one by one. This results in slightly different implementations of the sub-sampling modes for the two directions (Figure 11. and Figure 12.).

Table 12. Subsample Patterns

Mode	Bits	Read	Step	
A	000	2	2	Default mode
B	001	2	4	(Skip 2)
C	010	2	6	(Skip 4)
D	011	2	8	(Skip 6)
E	1xx	2	12	(Skip 10)

Figure 11. X-subsampling

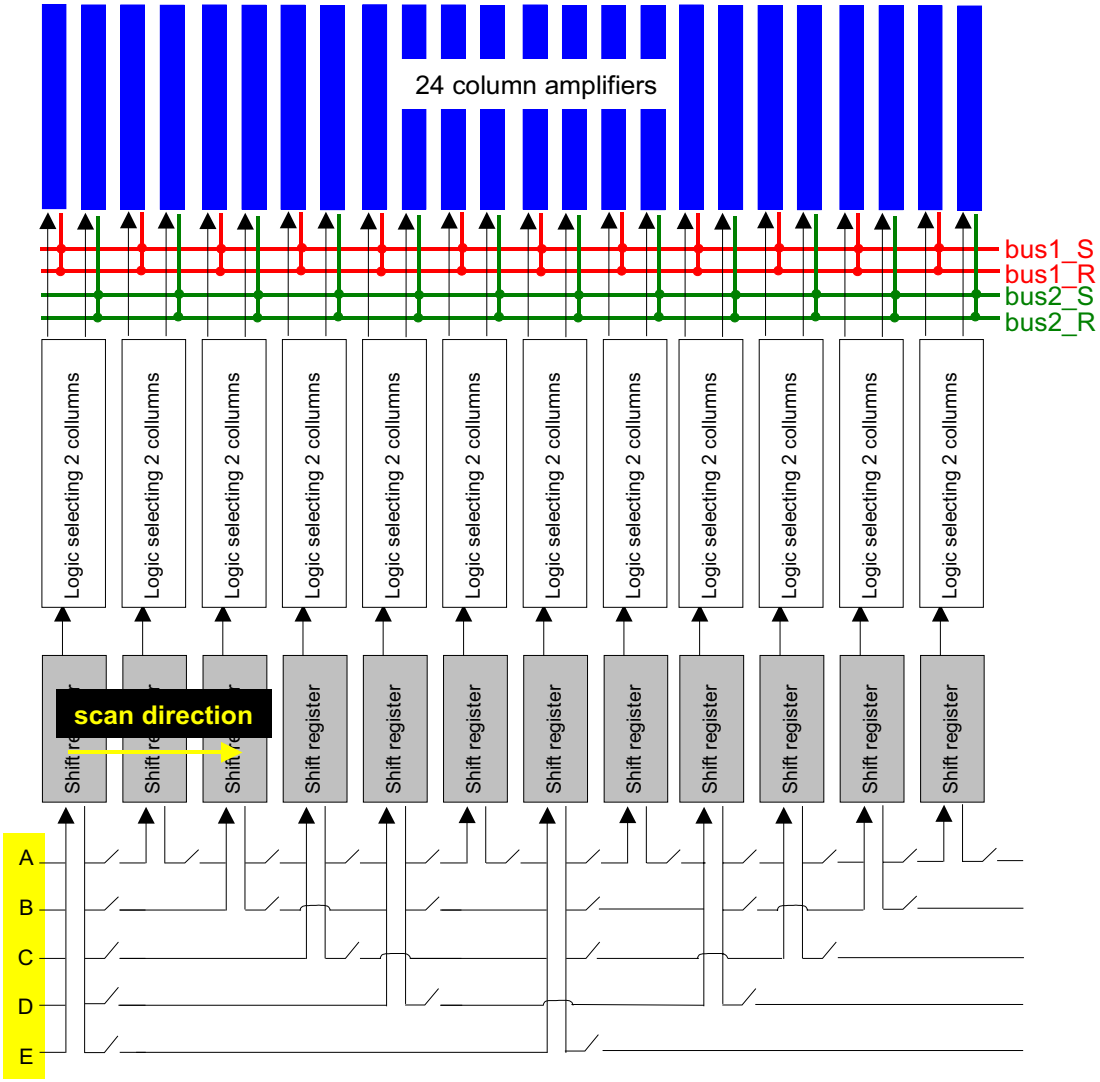


Figure 12. Y-subsampling

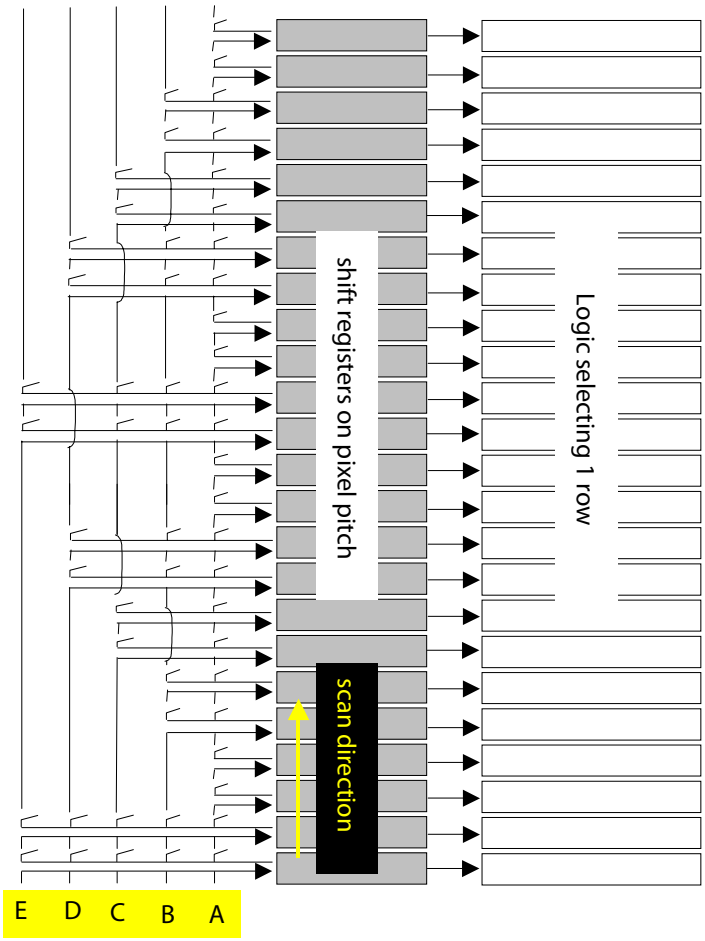
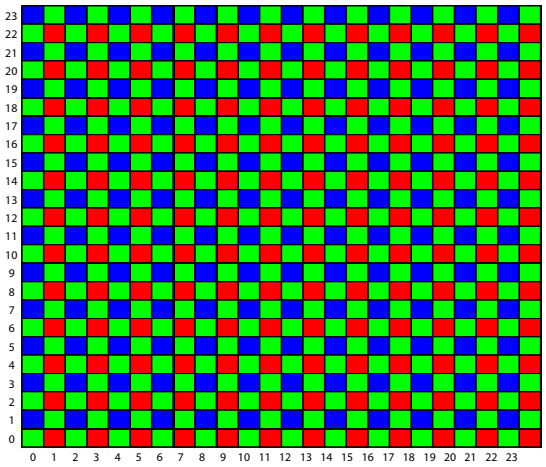


Table 13. Frame Rate vs. Subsample Mode

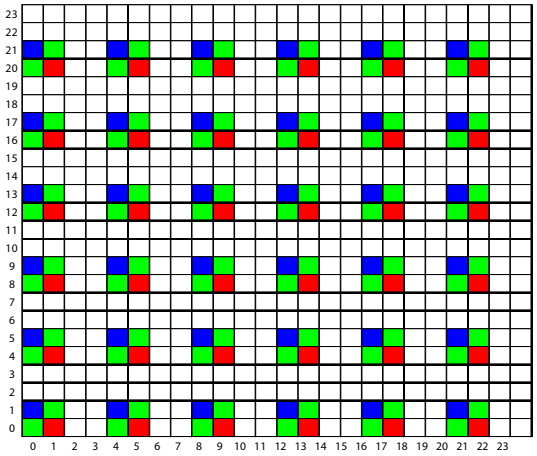
Mode	Ratio	Resolution (Y*X)	Frame time [ms]	Frame time [ms]
A	1:1	3002 x 2210	187.4	5.3
B	1:4	1502 x 1106	52.3	19.1
C	1:9	1002 x 738	25.7	38.9
D	1:16	752 x 554	15.8	63.2
63.2	1:36	502 x 370	8.2	121.2
VGA (p)		640 x 480	12.3	81.5
VGA (p) + 23		663 x 503	13.1	76.4
VGA (l)		480 x 640	11.1	89.9
VGA(l) + 23		503 x 663	11.9	83.7

Figure 13. shows the pixels read out in each color sub-sampling mode.

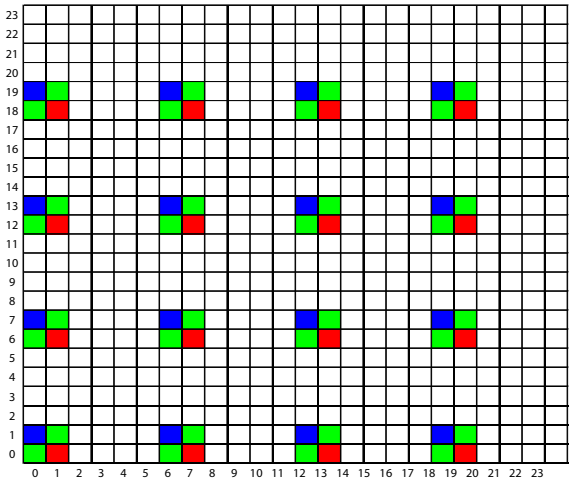
Figure 13. Pixel Readout in Various Subsample Modes



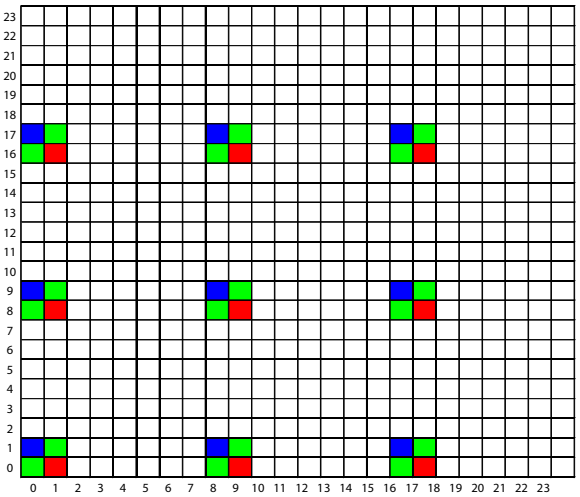
Mode A



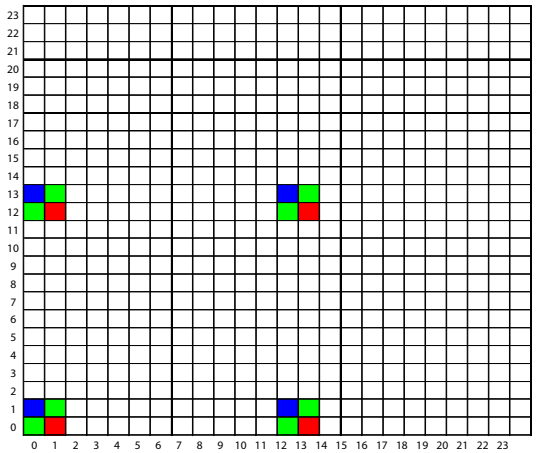
Mode B



Mode C



Mode D



Mode E

Electronic Shutter

A curtain-like (rolling) electronic shutter has been implemented on-chip. As can be seen in Figure 14., there are two Y shift registers. One of them points to the row that is currently being read out. The other shift register points to the row that is currently being reset. Both pointers are shifted by the same Y-clock and move over the focal plane. The integration time is set by the delay between both pointers.

In case of a mechanical shutter, the two shift registers can be combined to apply the pulses from both sides of the pixel array simultaneously. This is to halve the influence of the parasitic RC times of the reset and select lines in the pixel array (which can result in a reduction of the row blanking time). This is the case when FAST_RESET in the SEQUENCER register is set to 1 or in the non-destructive readout modes 1 and 2.

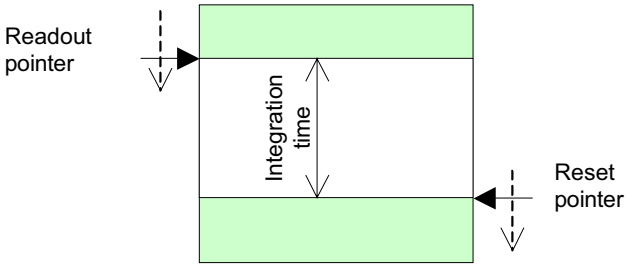
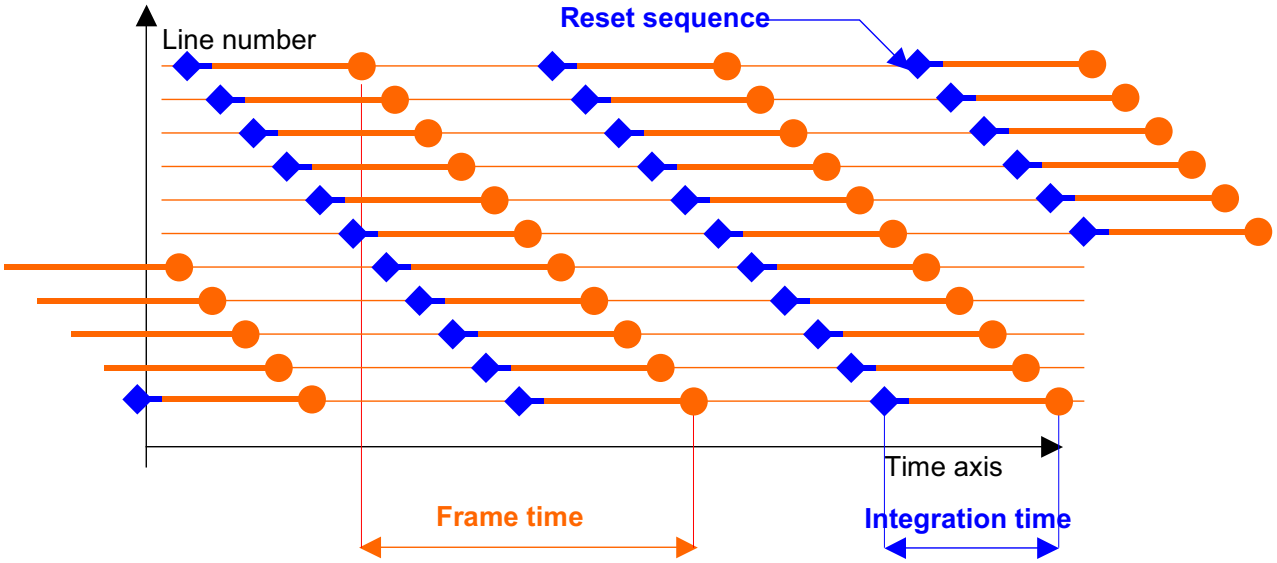


Figure 14. Electronic Rolling Shutter Operation



High Dynamic Range Modes

Double Slope Integration

The IBIS4-6600 has a feature to increase the optical dynamic range of the sensor; called double slope integration. The pixel response can be extended over a larger range of light intensities by using a "dual slope integration" (patents pending). This is obtained by the addition of charge packets from a long and a short integration time in the pixel during the same exposure time. Figure 15. shows the response curve of a pixel in dual slope integration mode. The curve also shows the response of the same pixel in linear integration mode, with a long and short integration time, at the same light levels.

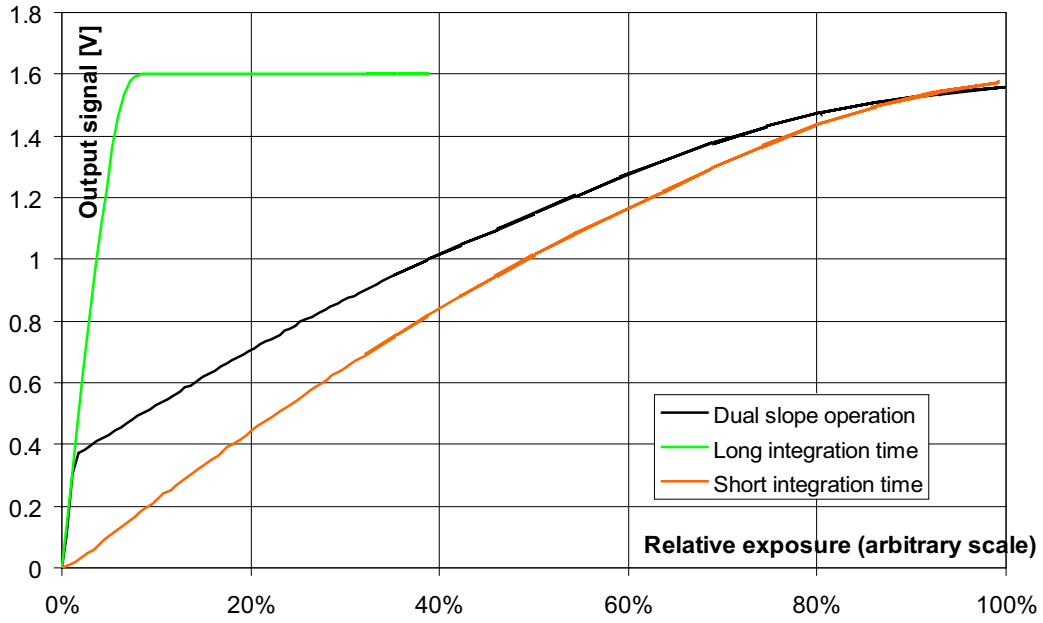
Dual slope integration is obtained by:

Feeding a lower supply voltage to VDD_RESET_DS (e.g., apply 2.0V to 2.5V). Note that for normal (single slope operation VDD_RESET_DS should have the same value as VDD_RESET. The difference between VDD_RESET_DS and VDD_RESET determines the range of the high sensitivity, thus the output signal level at which the transition between high and low sensitivity occurs.

Put the amplifier gain to the lowest value where the analog output swing covers the ADC's digital input swing. Increasing the amplification too much will likely boost the high sensitivity part over the whole ADC range.

The electronic shutter determines the ratio of integration times of the two slopes. The high sensitivity ramp corresponds to "no electronic shutter", thus maximal integration time (frame read out time). The low sensitivity ramp corresponds to the electronic shutter value that would have been obtained in normal operation.

Figure 15. Double Slope Response



Non-destructive Read Out (NDR)

The default mode of operation of the sensor is with FPN correction (double sampling). However, the sensor can also be read out in a non-destructive way. After a pixel is initially reset, it can be read multiple times, without resetting. The initial reset level and all intermediate signals can be recorded. High light levels will saturate the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, one has to use the later or latest samples. Essentially an active pixel array is read multiple times, and reset only once. The external system intelligence takes care of the interpretation of the data. Table 14. summarizes the advantages and disadvantages of non-destructive readout.

Figure 16. Principle of Non-destructive Readout

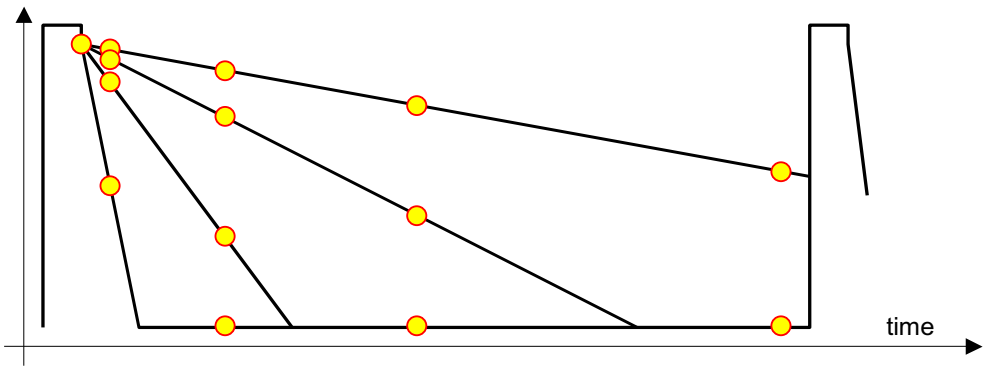


Table 14. Pros and Cons of NDR

Advantages	Disadvantages
Low noise - as it is true CDS. In the order of 10 e- or below.	System memory required to record the reset level and the intermediate samples.
High sensitivity - as the conversion capacitance is kept rather low.	Requires multiples readings of each pixel, thus higher data throughput.
High dynamic range - as the results includes signal for short and long integrations times.	Requires system level digital calculations.

Sequencer and Registers

Figure 3. showed a number of control signals that are needed to operate the sensor in a particular sub-sampling mode, with a certain integration time, output amplifier gain, etc. Most of these signals are generated on-chip by the sequencer that uses only a few control signals. These control signals should be generated by the external system:

SYS_CLOCK, which defines the pixel rate (nominal 40 MHz),

Y_START pulse, which indicates the start of a new frame,

Y_CLOCK, which selects a new row and will start the row blanking sequence, including the synchronization and loading of the X-register.

The relative position of the pulses will be determined by a number of data bits that are uploaded in internal registers through a Serial to Parallel interface (SPI).

Internal Registers

Table 15. shows a list of the internal registers with a short description. In the next section, the registers are explained in more detail.

Table 15. List of Internal Registers

Register	Bit	Name	Description
0 (0000)	11:0	SEQUENCER register	Selection of mode, granularity of the X sequencer clock, calibration, Default value <11:0>:"000100000000"
	0	NDR	Mode of readout: NDR = 0: normal readout (double sampling) NDR = 1: non-destructive readout
	1:2	NDR_mode	4 different modes of non-destructive readout (no influence if NDR = 0)
	3	RESET_BLACK	0 = normal operation 1 = reset of pixels before readout
	4	FAST_RESET	0 = electronic shutter operation 1 = addressing from both sides
	5	FRAME_CAL_MODE	0 = fast 1 = slow
	6	LINE_CAL_MODE	0 = fast 1 = slow
	7	CONT_CHARGE	0 = normal mode 1 = 'continuous precharge'
	8	GRAN_X_SEQ_LSB	Granularity of the X sequencer clock
	9	GRAN_X_SEQ_MSB	
	10	BLACK	0 = normal mode 1 = disconnects column amplifiers from busses, output of amplifier equals dark reference level
	11	RESET_ALL	0 = normal mode 1 = continuous reset of all pixels
1 (0001)	10:0	NROF_PIXELS	Number of pixels to count (X direction). Max. 2222/2 (2210 real + 12 dummy pixels). Default value <10:0>:"01000000000"
2 (0010)	11:0	NROF_LINES	Number of lines to count (Y direction). Max. 3014 (3002 real + 12 dummy pixels). Default value <11:0>:"101111000110"
3 (0011)	11:0	INT_TIME	Integration time. Default value <11:0>:"000000000001"
4 (0100)	7:0	DELAY	Delay of sequencer pulses Default value <7:0>:"00000011"
	0:3	DELAY_PIX_VALID	Delay of PIX_VALID pulse
	4:7	DELAY_EOL/EOF	Delay of EOL/EOF pulses
5 (0101)	6:0	X_REG	X start position (0 to 98). Default value <6:0>:"0000000"
6 (0110)	7:0	Y_REG	Y start position (0 to 137). Default value <7:0>:"00000000"

Table 15. List of Internal Registers (continued)

Register	Bit	Name	Description
7 (0111)	7:0	IMAGE CORE register	Default value <7:0>:"00000000"
	1:0	TEST_mode	LSB: odd, MSB: even 0 = normal operation
	4:2	X_SUBSAMPLE	sub-sampling mode in X-direction
	7:5	Y_SUBSAMPLE	sub-sampling mode in X-direction
8 (1000)	9:0	AMPLIFIER register	Default value <9:0>:"0000010000"
	3:0	GAIN<3:0>	Output amplifier gain setting
	4	UNITY	0 = gain setting by GAIN<3:0> 1 = unity gain setting
	5	ONE_OUT	0 = two analog outputs 1 = multiplexing to one output (out_1)
	6	STANDBY	0 = normal operation 1 = amplifier in standby mode.
	7:9	DELAY_CLK_AMP	Delay of pixel clock to output amplifier.
9 (1001)	7:0	DAC_RAW_REG	Amplifier DAC raw offset. Default value <7:0>:"10000000"
10 (1010)	7:0	DAC_FINE_REG	Amplifier DAC fine offset. Default value <7:0>:"10000000"
11 (1011)	7:0	DAC_DARK_REG	DAC dark reference on output bus. Default value <7:0>:"10000000"
12 (1100)	10:0	ADC register	Default value <10:0>:"00000000000"
	0	STANDBY_1	0 = normal operation 1 = ADC in standby
	1	STANDBY_2	
	2	ONE	0 = multiplexing of two ADC outputs 1 = disable multiplexing
	3	SWITCH	if ONE = 0: delay of output with one (EXT_CLK = 0) or half (EXT_CLK = 1) clock cycle if ONE = 1: switch between two ADCs
	4	EXT_CLK	0 = internal clock (same as clock to X shift register and output amplifier) 1 = external clock
	5	TRISTATE	0 = normal operation 1 = outputs in tristate mode
	6:8	DELAY_CLK_ADC	Delay of clock to ADCs and digital multiplexer
	9	GAMMA	0 = linear conversion 1 = 'gamma' law conversion
	10	BITINVERT	0 = no inversion of bits 1 = inversion of bits
13 (1101)		Reserved.	
14 (1110)		Reserved.	
15 (1111)		Reserved.	

Detailed Description of Registers

SEQUENCEHR Register

a. NDR (bit 0)

In normal operation (NDR = 0), the sensor operates in double sampling mode. At the start of each row readout, the signals from the pixels are sampled, the row is reset and the signals from the pixels are sampled again. The values are subtracted in the output amplifier.

When NDR is set to 1, the sensor operates in non-destructive readout (NDR) mode (see Table 16.).

b. NDR_mode (bit 1 and 2)

These bits only influence the operation of the sensor in case NDR (bit 0) is set to 1. There are basically two modes for non-destructive readout (mode 1 and 2). Each mode needs two different frame readouts (setting 1 and 2 for mode 1, setting 3 and 4 for mode 2). First a reset/readout sequence (called reset_seq hereafter) and then one or several pure readout sequences (called read_seq hereafter). Table 16. gives an overview of the different NDR modes.

Table 16. Overview of NDR Modes.

Setting	Bits	NDR mode	Sequence
1	00	1	reset
2	01	1	read
3	10	2	reset
4	11	2	read

Mode 1

In this mode, the sensor is readout in the same way as for non-destructive readout. However, electronic shutter control is not possible in this case, i.e., the minimal (integration) time between two readings is equal to the number of lines that has to be read out (frame read time). The row lines are clocked simultaneously (left and right clock pulses are equal).

Mode 2

In mode 2, it is possible to have a shorter integration time than the frame read time. Rows are alternating read out with the left and right pointer. These two pointers can point to two different rows (see INT_TIME register). The (integration) time between two readings of the same row is equal to the number of lines that is set in the INT_TIME register times 2 plus 1 and is minimal 1 line read time. In setting 3, the row that is read out by the left pointer is reset and read out (first Y_CLOCK), the row that is read out by the right pointer is read out without resetting (second Y_CLOCK). In setting 4, both rows are read out without resetting (on the first Y_CLOCK the row is read out by the left pointer; on the second Y_CLOCK the row is read out by the right pointer).

For both modes, the signals are read out through the same path as with destructive readout (double sampling) but the busses that are carrying the reset signals in destructive readout, are in non-destructive readout set to the voltage given by DAC_DARK.

c. Reset_black (bit 3)

If RESET_BLACK is set to 1, each line is reset before it is read out (except for the row that is read out by the right pointer in NDR mode 2). This might be useful to obtain black pixels.

d. Fast_reset (bit 4)

The fast reset option (FAST_RESET = 1) might be useful in case a mechanical camera shutter is used. The fast reset is done on a row-by-row basis, not by a global reset. A global reset means charging all the pixels at the same time, which may result in a huge peak current. Therefore, the rows can be scanned rapidly while the left and right shift registers are both controlled identically, so that the reset lines over the pixel array are driven from both sides. This reduces the reset (row blanking) time (when FAST_RESET = 1 the smallest X-granularity can be used). After the row blanking time the row is reset and Y_CLOCK can be asserted to reset the next row.

After a certain integration time, the read out can be done in a similar way. The Y shift registers are again synchronized to the first row. Both shift registers are driven identically, and all rows & columns are scanned for (destructive) readout. FAST_RESET = 1 puts the sequencer in such mode that the left and right shift registers are both controlled identically.

e. Output amplifier calibration (bit 5 and 6)

Bits FRAME_CAL_MODE and LINE_CAL_MODE define the calibration mode of the output amplifier.

During every row-blanking period, a calibration is done of the output amplifier. There are 2 calibration modes. The FAST mode (= 0) can force a calibration in one cycle but is not so accurate and suffers from kTC noise, while the SLOW mode (= 1) can only make incremental adjustments and is noise free. Approximately 200 or more "slow" calibrations will have the same effect as 1 "fast" calibration.

Different calibration modes can be set at the beginning of the frame (FRAME_CAL_MODE bit) and for every subsequent row that is read (LINE_CAL_MODE bit).

f. Continuous charge (bit 7)

For some applications it might be necessary to use continuous charging of the pixel columns instead of a precharge on every row sample operation.

Setting bit CONT_CHARGE to 1 will activate this function. The resistor connected to pin CMD_COL is used to control the current level on every pixel column.

g. Internal clock granularities

The system clock is divided several times on-chip.

The X-shift-register that controls the column/pixel readout, is clocked by half the system clock rate. Odd and even pixel columns are switched to 2 separate busses. In the output amplifier the pixel signals on the 2 busses can be combined to one pixel stream at 40 MHz.

The clock that drives the X-sequencer can be a multiple of 2, 4, 8 or 16 times the system clock. Table 17. gives the settings for the granularity of the X-sequencer clock and the corresponding row blanking time (for NDR = 0). A row blanking time of 7.18 µs is the baseline for almost all applications

.

Table 17. Granularity of X-Sequencer Clock and Corresponding Row Blanking Time (for NDR = 0).

Gran_x_seq_msb/lsb	X-sequencer clock	Row blanking time	Row blanking time [µs]
00	2 x sys_clock	142 x TSYS_CLOCK	3.55
01	4 x sys_clock	282 x TSYS_CLOCK	7.05
10	8 x sys_clock	562 x TSYS_CLOCK	14.05
11	16 x sys_clock	1122 x TSYS_CLOCK	1122 x TSYS_CLOCK

h. Black (bit 10)

In case BLACK is set to 1, the internal black signal will be held high continuously. As a consequence, the column amplifiers are disconnected from the busses, the busses are set to the voltage given by DAC_DARK and the output of the amplifier equals the voltages from the offset DACs.

i. Reset_all (bit 11)

In case RESET_ALL is set to 1, all the pixels are simultaneously put in a 'reset' state. In this state, the pixels behave logarithmically with light intensity. If this state is combined with one of the NDR modes, the sensor can be used in a non-integrating, logarithmic mode with high dynamic range.

j. Nrof_pixels Register

After the internal X_SYNC is generated (start of the pixel readout of a particular row), the PIXEL_VALID signal goes high. The PIXEL_VALID signal goes low when the pixel counter reaches the value loaded in the NROF_PIXEL register and an EOL pulse is generated. Due to the fact that 2 pixels are addressed at each internal clock cycle the amount of pixels read out in one row = 2*(NROF_PIXEL + 1).

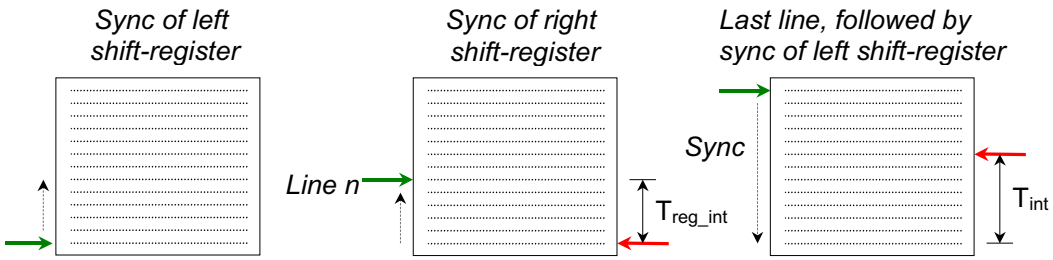
k. Nrof_lines Register

After the internal YL_SYNC is generated (start of the frame readout with Y_START), the line counter increases with each Y_CLOCK pulse until it reaches the value loaded in the NROF_LINES register and an EOF pulse is generated. In NDR mode 2, the line counter increments only every two Y_CLOCK pulses and the EOF pulse shows up only after the readout of the row indicated by the right shift register

INT_TIME Register

When the Y_START pulse is applied (start of the frame readout), the sequencer will generate the YL_SYNC pulse for the left Y-shift register. This loads the left Y-shift register with the pointer loaded in Y_REG register. At each Y_CLOCK pulse, the pointer shifts to the next row and the integration time counter increases (increment only every two Y_CLOCK pulses in NDR mode 2) until it reaches the value loaded in the INT_TIME register. At that moment, the YR_SYNC pulse for the right Y-shift register is generated which loads the right Y-shift register with the pointer loaded in Y_REG register (Figure 17.).

Figure 17. Syncing of the Y-shift Registers.



Treg_int: ..... Difference between left and right pointer

. = integration counter until value "n" of INT_TIME register is reached

.....= INT_TIME register.

In case of NDR = 0, the actual integration time Tint is given by

TintL: .....Integration time [# lines]

.....= NROF_LINES register - INT_TIME register + 1

In case of NDR = 1, NDR mode 1, the time Tint between two readings of the same row is given by

Tint: .....Integration time [# lines]

.....= NROF_LINES register + 1

In case of NDR = 1, NDR mode 2, the times Tint1 and Tint2 between two readings of the same row (alternatingly) are given by

Tint1:..... Integration time [# lines]

.....= 2 * INT_TIME register + 1

Tint2:..... Integration time [# lines]

= 2 * (NROF_LINES register + 1) - (2 * INT_TIME register + 1)

DELAY register

The DELAY register can be used to delay the PIXEL_VALID pulse (bits 0:3) and the EOL/EOF pulses (bits 4:7) to

synchronize them to the real pixel values at the analog output or the ADC output (which give additional delays depending on their settings). The bit settings and corresponding delay is indicated in Table 18. .

Table 18. Delay added by Changing the Settings of the DELAY Register

bits	Delay [# SYS_CLOCK periods]	bits	Delay [# SYS_CLOCK periods]
0000	0	1000	6
0001	0	1001	7
0010	0	1010	8
0011	1	1011	9
0100	2	1100	10
0101	3	1101	11
0110	4	1110	12
0111	5	1111	13

X_REG Register

The X_REG register determines the start position of the window in the X-direction. In this direction, there are 2208 + 2 + 12 readable pixels. In the active pixel array sub-sampling blocks are 24 pixels wide and the columns are read two by two and therefore, the number of start positions equals 2208/24 +2/2 +12/2 = 92 + 1 + 6 = 99.

Y_REG Register

The Y_REG register determines the start position of the window in the Y-direction. In this direction, there are 3000 + 2 + 12 readable pixels. In the active pixel array sub-sampling blocks are 24 pixels wide and the rows are read one by one and therefore, the number of start positions equals 3000/24 + 2/2 +12 = 125 + 1 + 12 = 138.

Image_core Register

Bits 0:1 of the IMAGE_CORE register defines the several test modes of the image core. Setting 00 is the default and normal operation mode. In case the bit is set to 1, the odd (bit 0) or even (bit 1) columns are tight to VDD. These test modes can be used to tune the sampling point of the ADCs to an optimal position.

Bits 2:7 of the IMAGE_CORE register define the sub-sampling mode in the X-direction (bits 2:4) and in the Y-direction (bits 5:7). The sub-sampling modes and corresponding bit setting are given in Analog to Digital Converter on page 13

AMPLIFIER Register

a. Gain (bits 0:3)

The gain bits determine the gain setting of the output amplifier. They are only effective if UNITY = 0. The gains and corresponding bit setting are given in Table 9. Stage 2: Programmable Gain Amplifier on page 12.

b. Unity (bit 4)

In case UNITY = 1, the gain setting of GAIN is bypassed and the gain amplifier is put in unity feedback.

c. One_out

If ONE_OUT = 0, the two output amplifiers are active. If ONE_OUT = 1, the signals from the two busses are multiplexed to output OUT1. The gain amplifier and output driver of the second path are put in standby.

d. Standby

If STANDBY = 1, the complete output amplifier is put in standby (this reduces the power consumption significantly)

e. Delay_clk_amp

The clock that acts on the output amplifier can be delayed to compensate for any delay that is introduced in the path from shift register, column selection logic, column amplifier and busses to the output amplifier. Setting '000' is used as a baseline.

Table 19. Delay added by Changing the Settings of the DELAY_CLK_AMP Bits

Bits	Delay [ns]	Bits	Delay [ns]
000	1.7	100	Inversion + 8.3
001	2.9	2.9	Inversion + 9.7
010	4.3	110	Inversion + 11.1
011	6.1	111	Inversion + 12.3

Dac_raw_reg and Dac_fine_reg Register

These registers determine the black reference level at the output of the output amplifier. Bit setting 11111111 for DAC_RAW_REG register gives the highest offset voltage; bit setting 00000000 for DAC_RAW_REG register gives the lowest offset voltage. Ideally, if the two output paths have no offset mismatch, the DAC_FINE_REG register must be set to 10000000. Deviation from this value can be used to compensate the internal mismatch (see Offset DACs on page 13).

Dac_raw_dark Register

This register determines the voltage level that is put on the internal busses during calibration of the output stage. This voltage level is also continuously put on the reset busses in case of non-destructive readout (as a reset level for the double sampling FPN correction).

ADC Register

a. Standby_1 and standby_2

In case only one or none of the ADCs is used, the other or both ADCs can be put in standby by setting the bit to 1 (this reduces the power consumption significantly).

b. One

In case OUT1 and OUT2 are both used and connected to ADC_IN1 and ADC_IN2 respectively, ONE must be 0 to use both ADCs and to multiplex their output to ADC_D<9:0>. If ONE = 1, the multiplexing is disabled.

c. Switch

In case the two ADCs are used (ONE = 0) and internal pixel clock (EXT_CLK = 0), the ADC output is delayed with one system clock cycle if SWITCH = 1. In case the two ADCs are used (ONE = 0) and an external ADC clock (EXT_CLK = 1) is applied, the ADC output is delayed with half ADC clock cycle if SWITCH = 1.

In case only one ADC is used, the digital multiplexing is disabled by ONE = 1, but SWITCH selects which ADC output is on ADC_D<9:0> (SWITCH = 0: ADC_1, SWITCH = 1: ADC_2).

d. Ext_clk

In case EXT_CLK = 0, the internal pixel clock (that drives the X-shift registers and output amplifier, i.e. half the system clock) is used as input for the ADC clock. In case EXT_CLK = 1, an external clock must be applied to pin ADC_CLK_EXT (pin 46).

e. Tristate

In case TRISTATE = 1, the ADC_D<9:0> outputs are in tri-state mode.

f. Delay_clk_adc

The clock that finally acts on the ADCs can be delayed to compensate for any delay that is introduced in the path from the analog outputs to the input stage of the ADCs. The same settings apply as for the delay that can be given to the clock acting on the output amplifier (see Table 19.). The best setting will also depend on the delay of the output amplifier clock and the load of the output amplifier. It must be used to optimize the sampling moment of the ADCs with respect to the analog pixel input signals. Setting '000' is used as a baseline.

g. Gamma

If GAMMA is set to 0, the ADC input to output conversion is linear, otherwise the conversion follows a 'gamma' law (more contrast in dark parts of the window, lower contrast in the bright parts).

h. Bitinvert

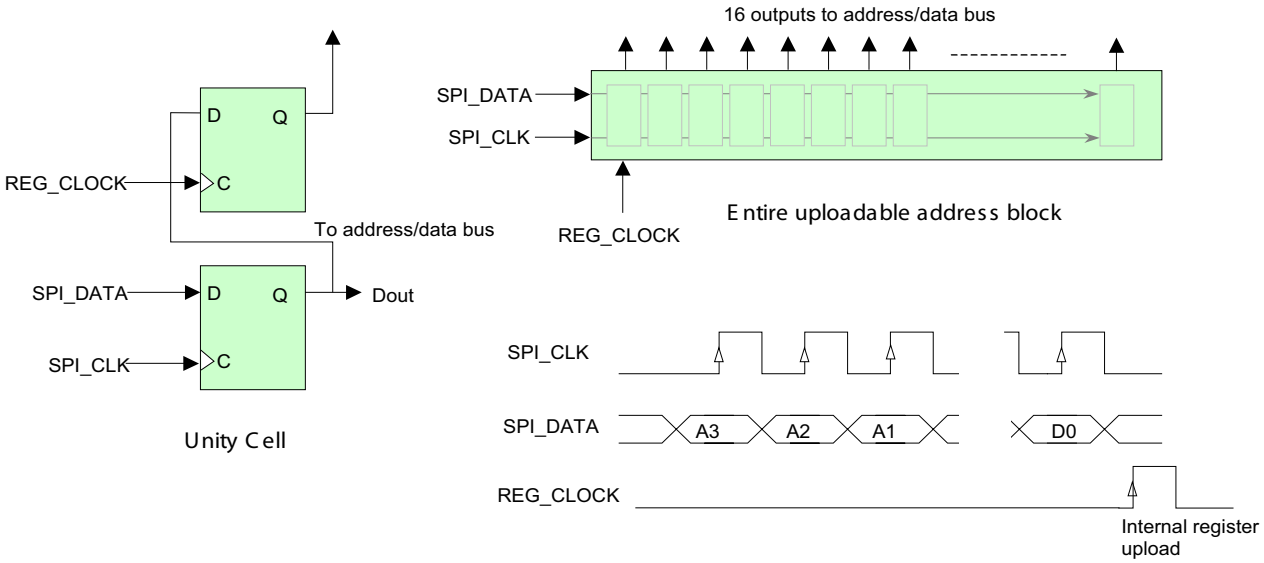
If BITINVERT = 0, 0000000000 is the conversion of the lowest possible input voltage, otherwise the bits are inverted.

Serial to Parallel Interface

To upload the sequencer registers a dedicated serial to parallel interface (SPI) is implemented. 16 bits (4 address bits + 12 data bits) must be uploaded serially. The address must be uploaded first (MSB first), then the data (also MSB first).

The elementary unit cell is shown in Figure 18. 16 of these cells connected in series, having a common SPI_CLK form the entire uploadable parameter block, where Dout of one cell is connected to SPI_DATA of the next cell (max. speed 20 MHz). The uploaded settings on the address/data bus are loaded into the correct register of the sensor on the rising edge of signal REG_CLOCK and become effective immediately.

Figure 18. SPI Interface



Timing Diagrams

Sequencer Control Signals

There are 3 control signals that operate the image sensor:

Sys_clock

Y_clock

Y_start

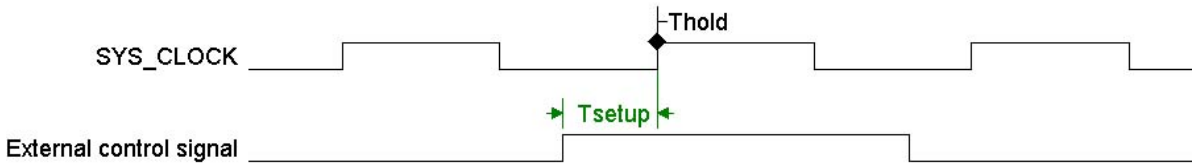
These control signals should be generated by the external system with following time constraints to SYS_CLOCK (rising edge = active edge):

TSETUP >7.5 ns.

THOLD > 7.5 ns.

It is important that these signals are free of any glitches.

Figure 19. Relative Timing of the 3 Control Signals



Basic Frame and Line Timing

The basic frame and line timing of the IBIS4-6600 sensor is shown in Figure 20.

The pulse width of Y_CLOCK should be minimum 1 clock cycle and 3 clock cycles for Y_START. As long as Y_CLOCK is applied, the sequencer stays in a suspended state.

T1 Row blanking time: During this period, the X-sequencer generates the control signals to sample the pixel signal and pixel reset levels, and start the readout of one line. It depends on the granularity of the X-sequencer clock (see Table 17.).

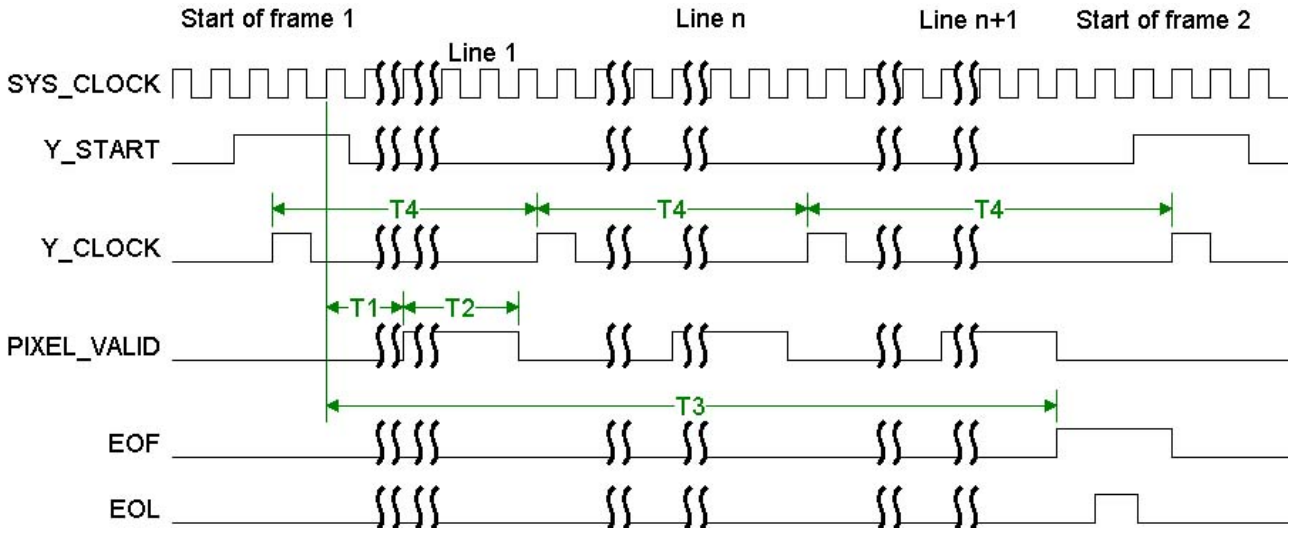
T2 Pixels counted by pixel counter until the value of Nrof_pixels register is reached. Pixel_valid goes high when the internal X_sync signal is generated, in other words when the readout of the pixels is started. Pixel_valid goes low when the pixel counter reaches the value loaded in the Nrof_pixels register. Eol goes high Sys_clock cycle after the falling edge of Pixel_valid.

T3 EOF goes high when the line counter reaches the value loaded in the NROF_LINES register and the line is read (PIXEL_VALID goes low).

T4 The time delay between successive Y_CLOCK pulses needs to be equal to avoid any horizontal illumination (integration) discrepancies in the image.

Both EOF and EOL can be tied to Y_START (EOF) and Y_CLOCK (EOL) if both signals are delayed with at least 2 SYS_CLOCK periods to let the sensor run in a fully automatic way.

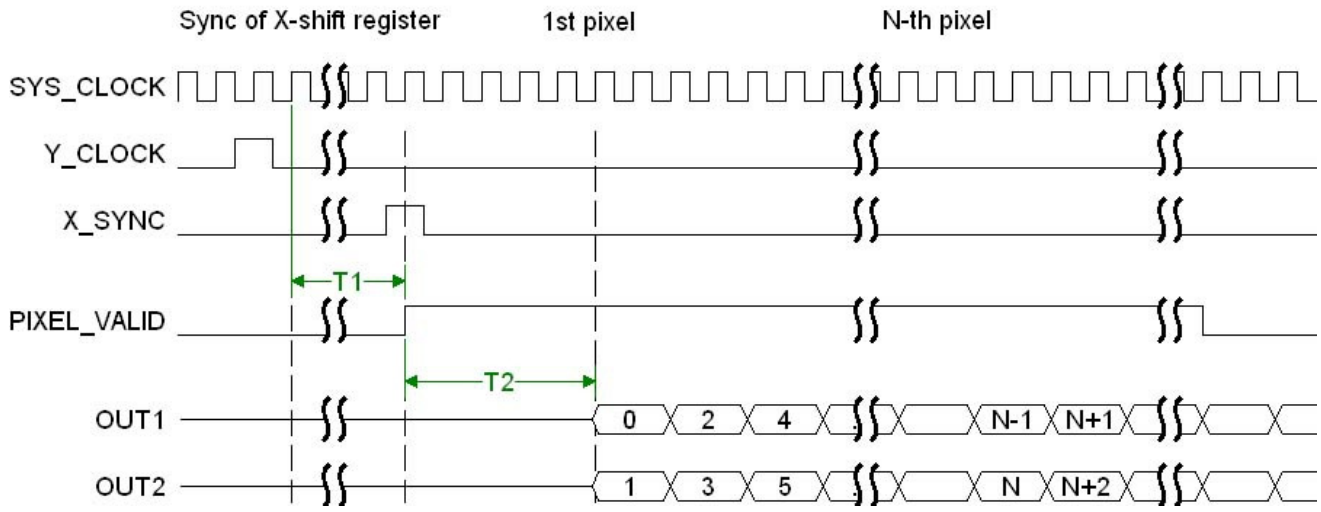
Figure 20. Basic Frame and Line Timing



Pixel Output Timing

Using Two Analog Outputs

Figure 21. Pixel Output Timing using Two Analog Outputs



The pixel signal at the OUT1 (OUT2) output becomes valid after 4 SYS_CLOCK cycles when the internal X_SYNC (= start of PIXEL_VALID output) has appeared (see Figure 21.). The PIXEL_VALID and EOL/EOF pulses can be delayed by the user through the DELAY register.

T1 ..... Row blanking time (see Table 17.)

T2 ..... 4 SYS_CLOCK cycles.

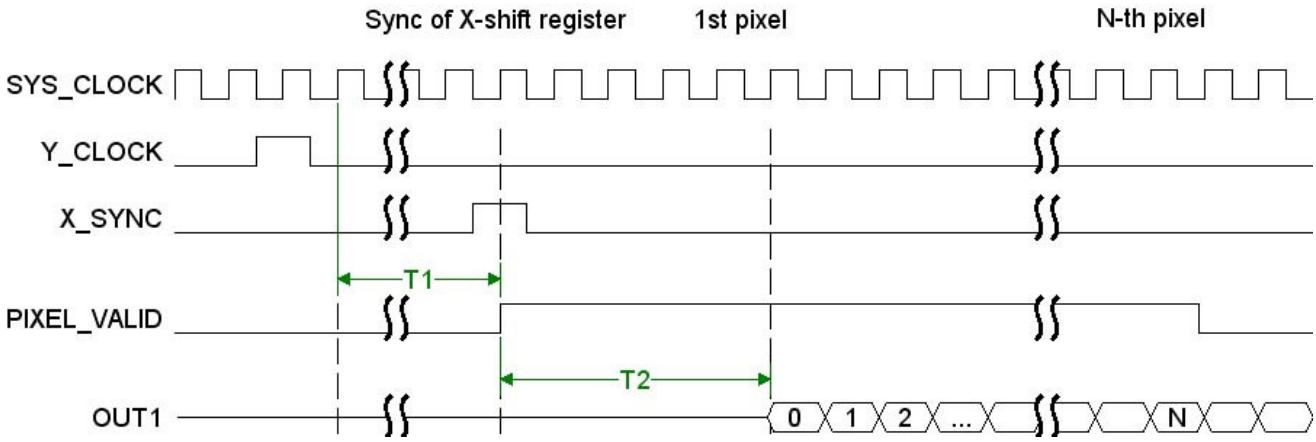
Multiplexing to One Analog Output

The pixel signal at the OUT1 output becomes valid after 5 SYS_CLOCK cycles when the internal X_SYNC (= start of PIXEL_VALID output) has appeared (see Figure 22.). The PIXEL_VALID and EOL/EOF pulses can be delayed by the user through the DELAY register.

T1 ..... Row blanking time

T2 ..... 5 SYS_CLOCK cycles.

Figure 22. Pixel Output Timing Multiplexing to One Analog Output



ADC Timing

Two Analog Outputs

Figure 23. ADC Timing using Two Analog Outputs

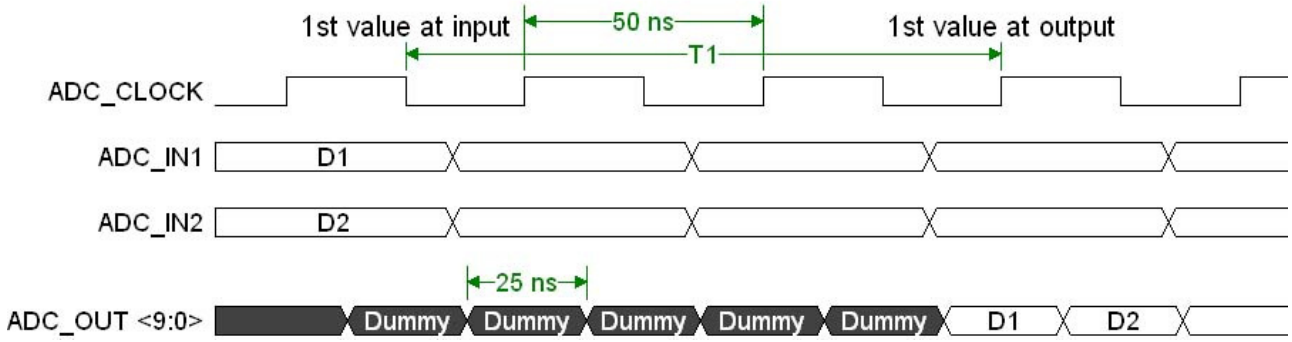


Figure 23. shows the timing of the ADC using two analog outputs. Internally, the ADCs sample on the falling edge of the ADC_CLOCK (in case of internal clock, the clock is half the SYS_CLOCK).

T1: Each ADC has a pipeline delay of 2 ADC_CLOCK cycles. This results in a total pipeline delay of 4 pixels.

One Analog Output

Figure 24. ADC Timing using One Analog Output

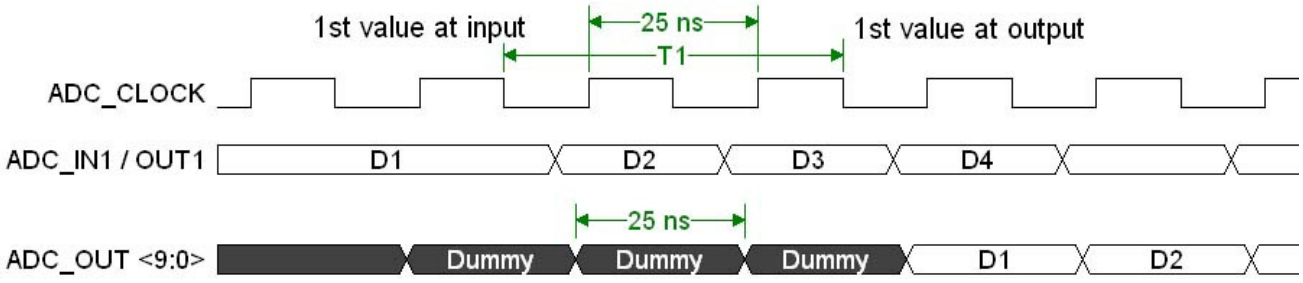


Figure 24. shows the timing of the ADC using one analog output. Internally, the ADC samples on the falling edge of the ADC_CLOCK.

T1: The ADC has a pipeline delay of 2 ADC_CLOCK cycles.

Pin List

Table 20. is a list of all the pins and their function. In total, there are 68 pins. All pins with the same name can be connected together.

Table 20. Pin List

Pin	Pin Name	Pin Type	Expected Voltage [V]	Pin Description
1	CMD_COL_CTU	Input	0	Biasing of columns (ctu). Decouple with 100 nF to GNDA.
2	CMD_COL	Input	1.08	Biasing of columns. Connect to VDDA with R = 10 k and decouple to GNDA with C = 100 nF.
3	CMD_COLAMP	Input	0.66	Biasing of column amplifiers. Connect to VDDA with R = 100 k and decouple to GNDA with C = 100 nF.
4	CMD_COLAMP_CTU	Input	0.37	Biasing of column amplifiers. Connect to VDDA with R = 10 M and decouple to GNDA with C = 100 nF.
5	RCAL_DAC_DARK	Input	1.27 @ code 128 DAC_DARK reg	Biasing of DAC for dark reference. Can be used to set output range of DAC. Default: decouple to GNDA with C = 100 nF.
6	RCAL_DAC_OUT	Input	0	Biasing of DAC for output dark level. Can be used to set output range of DAC. Default: connect to GNDA.
7	VDDA	Power	2.5	VDD of analog part [2.5V].
8	GNDA	Power	0	GND (&substrate) of analog part.
9	VDDD	Power	2.5	VDD of digital part [2.5V].
10	GNDD	Power	0	GND (&substrate) of digital part.
11	CMD_OUT_1	Input	0.78	Biasing of first stage output amplifiers. Connect to VDDAMP with R = 50 k and decouple to GNDAMP with C = 100 nF.
12	CMD_OUT_2	Input	0.97	Biasing of second stage output amplifiers. Connect to VDDAMP with R = 25 k and decouple to GNDAMP with C = 100 nF.
13	CMD_OUT_3	Input	0.67	Biasing of third stage output amplifiers. Connect to VDDAMP with R = 100 k and decouple to GNDAMP with C = 100 nF.
14	SPI_CLK	Input	-	Clock of digital parameter upload. Shifts on rising edge.
15	SPI_DATA	Input	-	Serial address and data input. 16 bit word. Address first. MSB first.
16	VDDAMP	Power	2.5	VDD of analog output [2.5V] (Can be connected to VDDA).
17	CMD_FS_ADC	Input	0.73	Biasing of first stage ADC. Connect to VDDA_ADC with R = 50 k and decouple to GNDA_ADC with C = 100 nF.
18	CMD_SS_ADC	Input	0.73	Biasing of second stage ADC. Connect to VDDA_ADC with R = 50 k and decouple to GNDA_ADC.
19	CMD_AMP_ADC	input	0.59	Biasing of input stage ADC. Connect to VDDA_ADC with R = 180 k and decouple to GNDA_ADC with C = 100 nF.
20	GNDAMP	Ground	0	GND (&substrate) of analog output.
21	OUT1	Output	Black level: 1 @ code 190 DAC_RAW reg.	Analog output 1.
22	ADC_IN1	Input	See OUT1.	Analog input ADC 1.
23	VDDAMP	Power	2.5	VDD of analog output [2.5V] (Can be connected to VDDA).

Table 20. Pin List (continued)

Pin	Pin Name	Pin Type	Expected Voltage [V]	Pin Description
24	OUT2	Output	Black level: 1 @ code 190 DAC_RAW reg.	Analog output 2.
25	ADC_IN2	Input	See OUT2.	Analog input ADC 2.
26	VDDD	Power	2.5	VDD of digital part [2.5V].
27	GNDD	Power	0	GND (&substrate) of digital part.
28	GNDA	Power	0	GND (&substrate) of analog part.
29	VDDA	Power	2.5	VDD of analog part [2.5V].
30	REG_CLOCK	Input	-	Register clock. Data on internal bus is copied to corresponding registers on rising edge.
31	SYS_CLOCK	Input	-	System clock defining the pixel rate (nominal 40 MHz, 50% +/- 5% duty cycle).
32	SYS_RESET	Input	-	Global system reset (active high).
33	Y_CLK	Input	-	Line clock.
34	Y_START	Input	-	Start frame readout.
35	GNDD_ADC	Power	0	GND (&substrate) of digital part ADC.
36	VDDD_ADC	Power	2.5	VDD of digital part [2.5V] ADC.
37	GNDA_ADC	Power	0	GND (&substrate) of analog part.
38	VDDA_ADC	Power	2.5	VDD of analog part [2.5 V].
39	VHIGH_ADC	Input	1.5	ADC high reference voltage (e.g. connect to VDDA_ADC with R = 560 Ω and decouple to GNDA_ADC with C = 100 nF.
40	VLOW_ADC	Input	0.42	ADC low reference voltage (e.g. connect to GNDA_ADC with R = 220 Ω and decouple to GNDA_ADC with C = 100 nF.
41	GNDA_ADC	Power	0	GND (&substrate) of analog part.
42	VDDA_ADC	Power	2.5	VDD of analog part [2.5 V].
43	GNDD_ADC	Power	0	GND (&substrate) of digital part ADC.
44	VDDD_ADC	Power	2.5	VDD of digital part [2.5 V] ADC.
45	VDD_RESET_DS	Power	2.5 (for no dual slope)	Variable reset voltage (dual slope).
46	ADC_CLK_EXT	Input	-	External ADC clock.
47	EOL	Output	-	Diagnostic end of line signal (produced by sequencer), can be used as Y_CLK.
48	EOF	Output	-	Diagnostic end of frame signal (produced by sequencer), can be used as Y_START.
49	PIX_VALID	Output	-	Diagnostic signal. High during pixel readout.
50	TEMP	Output	-	Temperature measurement. Output voltage varies linearly with temperature.
51	ADC_D<9>	Output	-	ADC data output (MSB).
52	VDD_PIX	Power	2.5	VDD of pixel core [2.5V].
53	GND_AB	Power	0	Anti-blooming ground. Set to 1 V for improved anti-blooming behavior.
54	ADC_D<8>	Output	-	ADC data output.
55	ADC_D<7>	Output	-	ADC data output.
56	ADC_D<6>	Output	-	ADC data output.

Table 20. Pin List (continued)

Pin	Pin Name	Pin Type	Expected Voltage [V]	Pin Description
57	ADC_D<5>	Output	-	ADC data output.
58	ADC_D<4>	Output	-	ADC data output.
59	ADC_D<3>	Output	-	ADC data output.
60	VDD_RESET	Power	2.5	Reset voltage [2.5V]. Highest voltage to the chip. 3.3 V for extended dynamic range or 'hard reset'.
61	ADC_D<2>	Output	-	ADC data output.
62	ADC_D<1>	Output	-	ADC data output.
63	ADC_D<0>	Output	-	ADC data output (LSB).
64	BS_RESET	Input	-	Boundary scan (allows debugging of internal nodes): reset. Tie to GND if not used.
65	BS_CLOCK	Input	-	Boundary scan (allows debugging of internal nodes): clock. Tie to GND if not used.
66	BS_DIN	Input	-	Boundary scan (allows debugging of internal nodes): in. Tie to GND if not used.
67	BS_BUS	Output	-	Boundary scan (allows debugging of internal nodes): bus. Leave floating if not used.
68	CMD_DEC	Input	0.74	Biasing of X and Y decoder. Connect to VDDD with R = 50 k? and decouple to GNDD with C = 100 nF.

Note on Power-on Behavior

At power-on, the chip is in an undefined state. It is advised that the power-on is accompanied by the assertion of the SYS_CLOCK and a SYS_RESET pulse that puts all internal registers in their default state (all bits are set to 0). The X-shift registers are in a defined state after the first X_SYNC which occurs a few microseconds after the first Y_START and Y_CLOCK pulse. Prior to this X_SYNC, the chip may draw more current from the analog power supply VDDA. It is therefore favorable to have separate analog and digital supplies. The current spike (if there will be any) may also be avoided by a slower ramp-up of the analog power supply or by disconnecting the resistor on pin 3 (CMD_COLAMP) at start-up.

Packaging

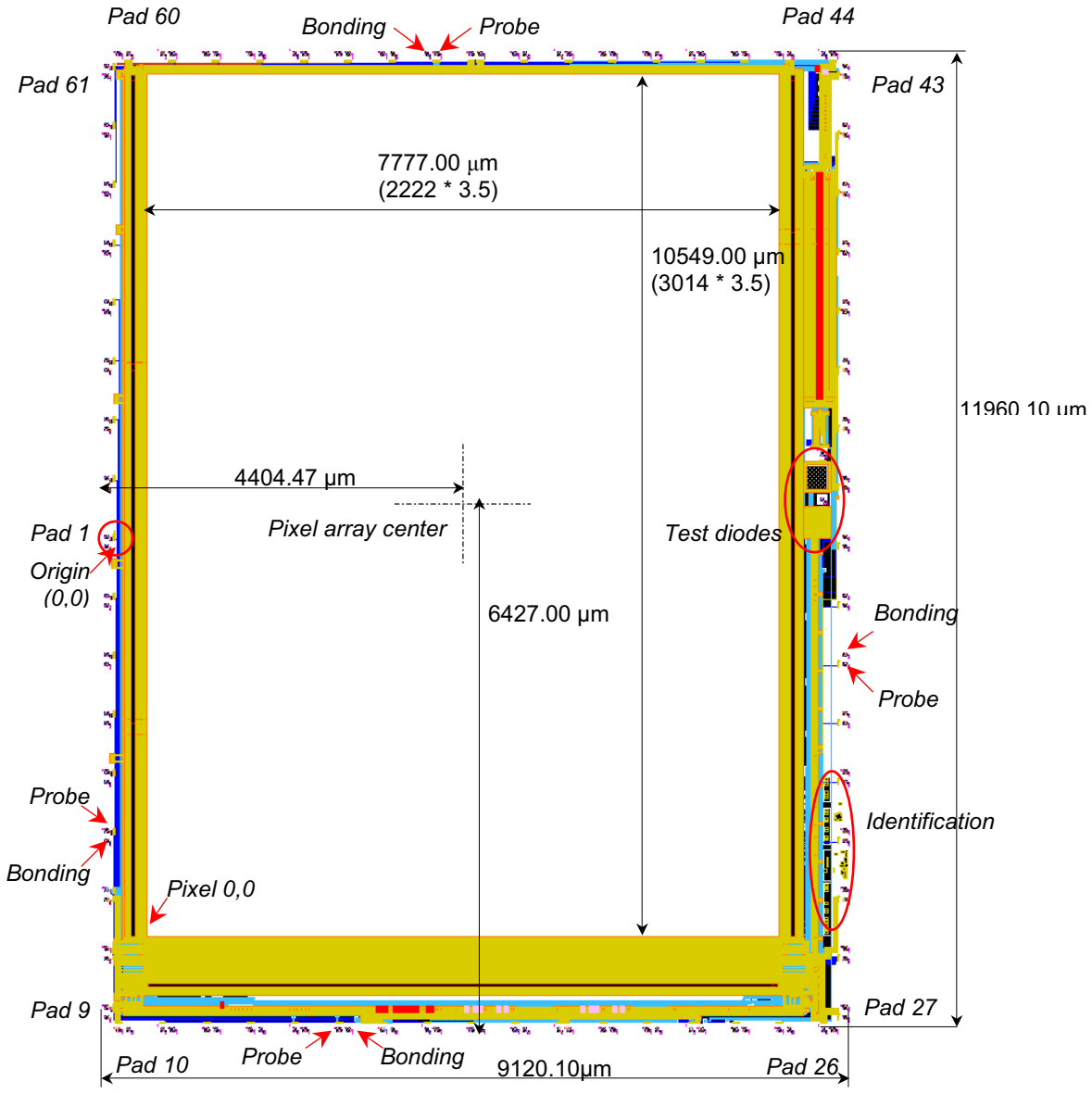
Bare Die

The IBIS4-6600 image sensor has 68 pins, 17 pins on each side. The die size from pad-edge to pad-edge (without scribe-line) is 9120.10 ?m (X) by 11960.10 ?m (Y). Scribe lines will take about 100 to 150 ?m extra on each side.

Pin 1 is located in the middle of the left side, indicated by a "1" on the layout.

A logo and some identification tags can be found on the lower right of the die (see Figure 25.).

Figure 25. Bare Die Dimensions



Package Drawing

Technical Drawing of the 68-pin LCC Package

Figure 26. Package Top View (all dimensions in inch)

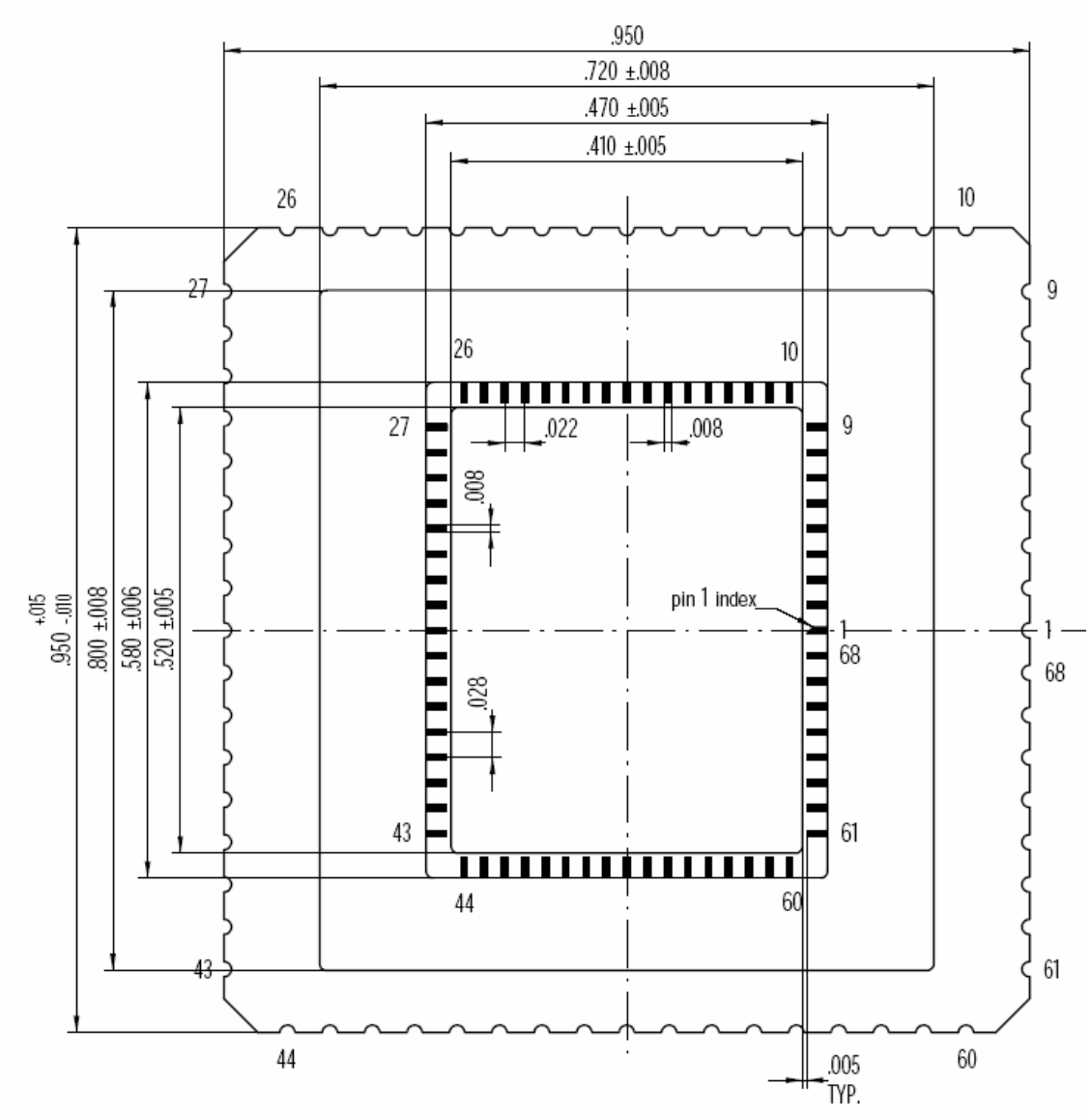


Figure 27. Package Side View (all dimensions in inch)

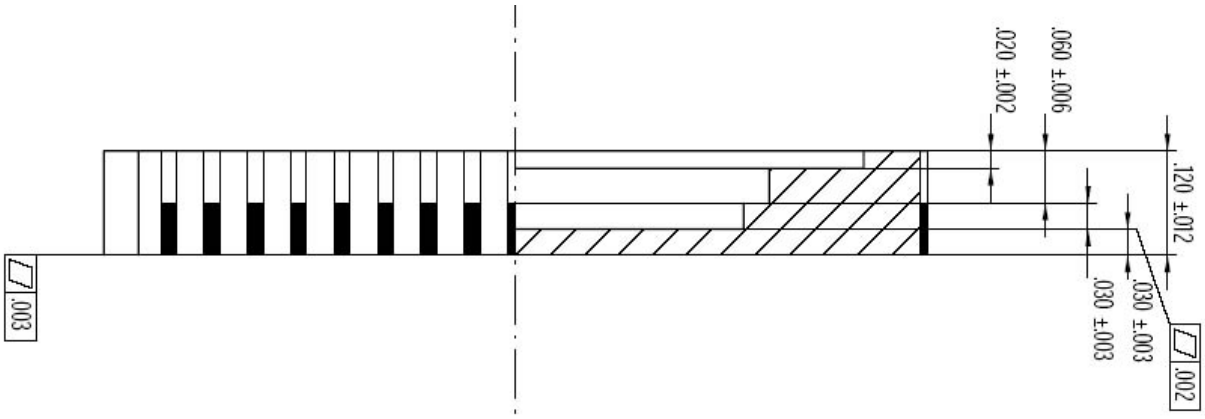


Table 21. Package Side View Dimensions.

		Inch			(mm)		
Dimension	**Description**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A	Glass (thickness)	0.037	0.039	0.039	0.950	1.000	1.050
B	Die - Si (thickness)		0.029			0.740	
C	Die attach (thickness)	0.002	0.004	0.006	0.030	0.060	0.090
D	Glass attach (thickness)	0.002	0.004	0.006	0.030	0.070	0.110
E	Imager to lid-outer surface		0.081			2.048	
F	Imager to lid-inner surface		0.039			0.978	
G	Imager to seating plane of pkg	0.060	0.061	0.062	1.512	1.562	1.612

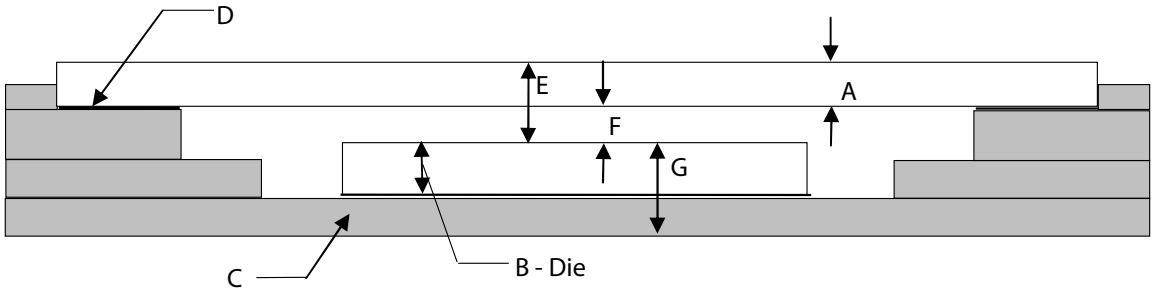
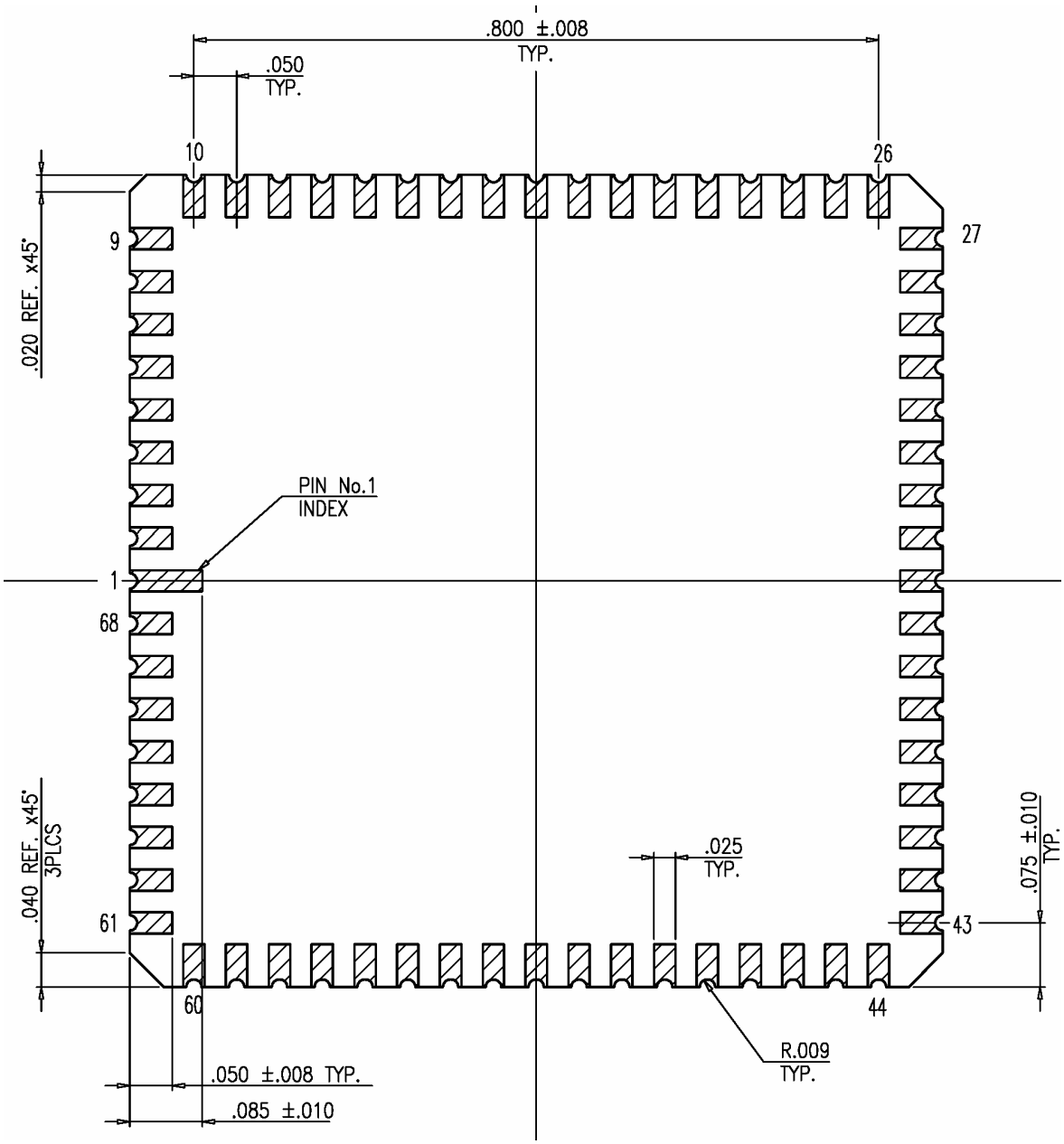
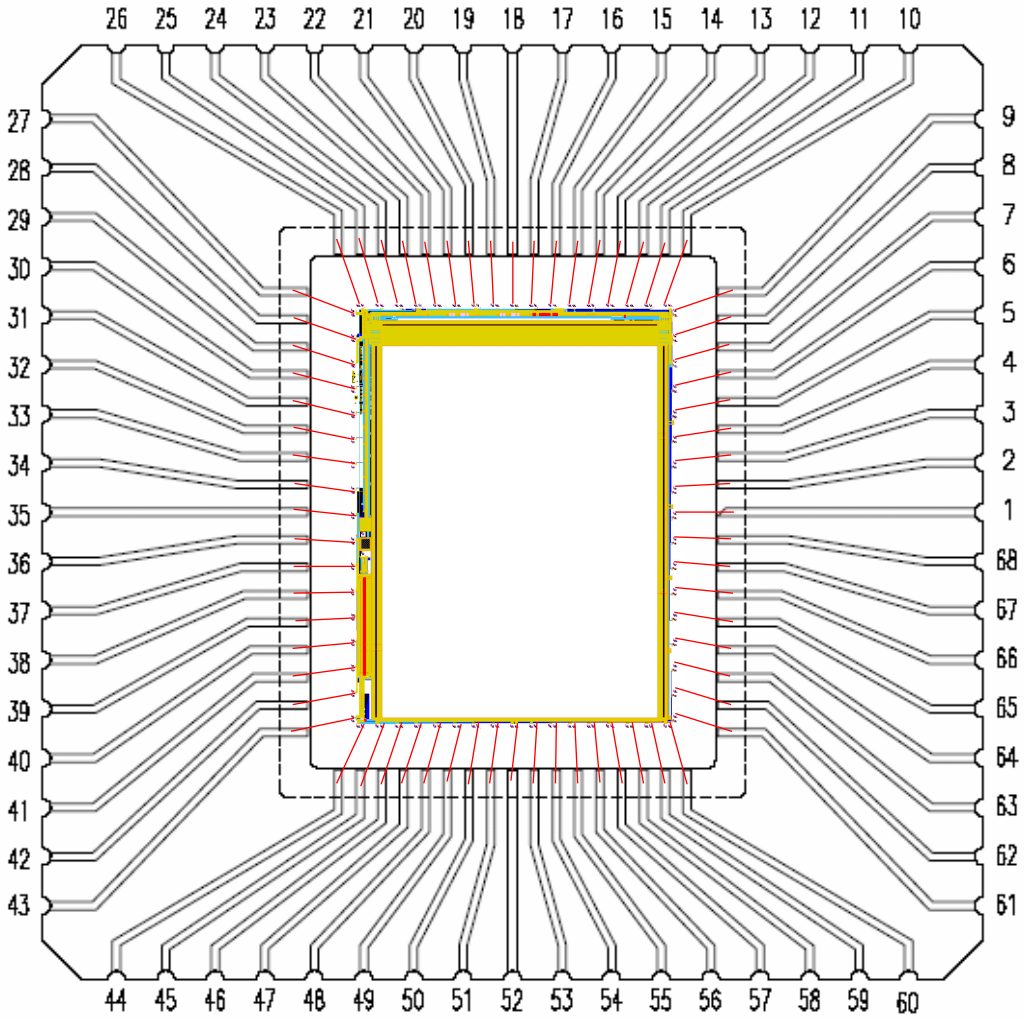


Figure 28. Package Back View (all dimensions in inch)



Bonding of the IBIS4-A-6600 in the 68-pin LCC Package

Figure 29. Bonding Scheme of the IBIS4-A-6600 in the LCC Package



The middle of the die corresponds with the middle of the package cavity (± 50 µm).

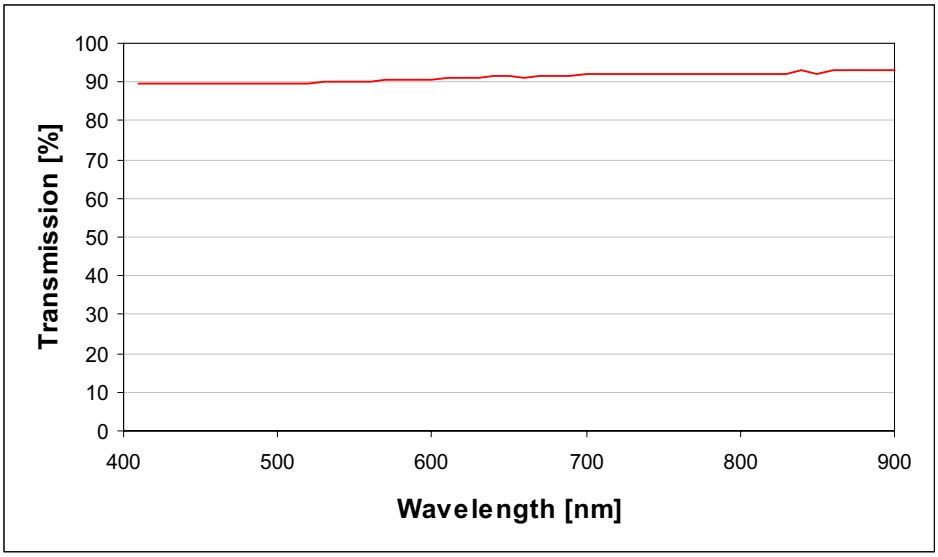
Pixel 0,0 is located at x = –4023 µm, y = –4806 µm (mechanical centre of the die/package is x = 0, y = 0).

Glass Lid Specifications

Monochrome Sensor

A D263 glass will be used as protection glass lid on top of the IBIS4-6600 monochrome sensors. The refraction index of the D263 glass lid is 1.52. Figure 30. shows the transmission characteristics of the D263 glass.

Figure 30. Transmittance Curve of the D263 Cover Glass Lid



Storage and Handling

Storage Conditions

Table 22. Storage conditions.

Description	Minimum	Maximum	Maximum
Temperature	–30	+85	°C

Handling and Soldering Conditions

Special care should be taken when soldering image sensors with color filter arrays (RGB color filters), onto a circuit board, since color filters are sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. The following recommendations are made to ensure that sensor performance is not compromised during end-users' assembly processes.

Board Assembly:

Device placement onto boards should be done in accordance with strict ESD controls for Class 0, JESD22 Human Body Model, and Class A, JESD22 Machine Model devices. Assembly operators should always wear all designated and approved grounding equipment; grounded wrist straps at ESD protected workstations are recommended including the use of ionized blowers. All tools should be ESD protected.

Manual Soldering:

When a soldering iron is used the following conditions should be observed:

Use a soldering iron with temperature control at the tip. The soldering iron tip temperature should not exceed 350°C.

The soldering period for each pin should be less than 5 seconds.

Reflow Soldering:

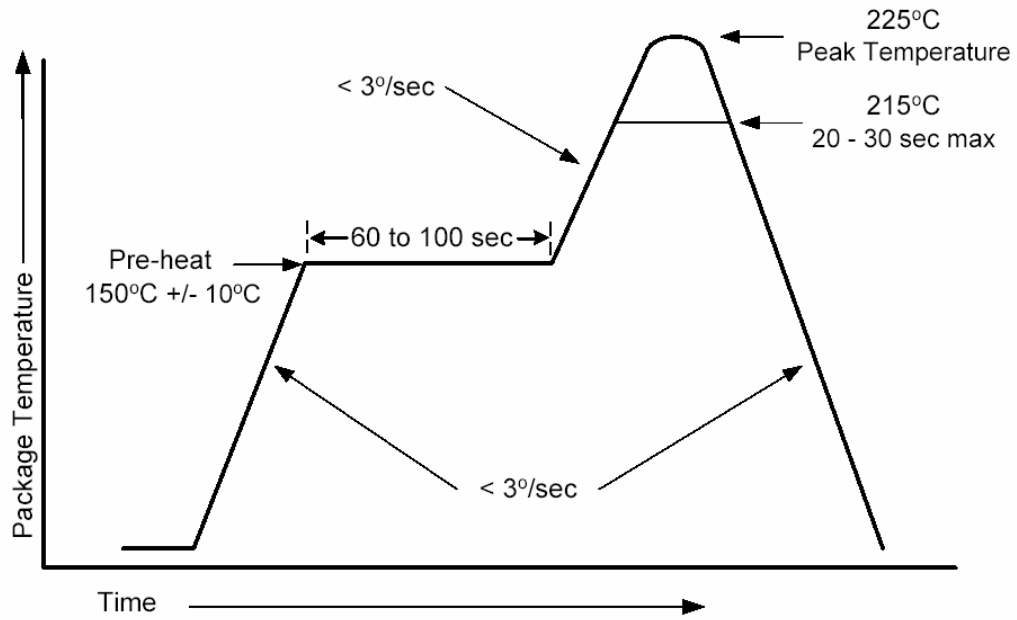
Figure 31. shows the maximum recommended thermal profile for a reflow soldering system. If the temperature/time profile exceeds these recommendations damage to the image sensor may occur. See Figure 31. for more details.

Precautions and cleaning:

Avoid spilling solder flux on the cover glass; bare glass and particularly glass with antireflection filters may be adversely affected by the flux. Avoid mechanical or particulate damage to the cover glass.

It is recommended that isopropyl alcohol (IPA) is used as a solvent for cleaning the image sensor glass lid. When using other solvents, it should be confirmed beforehand whether the solvent will dissolve the package and/or the glass lid or not.

Figure 31. Reflow Soldering Temperature Profile



RoHS (lead free) Compliance

This paragraph reports the use of Hazardous chemical substances as required by the RoHS Directive (excluding packing material).

Table 23. The Chemical Substances and Information about Any Intentional Content

Chemical Substance	Any intentional content	If there is any intentional content, in which portion is it contained?
Lead	NO	-
Cadmium	NO	-
Mercury	NO	-
Hexavalent chromium	NO	-
PBB (Polybrominated biphenyls)	NO	-
PBDE (Polybrominated diphenyl ethers)	NO	-

Information on lead free soldering:

IBIS4-A-6600-M2 (serial numbers beyond 3694): the product was tested successfully for lead-free soldering processes, using a reflow temperature profile with maximum 260°C, minimum 40s at 255°C and minimum 90s at 217°C.

IBIS4-A-6600-C2: the product will not withstand a lead free soldering process. Maximum allowed reflow or wave soldering temperature is 220°C. Hand soldering is recommended for this part type.

Note:

"Intentional content" is defined as any material demanding special attention is contained into the inquired product by following cases:

1. A case that the above material is added as a chemical composition into the inquired product intentionally in order to produce and maintain the required performance and function of the intended product
2. A case that the above material, which is used intentionally in the manufacturing process, is contained in or adhered to the inquired product

The following case is not treated as "intentional content":

1. A case that the above material is contained as an impurity into raw materials or parts of the intended product. The impurity is defined as a substance that cannot be removed industrially, or it is produced at a process such as chemical composing or reaction and it cannot be removed technically.

Ordering Information

Table 24. Ordering Information.

Cypress Part number	Package	Glass Lid	Mono/Color
CYII4SC6600AB-QDC	68-pin LCC	D263	RGB Bayer pattern
CYII4SM6600AB-QDC	68-pin LCC	D263	B&W
CYII4SC6600AB-HDC	84-pinJLCC	D263	RGB Bayer pattern
CYII4SM6600AB-HDC	84-pin JLCC	D263	B&W

* JLCC package for use in evaluation kits only.

** D263 is used as monochrome glass lid (see Figure 30. for spectral transmittance).

Other packaging combinations are available upon special request.

Disclaimer

The IBIS4-6600 sensor is only to be used for non-low vision aid applications. A strict exclusivity agreement prevents us to sell the IBIS4-6600 sensor to customers who intend to use it for the above specified applications.

All products and company names mentioned in this document may be the trademarks of their respective holders.

Document History Page

Document Title: IBIS4-A-6600 CMOS image sensor Document Number: 001-02366				
REV.	**ECN.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	384900	See ECN	FWU	Origination.
*A	402976	See ECN	FWU	Preliminary notice removed. Electro-optical spec updated to characterization data.
*B	418669	See ECN	FVK	Table 20. ADC resistor values changed ADC section added Figure 29. p41 corrected
*C	502551	See ECN	QGS	Converted to Frame file
*D	642596	See ECN	FPW	Ordering information update