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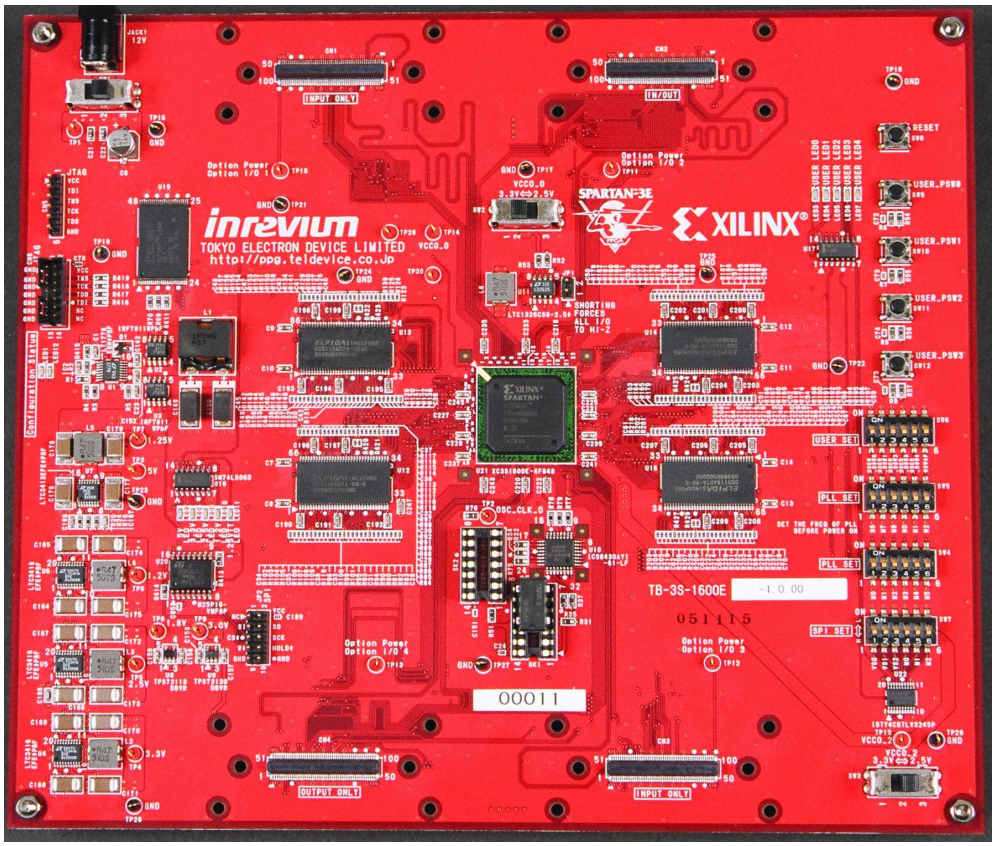

TB-3S-1600E

SPARTAN3E Evaluation Board
TB-3S-1600E
Hardware User's Guide Rev1.1

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1. Accessories

■ 12V 4A AC Adaptor
■ User's Manual
■ Board Mounting Leg

2. Precautions

■ The product and the information contained in this manual is subject to change without prior notice for improvement.

■ Every possible effort has been made to avoid any errors in this document. Should an error or other problems be found, please do not hesitate to contact us.

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■ This board has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

■ Repair of the board is carried out by replacing it on a chargeable basis; not repairing the faulty devices.

■ Replacement of initial faults carried out by free of charge, however, it is required for the customer to inform us of relevant problem within two weeks after delivery.

3. Overview

The TB-3S-1600E evaluation board is equipped with high performance, low cost Spartan-3E series and DDR SDRAM chips for evaluation of these chips. It can support a wide variety of application evaluation, allowing significant reduction of design load and development period for faster time to market.

4. Feature

■ FPGA
Xilinx XC3S1600E-4FG484C

■ Elpida Memory EDD5116ADTA-6B-E (512Mbit x16): 4 chips
Four DDR SDRAM Memory Chips (512Mbit) allows high speed data memory access (266Mbps or more).

■ST Micro Serial Flash Memory M25P16-VMF6P
One SPI 16Mbit memory chip allows configuration from SPI and use of any data storage.

■Clock PLL
The board is equipped with an external PLL to support the input signals to FPGA with various clock frequencies.

■ Sample Application
Sample applications including high speed DDR SDRAM interface (266Mbps or higher) and DVI interface come with the board to support prompt evaluation need.

■ Dedicated Option Boards
A variety of option boards are available for high speed extension I/O connection in DVI, CameraLink, optical link, USB or AD/DA I/F (TBD) application.

5. Block Diagram

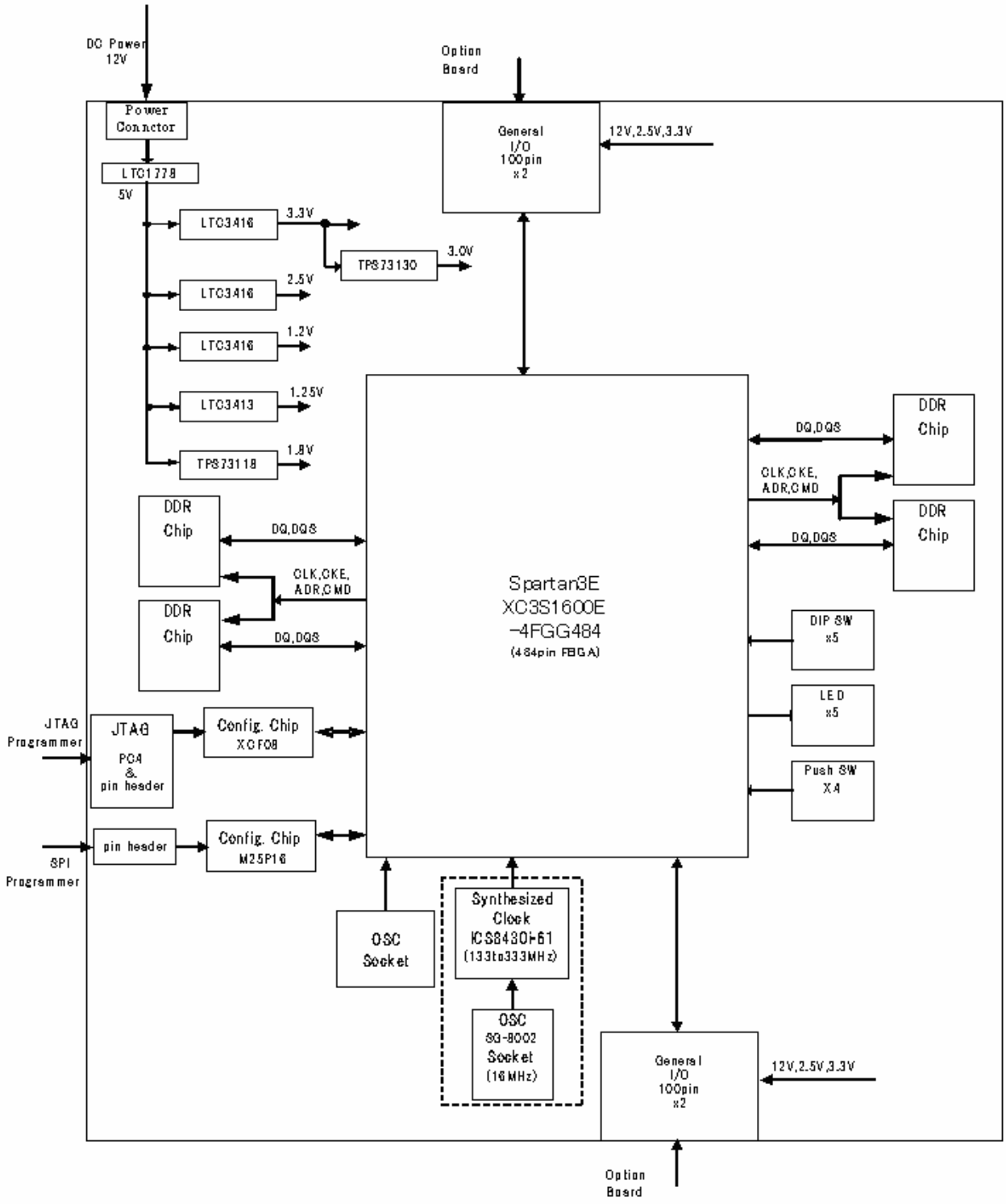


Figure.1 TB-3S-1600E Block diagram

6. External View

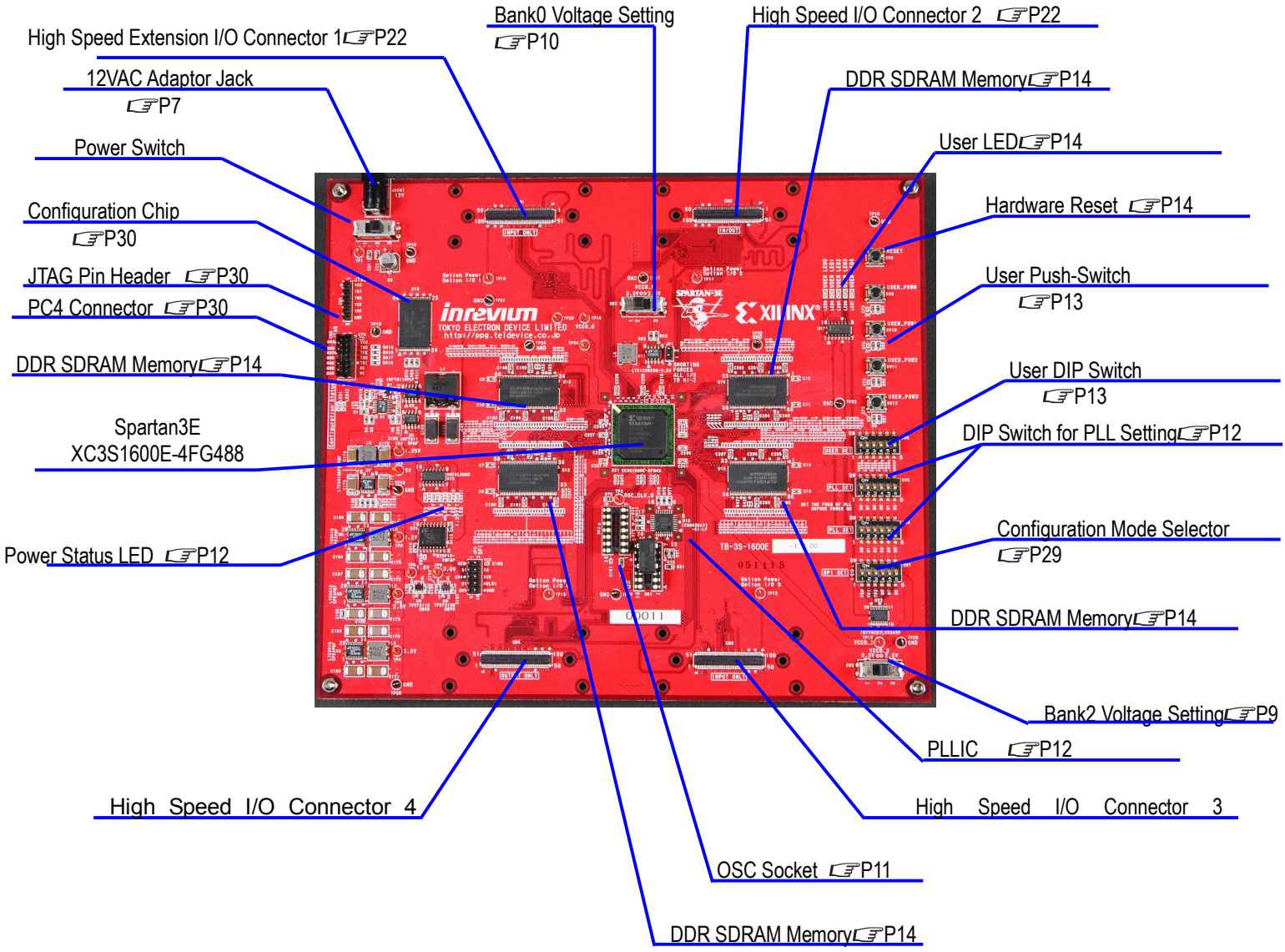


Figure.2 TB-3S-1600E External View

7. Specification

Dimension : 200mm x 230mm
# of Board Layer : 8
Thickness : 1.6mm
Board Material : General FR4
FPGA : Xilinx XC3S1600E-4FG484C
Configuration PROM : XCF08PVO48
Memory Chip : 4 x Elpida Memory EDD5116ADTA(512Mbit x16) chips
General Purpose SPI Memory: ST Micro SPI Memory M25P16-VMF6P
High Speed Extension I/O : 4 x 100-pin connector（I/O:42-pin）

8. Board Components

Power Connector and Power Module

Single 12V power is externally supplied from the AC adaptor that comes with the board. Set SW1 to the 1-pin side to turn off or to the 3-pin side to turn on.

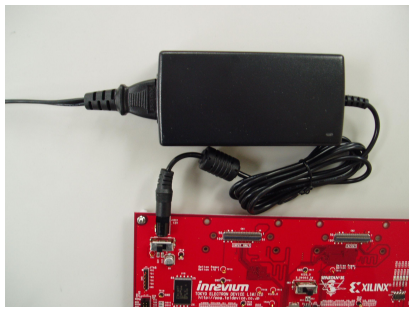


Figure.3 AC Adapter Connection

Power Supply Connections

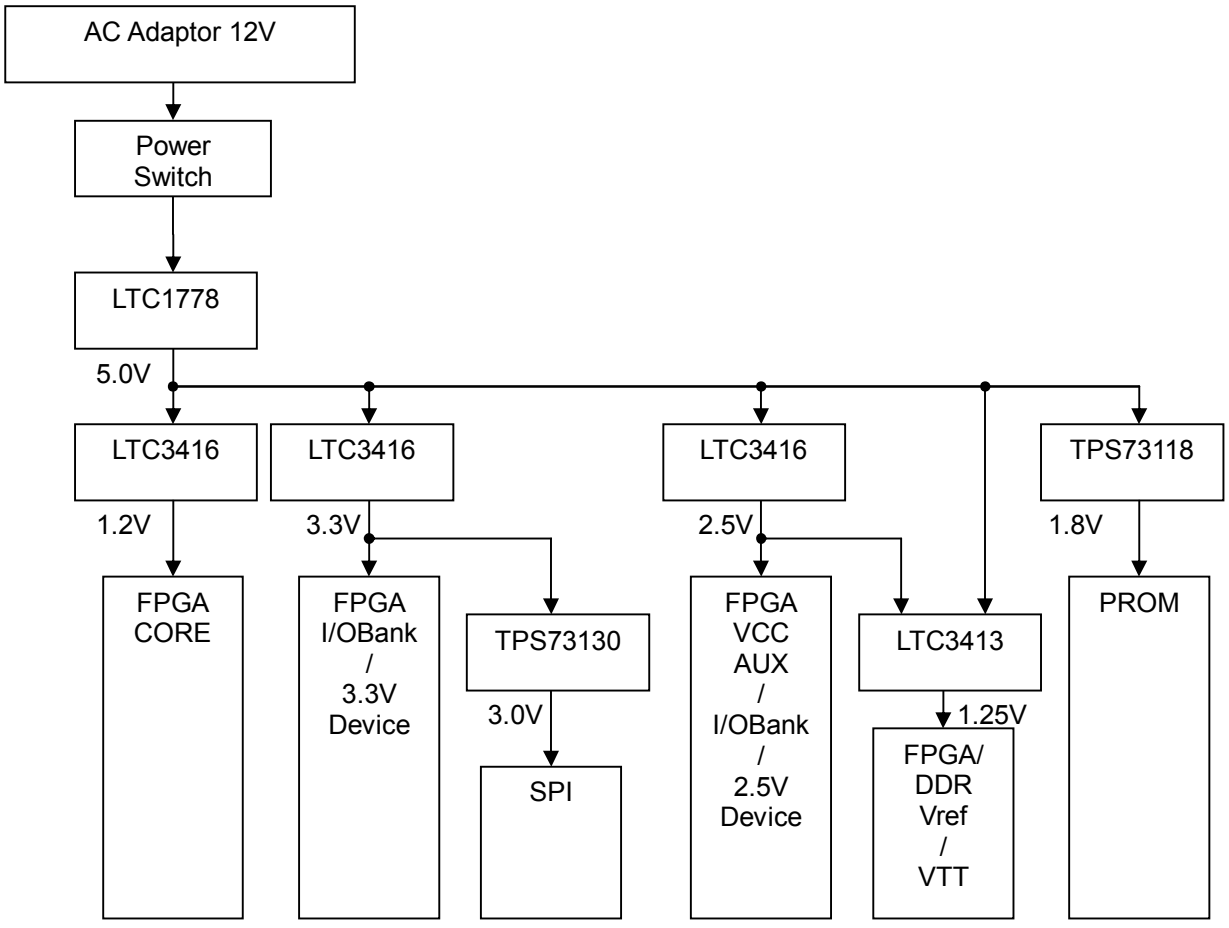


Figure.4 Power Supply Connection Diagram

Power Status LED

Power Status LEDs（LED2, LED8, LED9, LED10 and LED11）indicate that the power supply is running normally. Ensure that all Leeds are turned on, otherwise something is wrong with the board. Switch off the power supply since there may be a short circuit between the FPGA user circuit and a device.
LEDs for 1.8V/3.0V operation are not available.

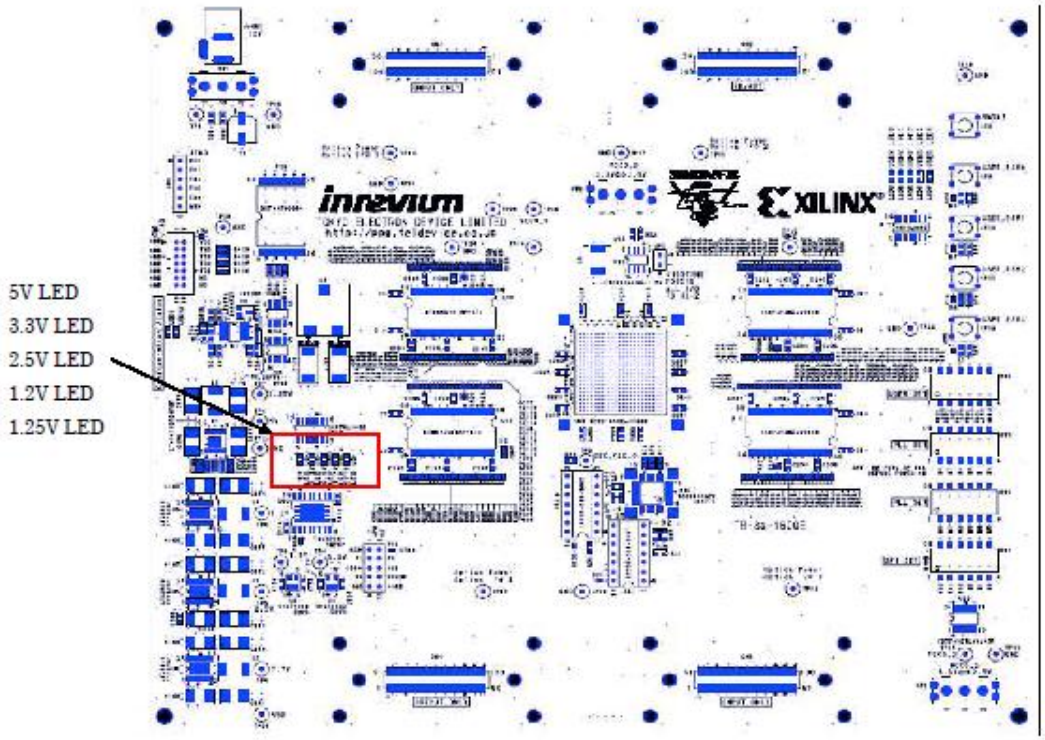


Figure.5 Power Supply status LED location

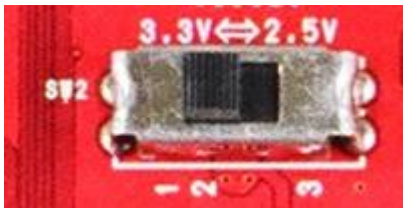
Power Voltage Selector for FPGAI/O Bank0,2

VCCO power voltage of I/OBank0, 2 can be selectable for 2.5V or 3.3V operation.

- Bank0、Bank2
  Connected to: High Speed I/O Connector

Set onboard slide switches SW2 and SW3 to a desired power voltage in accordance with a signal level of a device to which the high speed I/O connector is connected.

3.3V Setting



2.5V Setting

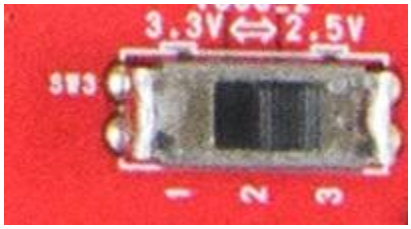


Figure.6 Slide Switch Setting for FPGA Bank0/2 Voltage Switching

Oscillator

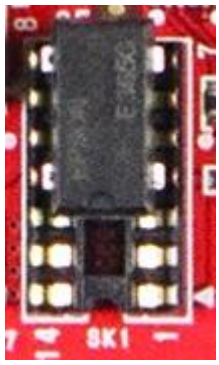
The board is provided with one differential LV-PECL PLLIC (DIP switch setting for variable frequency) and one oscillator socket that is connected to the FPGA's GCLK pin.
Be sure to set the 16MHz oscillator that comes with the board to a correct pin position of the oscillator socket (SK1) that is connected to the PLLIC.
If an oscillator other than that provided with the board is used, be sure to select a 3.3V oscillator. Either DIP14 or DIP8 pin size oscillator package can be supported.

BD Silk	Pin Name	FPGA Pin#	FPGA I/O Bank
SK1	IO_L22P_2/D2/GCLK2	Y12	2
	IO_L22N_2/D1/GCLK3	W12	2
SK2	IP_L21P_2/RDWR_B/GCLK0	R12	2

Table.1 Oscillator Pin Assignment

Example of Oscillator Setting

DIP8 Pin Type



For DIP14 pin type package, make sure to mount it so that 1-pin of the socket meets 1-pin of the oscillator.

Figure.7 How to insert an Oscillator

PLLIC (ICS8430-61) Setting

DIP switches SW4 and SW5 are used to set output frequency of PLLIC.
Output frequency can be obtained in the following formula.

Fout = (fxtal/16)×(M/N)

Be sure to set it so that internal VCO frequency fvco = (fxtal/16)x M is within a range of 250 - 500MHz.

Value of M	256	128	64	32	16	8	4	2	1
	M8	M7	M6	M5	M4	M3	M2	M1	M0
250	0	1	1	1	1	1	0	1	0
251	0	1	1	1	1	1	0	1	1
252	0	1	1	1	1	1	1	0	0
253	0	1	1	1	1	1	1	0	1
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
500	1	1	1	1	1	0	1	0	0

N	N2	N1	N0
1	0	0	0
1.5	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
6	1	0	1
8	1	1	0
12	1	1	1

Table.2 ICS8430-61 Setting Table

Set the DIP switch to OFF to set 1 or ON to set 0.

See Table 3 DIP Switch Setting for relationship between DIP switch setting and PLL output frequency when a 16MHz oscillator that comes with the board is used.

Output Frequency (MHz)	SW5						SW4					
	N2	N1	N0	M8	M7	M6	M5	M4	M3	M2	M1	M0
133	ON	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
166	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON
266	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
333.33	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	ON

Table.3 Dip Switch Setting Table

User DIP Switch

A 5bit DIP switch is connected to the I/O of FPGA. Set the switch to ON to set Low or OFF to set High. Note that the 6-pin of SW6 is not for user switch.

Table.4 User DIP Switch Pin Assignment

BD Silk		DIP Switch #	FPGA Pin #	FPGA I/O Bank
SW6	USER_DSW0	1	P20	1
	USER_DSW1	2	R15	1
	USER_DSW2	3	T17	1
	USER_DSW3	4	T20	1
	USER_DSW4	5	U18	1

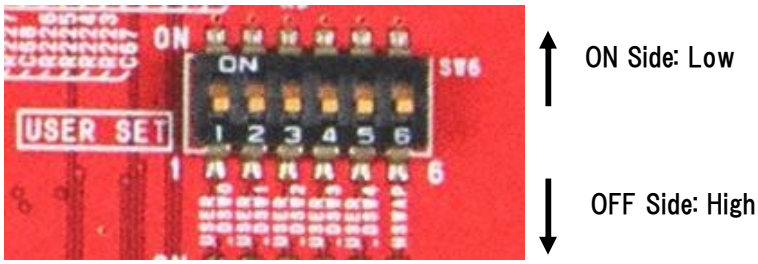


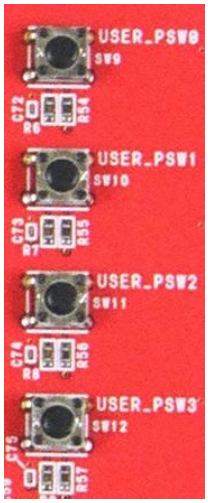
Figure.8 DIP Switch Setting Diagram

Pushbutton Switch

Four pushbutton switches are connected to the I/O of FPGA. While each switch is depressed, I/O of FPGA is set to Low.

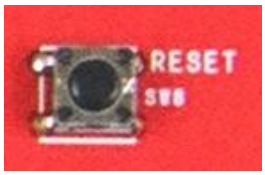
BD Silk		FPGA Pin #	FPGA I/O Bank
SW3	PSW1	A16	3
SW4	PSW2	B13	3
SW5	PSW3	C15	3
SW6	PSW4	C14	3
SW7	PSW5	B17	3
SW8	PSW6	A17	3

Table.5 User Push Switch Pin Assignment



Reset Pushbutton Switch

A reset pushbutton switch (SW8) is connected to an IC. Depress the switch for a short time (within 1.4 seconds) to output a reset pulse from a reset IC to FPGA. If the switch is depressed for a longer time (3 seconds or more), FPGA is reconfigured.



User LED

Five red LEDs can be used from FPGA. Each LED is turned on when set to High.

BD Silk	FPGA Pin #	FPGA I/O Bank
USER_LED0	R20	1
USER_LED1	T22	1
USER_LED2	U22	1
USER_LED3	L22	1
USER_LED4	P16	1

Table.6 User LED Assignment

Onboard DDR SDRAM Memory

The board is equipped with four DDR SDRAM memory chips with 512Mbit, 16bit data width per memory.
Two for Bank1 side and other two for Bank3 side share address, command and clock signals. Therefore, from the point of view of FPGA, it looks as if two memory chips with 32bit width are connected to the data bus. The memory chips at Bank1 side and Bank3 side are independently connected.

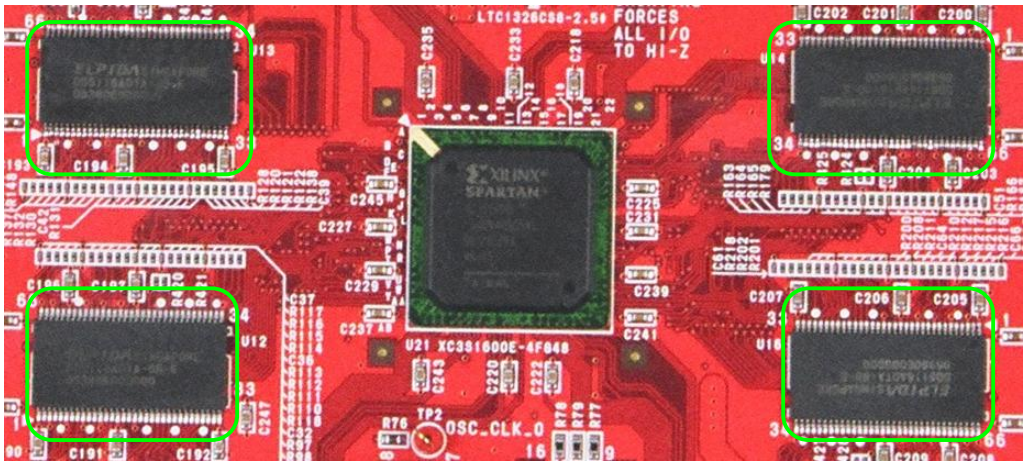


Figure.9 DDR SDRAM Memory

DDR SDRAM Memory Pin Assignment Table

BD Silk	Signal Name	FPGA Pin #	FPGA I/O Bank
IC12	DQ0	Y1	3
	DQ1	Y2	3
	DQ2	W2	3
	DQ3	V4	3
	DQ4	V1	3
	DQ5	W1	3
	DQ6	T5	3
	DQ7	T4	3
	DQ8	U1	3
	DQ9	T6	3
	DQ10	R6	3
	DQ11	R3	3
	DQ12	P5	3
	DQ13	P6	3
	DQ14	P7	3
	DQ15	R7	3
	LDQS	U4	3
	UDQS	R2	3
	LDM	V3	3
	UDM	R4	3

DDR SDRAM Memory Pin Assignment Table (continued from previous page)

BD Silk	Signal Name	FPGA Pin #	FPGA I/O Bank
IC12	A0	D3	3
	A1	G7	3
	A2	N5	3
	A3	C1	3
	A4	C26	3
	A5	E3	3
	A6	E4	3
	A7	E1	3
	A8	D1	3
	A9	F4	3
	A10	F3	3
	A11	G5	3
	A12	G4	3
	BA0	M1	3
	BA1	L7	3
	CK	AA2	3
	/CK	AA1	3
	CKE	F1	3
	CS	H2	3
	RAS	H3	3
	CAS	G1	3
	WE	H5	3
IC13	DQ0	N8	3
	DQ1	N6	3
	DQ2	N7	3
	DQ3	M4	3
	DQ4	L8	3
	DQ5	M8	3
	DQ6	M5	3
	DQ7	L5	3
	DQ8	K7	3
	DQ9	K1	3
	DQ10	L1	3
	DQ11	K4	3
	DQ12	K3	3
	DQ13	J6	3
	DQ14	J5	3
	DQ15	H1	3

DDR SDRAM Memory Pin Assignment Table (continued from previous page)

BD Silk	Signal Name	FPGA Pin #	FPGA I/O Bank
IC13	LDQS	N1	3
	UDQS	J8	3
	LDM	M3	3
	UDM	K5	3
	A0	D3	3
	A1	G7	3
	A2	N5	3
	A3	C1	3
	A4	C26	3
	A5	E3	3
	A6	E4	3
	A7	E1	3
	A8	D1	3
	A9	F4	3
	A10	F3	3
	A11	G5	3
	A12	G4	3
	BA0	M1	3
	BA1	L7	3
	CK	AA2	3
	/CK	AA1	3
	CKE	F1	3
	CS	H2	3
	RAS	H3	3
	CAS	G1	3
	WE	H5	3

DDR SDRAM Memory Pin Assignment Table (continued from previous page)

BD Silk	Signal Name	FPGA Pin #	FPGA I/O Bank
IC14	DQ0	C21	3
	DQ1	B22	3
	DQ2	E20	3
	DQ3	C22	3
	DQ4	D22	3
	DQ5	E22	3
	DQ6	G18	3
	DQ7	G19	3
	DQ8	F22	3
	DQ9	G20	3
	DQ10	H17	3
	DQ11	G22	3
	DQ12	J17	3
	DQ13	H22	3
	DQ14	J20	3
	DQ15	J18	3
	LDQS	F19	3
	UDQS	H20	3
	LDM	B21	3
	UDM	E19	3
	A0	Y21	3
	A1	W21	3
	A2	V20	3
	A3	U21	3
	A4	N20	3
	A5	N22	3
	A6	M22	3
	A7	M15	3
	A8	M16	3
	A9	U19	3
	A10	V19	3
	A11	V22	3
	A12	W22	3
	BA0	AA22	3
	BA1	Y22	3
	CK	T16	3
	/CK	R16	3
	CKE	H19	3
	CS	R18	3
	RAS	T19	3
	CAS	T18	3
	WE	R19	3

DDR SDRAM Memory Pin Assignment Table (continued from previous page)

BD Silk	Signal Name	FPGA Pin #	FPGA I/O Bank
IC16	DQ0	K19	3
	DQ1	K18	3
	DQ2	K17	3
	DQ3	K16	3
	DQ4	L19	3
	DQ5	L18	3
	DQ6	L21	3
	DQ7	L20	3
	DQ8	N16	3
	DQ9	N17	3
	DQ10	N18	3
	DQ11	N19	3
	DQ12	P22	3
	DQ13	R22	3
	DQ14	R21	3
	DQ15	P17	3
	LDQS	K22	3
	UDQS	P15	3
	LDM	G17	3
	UDM	J21	3
	A0	Y21	3
	A1	W21	3
	A2	V20	3
	A3	U21	3
	A4	N20	3
	A5	N22	3
	A6	M22	3
	A7	M15	3
	A8	M16	3
	A9	U19	3
	A10	V19	3
	A11	V22	3
	A12	W22	3
	BA0	AA22	3
	BA1	Y22	3
	CK	T16	3
	/CK	R16	3
	CKE	H19	3
	CS	R18	3
	RAS	T19	3
	CAS	T18	3
	WE	R19	3

Table.9 DDR SDRAM Memory Pin Assignment

High Speed Extension I/O Connector

Assuming the high speed image data input from an external device, the board provides 5 LVDS pairs for data, 2 LVDS pairs for clock parallel and other signal lines at 50Ω.
It also provides GND, VCC(2.5V,3.3V) and +12V power supply.
Note that input and output setting of each connector is predefined (CN1: input only, CN2: both input and output, CN3: input only and CN4: output only). Be careful about this when option boards are installed. The signal directions are mainly to or from FPGA.

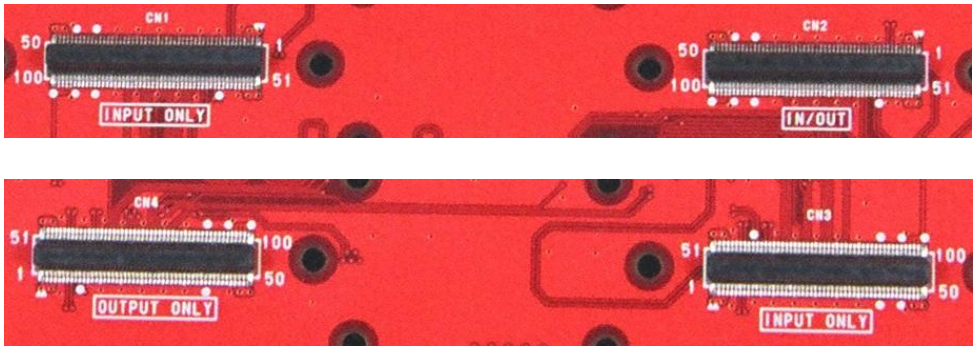


Figure.10 High-Speed Extended I/O Connector

High Speed Extension I/O Pin Assignment Table ((IP) of FPGA Pin # indicates dedicated input pin).

BD Silk	Connector Pin #	Signal Name	FPGA Pin #	FPGA I/O Bank
CN1	1	+3.3V	—	—
	2			
	3			
	4			
	5	GND	—	—
	6	GND	—	—
	7	JAE1_OPT_IO0	C11	0
	8	JAE1_OPT_IO1	B11	0
	9	GND	—	—
	10	JAE1_OPT_IO2	B9	0
	11	JAE1_OPT_IO3	C9	0
	12	GND	—	—
	13	JAE1_OPT_IO4	D9	0
	14	JAE1_OPT_IO5	E9	0
	15	GND	—	—
	16	JAE1_OPT_IO12	A5	0
	17	JAE1_OPT_IO13	A4	0
	18	JAE1_OPT_IO14	D7	0
	19	JAE1_OPT_IO15	E7	0
	20	GND	—	—
	21	JAE1_OPT_IO16	D5	0
	22	JAE1_OPT_IO17	D6	0
	23	JAE1_OPT_IO18	B3	0
	24	JAE1_OPT_IO19	B4	0
	25	GND	—	—

High Speed Extension I/O Pin Assignment Table (continued from previous page)

BD Silk	Connector Pin #	Signal Name	FPGA Pin #	FPGA I/O Bank
CN1	26	JAE1_OPT_IO20	D18(IP)	0
	27	JAE1_OPT_IO21	D17(IP)	0
	28	JAE1_OPT_IO22	B17(IP)	0
	29	JAE1_OPT_IO23	C17(IP)	0
	30	GND	—	—
	31	JAE1_OPT_IO24	D15(IP)	0
	32	JAE1_OPT_IO25	E15(IP)	0
	33	JAE1_OPT_IO26	C13(IP)	0
	34	JAE1_OPT_IO27	D13(IP)	0
	35	GND	—	—
	36～45			
	46	GND	—	—
	47	+12V	—	—
	48			
	49			
	50			
	51	+2.5V	—	—
	52			
	53			
	54			
	55	GND	—	—
	56	GND	—	—
	57	JAE1_OPT_IO6	A8	0
	58	JAE1_OPT_IO7	B8	0
	59	GND	—	—
	60	JAE1_OPT_IO8	F8	0
	61	JAE1_OPT_IO9	F7	0
	62	GND	—	—
	63	JAE1_OPT_IO10	A7	0
	64	JAE1_OPT_IO11	A6	0
	65	GND	—	—
	66	JAE1_OPT_IO28	A13(IP)	0
	67	JAE1_OPT_IO29	A12(IP)	0
	68	JAE1_OPT_IO30	F11(IP)	0
	69	JAE1_OPT_IO31	F10(IP)	0
	70	GND	—	—
	71	JAE1_OPT_IO32	G10(IP)	0
	72	JAE1_OPT_IO33	G9(IP)	0
	73	JAE1_OPT_IO34	D8(IP)	0
	74	JAE1_OPT_IO35	C8(IP)	0
	75	GND	—	—

High Speed Extension I/O Pin Assignment Table (continued from previous page)

BD Silk	Connector Pin #	Signal Name	FPGA Pin #	FPGA I/O Bank
CN1	76	JAE1_OPT_IO36	C6(IP)	0
	77	JAE1_OPT_IO37	C7(IP)	0
	78	JAE1_OPT_IO38	A2(IP)	0
	79	JAE1_OPT_IO39	A3(IP)	0
	80	GND	—	—
	81	JAE1_OPT_IO40	H12(IP)	0
	82	JAE1_OPT_IO41	H11(IP)	0
	83			
	84			
	85	GND	—	—
	86～95			
	96	GND	—	—
	97	Option Power	—	—
	98			
	99			
	100			
CN2	1	+3.3V	—	—
	2			
	3			
	4			
	5	GND	—	—
	6	GND	—	—
	7	JAE2_OPT_IO0	F12	0
	8	JAE2_OPT_IO1	E12	0
	9	GND	—	—
	10	JAE2_OPT_IO2	H13	0
	11	JAE2_OPT_IO3	J13	0
	12	GND	—	—
	13	JAE2_OPT_IO4	F13	0
	14	JAE2_OPT_IO5	G13	0
	15	GND	—	—
	16	JAE2_OPT_IO12	F15	0
	17	JAE2_OPT_IO13	G15	0
	18	JAE2_OPT_IO14	C15	0
	19	JAE2_OPT_IO15	B15	0
	20	GND	—	—
	21	JAE2_OPT_IO16	A17	0
	22	JAE2_OPT_IO17	A16	0
	23	JAE2_OPT_IO18	D16	0
	24	JAE2_OPT_IO19	C16	0
	25	GND	—	—

High Speed Extension I/O Pin Assignment Table (continued from previous page)

BD Silk	Connector Pin #	Signal Name	FPGA Pin #	FPGA I/O Bank
CN2	26	JAE2_OPT_IO20	A18	0
	27	JAE2_OPT_IO21	A19	0
	28	JAE2_OPT_IO22	A21	0
	29	JAE2_OPT_IO23	A20	0
	30	GND	—	—
	31	JAE2_OPT_IO24	C19	0
	32	JAE2_OPT_IO25	C18	0
	33	JAE2_OPT_IO26	G12	0
	34	JAE2_OPT_IO27	J11	0
	35	GND	—	—
	36～45			
	46	GND	—	—
	47	+12V	—	—
	48			
	49			
	50			
	51	+2.5V	—	—
	52			
	53			
	54			
	55	GND	—	—
	56	GND	—	—
	57	JAE2_OPT_IO6	G14	0
	58	JAE2_OPT_IO7	H14	0
	59	GND	—	—
	60	JAE2_OPT_IO8	A15	0
	61	JAE2_OPT_IO9	A14	0
	62	GND	—	—
	63	JAE2_OPT_IO10	E14	0
	64	JAE2_OPT_IO11	D14	0
	65	GND	—	—
	66	JAE2_OPT_IO28	H15	0
	67	JAE2_OPT_IO29	H10	0
	68	JAE2_OPT_IO30	G8	0
	69	JAE2_OPT_IO31	F16	0
	70	GND	—	—
	71	JAE2_OPT_IO32	H9	0
	72	JAE2_OPT_IO33	H8	0
	73	JAE2_OPT_IO34	C10	0
	74	JAE2_OPT_IO35	D10	0
	75	GND	—	—

High Speed Extension I/O pin Assignment Table (continued from previous page)

BD Silk	Connector Pin #	Signal Name	FPGA Pin #	FPGA I/O Bank
CN2	76	JAE2_OPT_IO36	A10	0
	77	JAE2_OPT_IO37	A9	0
	78	JAE2_OPT_IO38	E11	0
	79	JAE2_OPT_IO39	D11	0
	80	GND	—	—
	81	JAE2_OPT_IO40	B12	0
	82	JAE2_OPT_IO41	C12	0
	83			
	84			
	85	GND	—	—
	86～95			
	96	GND	—	—
	97	Option Power	—	—
	98			
	99			
	100			
CN3	1	+3.3V	—	—
	2			
	3			
	4			
	5	GND	—	—
	6	GND	—	—
	7	JAE3_OPT_IO0	R11	2
	8	JAE3_OPT_IO1	T11	2
	9	GND	—	—
	10	JAE3_OPT_IO2	AB19(IP)	2
	11	JAE3_OPT_IO3	AA19(IP)	2
	12	GND	—	—
	13	JAE3_OPT_IO4	W16(IP)	2
	14	JAE3_OPT_IO5	Y16(IP)	2
	15	GND	—	—
	16	JAE3_OPT_IO12	W10(IP)	2
	17	JAE3_OPT_IO13	Y10(IP)	2
	18	JAE3_OPT_IO14	AB6(IP)	2
	19	JAE3_OPT_IO15	AB7(IP)	2
	20	GND	—	—
	21	JAE3_OPT_IO16	AA6(IP)	2
	22	JAE3_OPT_IO17	Y6(IP)	2
	23	JAE3_OPT_IO18	Y4(IP)	2

High Speed Extension I/O pin Assignment Table (continued from previous page)

BD Silk	Connector Pin #	Signal Name	FPGA Pin #	FPGA I/O Bank
CN3	24	JAE3_OPT_IO19	AA4(IP)	2
	25	GND	—	—
	26	JAE3_OPT_IO20	AB2(IP)	2
	27	JAE3_OPT_IO21	V17(IP)	2
	28	JAE3_OPT_IO22	W18	2
	29	JAE3_OPT_IO23	Y18	2
	30	GND	—	—
	31	JAE3_OPT_IO24	Y17	2
	32	JAE3_OPT_IO25	W17	2
	33	JAE3_OPT_IO26	AA17	2
	34	JAE3_OPT_IO27	AB17	2
	35	GND	—	—
	36～45			
	46	GND	—	—
	47	+12V	—	—
	48			
	49			
	50			
	51	+2.5V	—	—
	52			
	53			
	54			
	55	GND	—	—
	56	GND	—	—
	57	JAE3_OPT_IO6	U15(IP)	2
	58	JAE3_OPT_IO7	T15(IP)	2
	59	GND	—	—
	60	JAE3_OPT_IO8	T13(IP)	2
	61	JAE3_OPT_IO9	R13(IP)	2
	62	GND	—	—
	63	JAE3_OPT_IO10	Y11(IP)	2
	64	JAE3_OPT_IO11	AA11(IP)	2
	65	GND	—	—
	66	JAE3_OPT_IO28	V16	2
	67	JAE3_OPT_IO29	U16	2
	68	JAE3_OPT_IO30	Y15	2

.

High Speed Extension I/O pin Assignment Table (continued from previous page)

BD Silk	Connector Pin #	Signal Name	FPGA Pin #	FPGA I/O Bank
CN3	69	JAE3_OPT_IO31	W15	2
	70	GND	—	—
	71	JAE3_OPT_IO32	AA15	2
	72	JAE3_OPT_IO33	AB15	2
	73	JAE3_OPT_IO34	V14	2
	74	JAE3_OPT_IO35	W14	2
	75	GND	—	—
	76	JAE3_OPT_IO36	AA14	2
	77	JAE3_OPT_IO37	Y14	2
	78	JAE3_OPT_IO38	R14	2
	79	JAE3_OPT_IO39	T14	2
	80	GND	—	—
	81	JAE3_OPT_IO40	V11	2
	82	JAE3_OPT_IO41	U11	2
	83			
	84			
	85	GND	—	—
	86～95			
	96	GND	—	—
	97	Option Power	—	—
	98			
	99			
	100			
CN4	1	+3.3V	—	—
	2			
	3			
	4			
	5	GND	—	—
	6	GND	—	—
	7	JAE4_OPT_IO0	U13	2
	8	JAE4_OPT_IO1	U14	2
	9	GND	—	—
	10	JAE4_OPT_IO2	W13	2
	11	JAE4_OPT_IO3	Y13	2
	12	GND	—	—
	13	JAE4_OPT_IO4	P10	2
	14	JAE4_OPT_IO5	R10	2
	15	GND	—	—

High Speed Extension I/O pin Assignment Table (continued from previous page)

BD Silk	Connector Pin #	Signal Name	FPGA Pin #	FPGA I/O Bank
CN4	16	JAE4_OPT_IO12	V9	2
	17	JAE4_OPT_IO13	W9	2
	18	JAE4_OPT_IO14	AA8	2
	19	JAE4_OPT_IO15	AB8	2
	20	GND	—	—
	21	JAE4_OPT_IO16	U8	2
	22	JAE4_OPT_IO17	T8	2
	23	JAE4_OPT_IO18	W8	2
	24	JAE4_OPT_IO19	V8	2
	25	GND	—	—
	26	JAE4_OPT_IO20	V7	2
	27	JAE4_OPT_IO21	U7	2
	28	JAE4_OPT_IO22	Y7	2
	29	JAE4_OPT_IO23	W7	2
	30	GND	—	—
	31	JAE4_OPT_IO24	V6	2
	32	JAE4_OPT_IO25	W6	2
	33	JAE4_OPT_IO26	AB21	2
	34	JAE4_OPT_IO27	AB4	2
	35	GND	—	—
	36～45			
	46	GND	—	—
	47	+12V	—	—
	48			
	49			
	50			
	51	+2.5V	—	—
	52			
	53			
	54			
	55	GND	—	—
	56	GND	—	—
	57	JAE4_OPT_IO6	T10	2
	58	JAE4_OPT_IO7	U10	2
	59	GND	—	—
	60	JAE4_OPT_IO8	AB10	2

High Speed Extension I/O pin Assignment Table (continued from previous page)

BD Silk	Connector Pin #	Signal Name	FPGA Pin #	FPGA I/O Bank
CN4	61	JAE4_OPT_IO9	AB9	2
	62	GND	—	—
	63	JAE4_OPT_IO10	T9	2
	64	JAE4_OPT_IO11	R9	2
	65	GND	—	—
	66	JAE4_OPT_IO28	AB11	2
	67	JAE4_OPT_IO29	AB18	2
	68	JAE4_OPT_IO30	AB16	2
	69	JAE4_OPT_IO31	AB14	2
	70	GND	—	—
	71	JAE4_OPT_IO32	AB13	2
	72	JAE4_OPT_IO33	AB5	2
	73	JAE4_OPT_IO34	AA10	2
	74	JAE4_OPT_IO35	Y9	2
	75	GND	—	—
	76	JAE4_OPT_IO36	Y8	2
	77	JAE4_OPT_IO37	Y19	2
	78	JAE4_OPT_IO38	AB20	2
	79	JAE4_OPT_IO39	AA20	2
	80	GND	—	—
	81	JAE4_OPT_IO40	V12	2
	82	JAE4_OPT_IO41	AA12	2
	83			
	84			
	85	GND	—	—
	86～95			
	96	GND	—	—
	97	Option Power	—	—
	98			
	99			
	100			

Table 10 Option I/O Pin Assignment

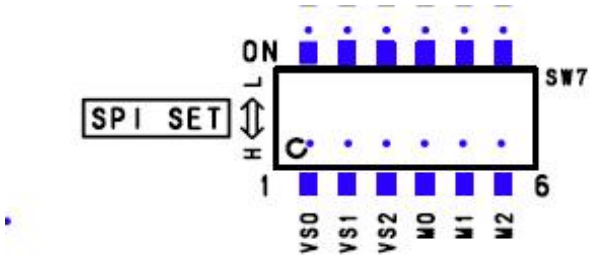
Others

The board provides 12 GND test points (TP16-TP19, TP21-TP27 and TP29). These test points can be used to measure the waveform using an oscilloscope.

Figure.11 GND Test Point

Configuration Mode Selector

The DIP switch at SW7 allows you to select configuration mode. Two configuration modes, Master Serial mode (serial configuration) and SPI mode (serial flash configuration), are available.



Master Serial setting

[M2:M0] = [0:0:0]

SPI setting

[M2:M0] = [0:0:1] [VS2:VS0] = [1:1:1]

Figure.12 Configuration Mode Setting Diagram

9. How to Write into a Device

Overview of Board Configuration Circuit (with PROM)

The following figure shows the board configuration structure.
Downloading can be performed in Master Serial Configuration using either a parallel cable 4(PC4) or 3(PC3).
Note that the XC3S1600E program may require a patch file.
For more information, refer to Xilinx home page, Answer Database 22092.

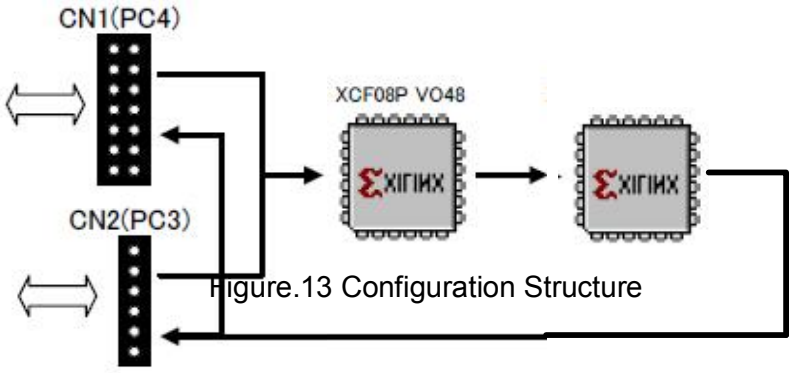


Figure.13 Configuration Structure

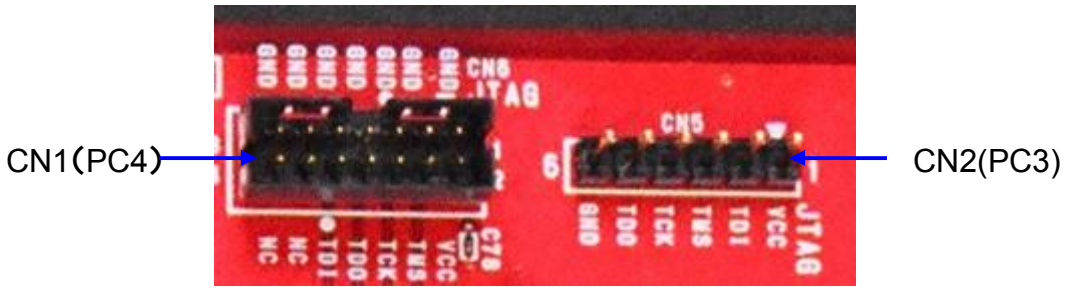


Figure.14 JTAG Connector

Creation of a FPGA Bit Stream File (MSC File)

1) A bit file to be created by Xilinx ISE must have FPGA Start-Up Clock as CCLK.
The following paragraph describes how to create it.

2) On Project, double-click Generate PROM, ACE or JTAG File to start up iMPACT or iMPACT in standalone. See Figure.15.

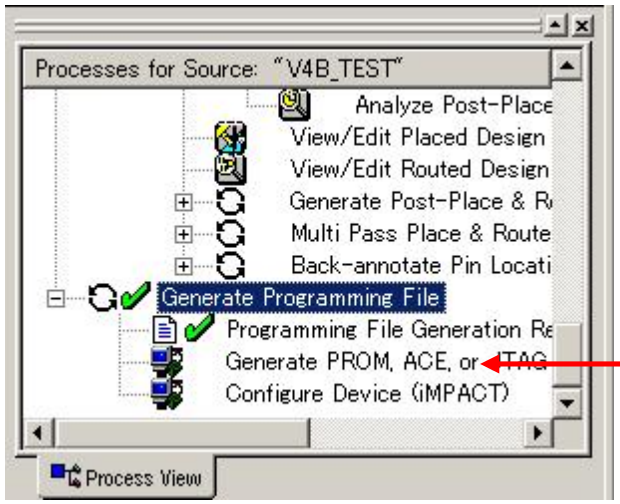


Figure.15

If iMPACT is set to run in standalone mode, select Prepare Configuration File and then click Next. See Figure.16.

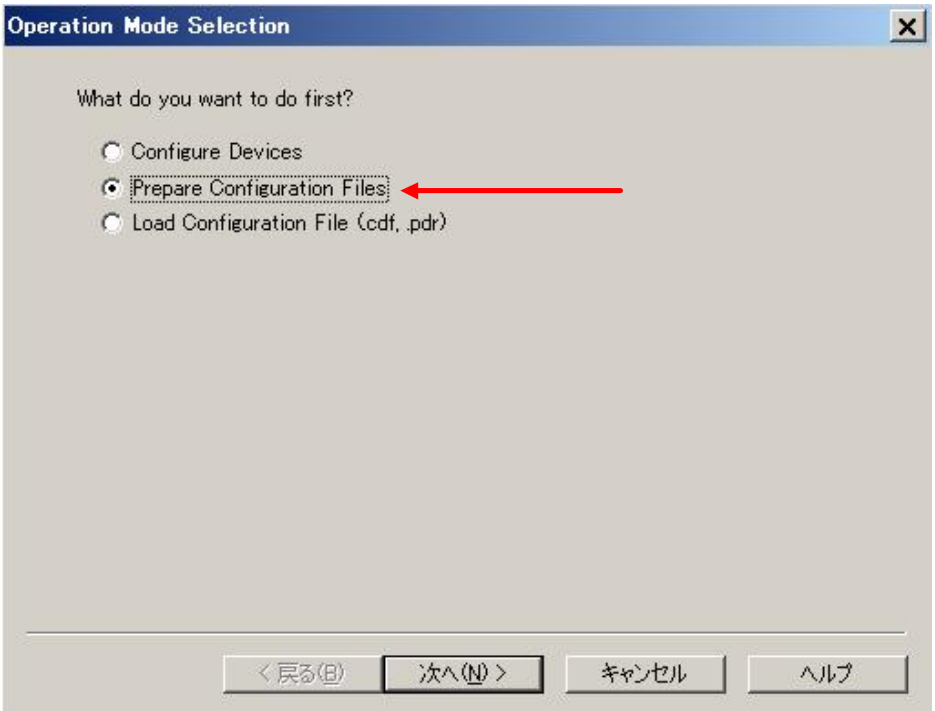


Figure.16

3) Select PROM File and then click Next. See Figure.17

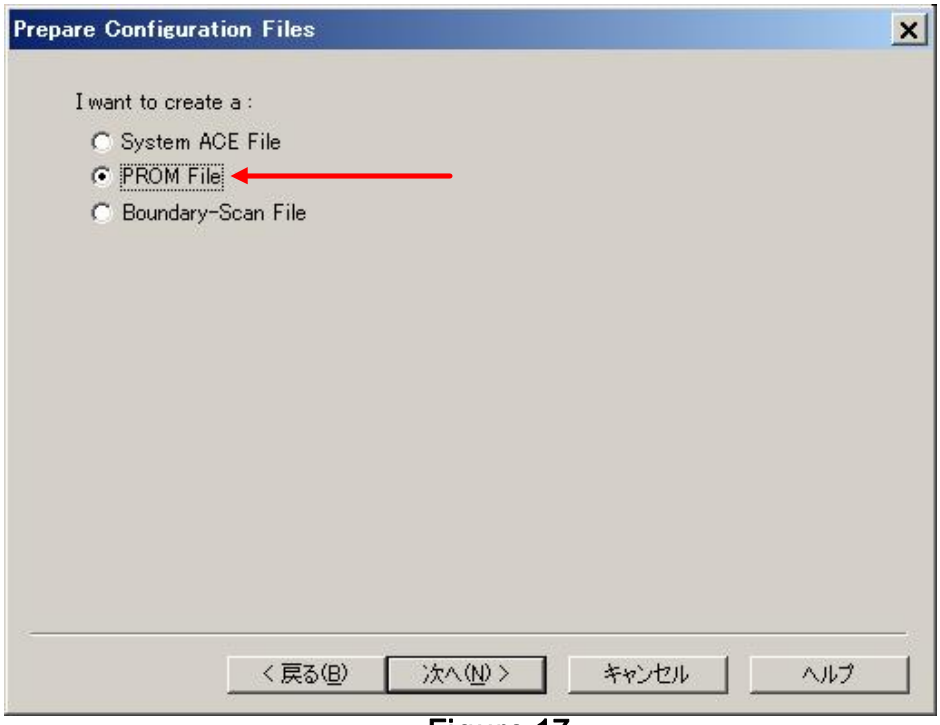


Figure.17

4) On the Prepare PROM Files window, set parameters as shown in Figure.18 and then click Next.

u

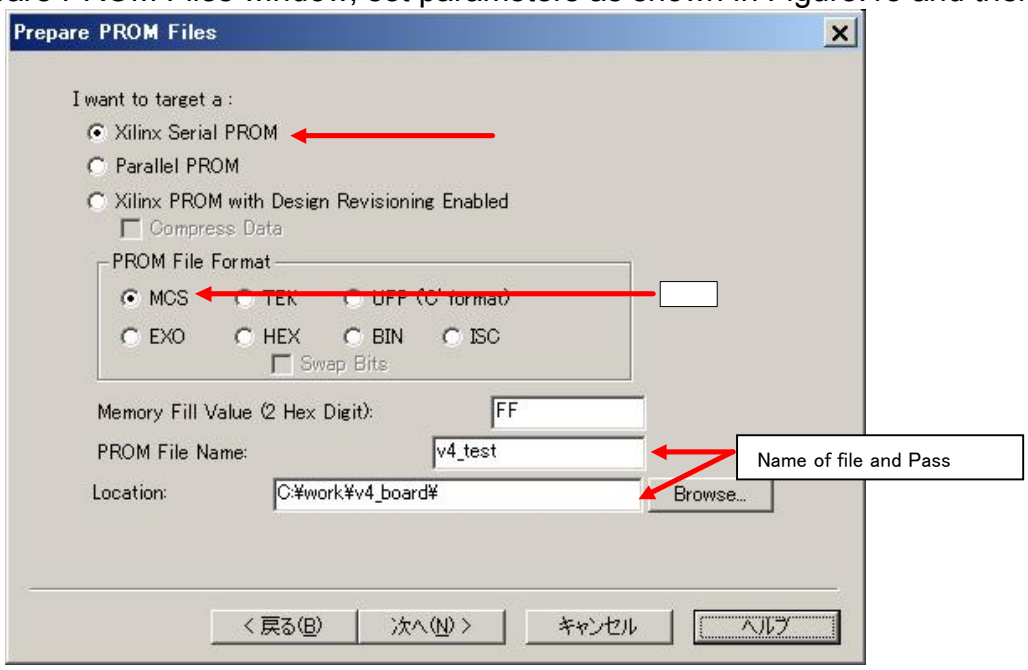


Figure.18

5) On the Specify Xilinx Serial PROM device window, set parameters as shown in Figure.19. For XC3S1600E, select "xcf"→"xcf08p", click the Add button and then Next.

Figure.19

6) Check the contents of the File Generation Summary window (Figure.20) and then click Next.

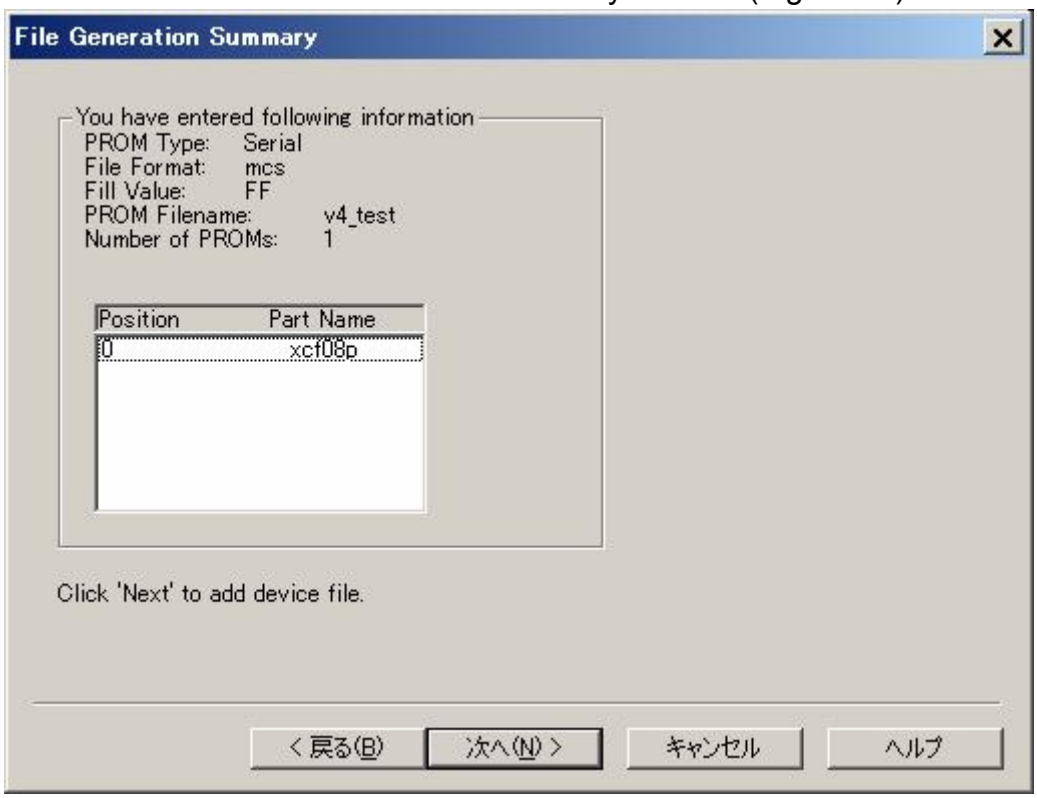


Figure.20

7) On the Add Device File window click on the Add File button (Figure.21).

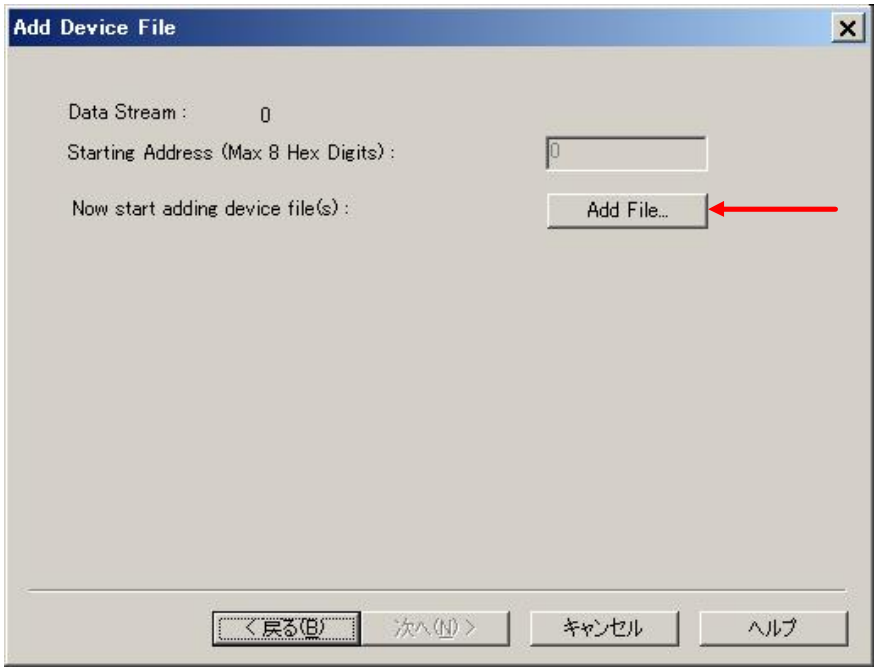


Figure.21

8) Specify a target bit file (Figure.22).

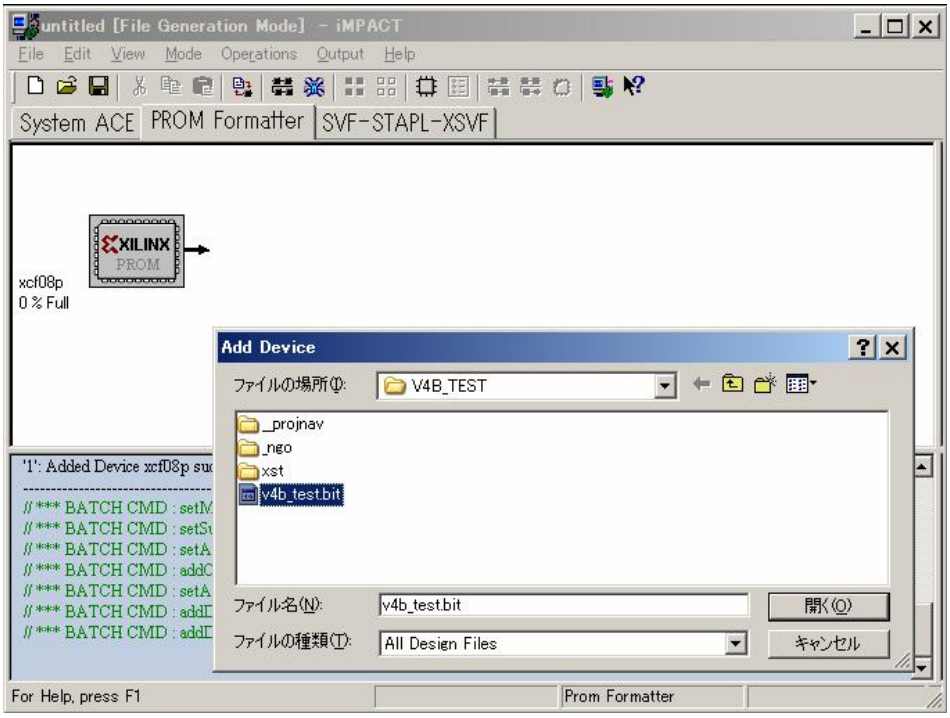


Figure.22

9) Only XC3S1600E exists as FPGA. So, click on the No button (Figure.23).

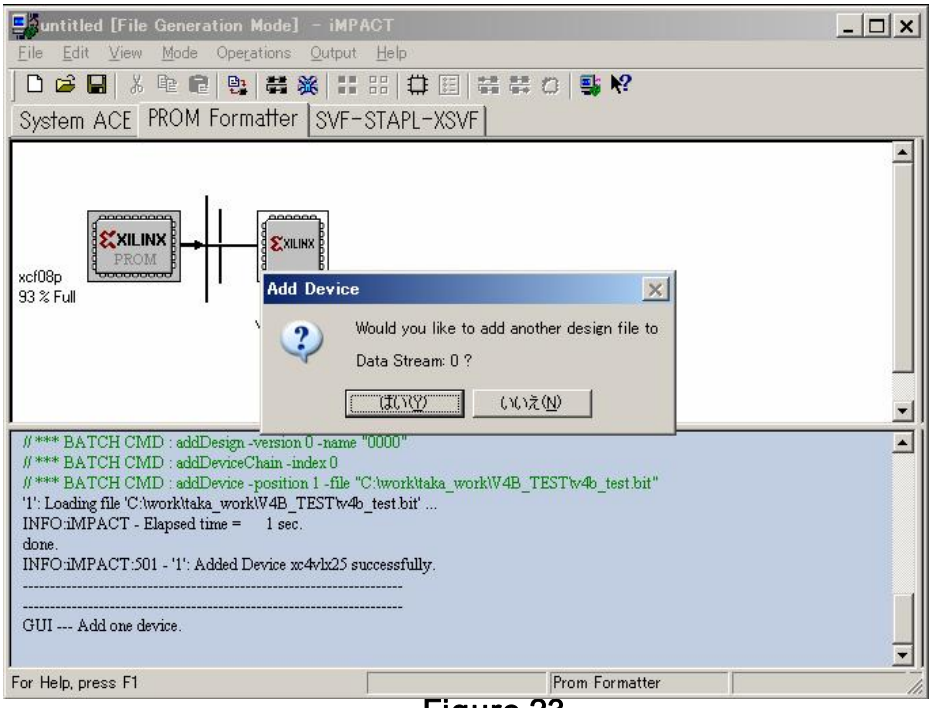


Figure.23

10) A screen as shown in Figure.24 appears. Click on the Complete button.

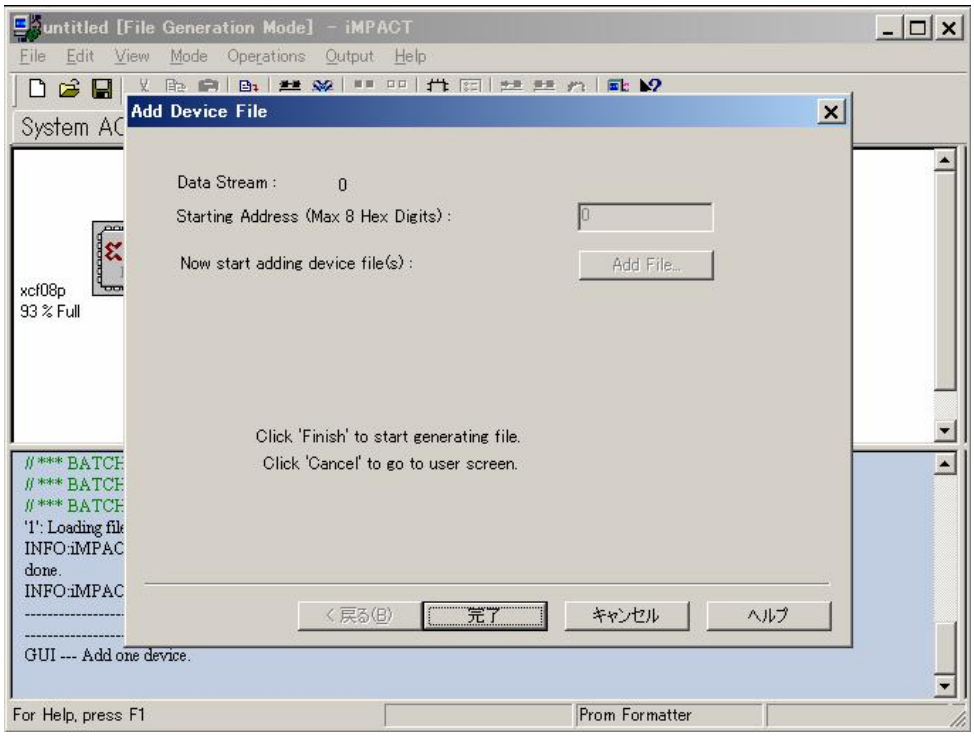


Figure.24

11) A screen as shown in Figure.25 appears. Click on the Yes button.

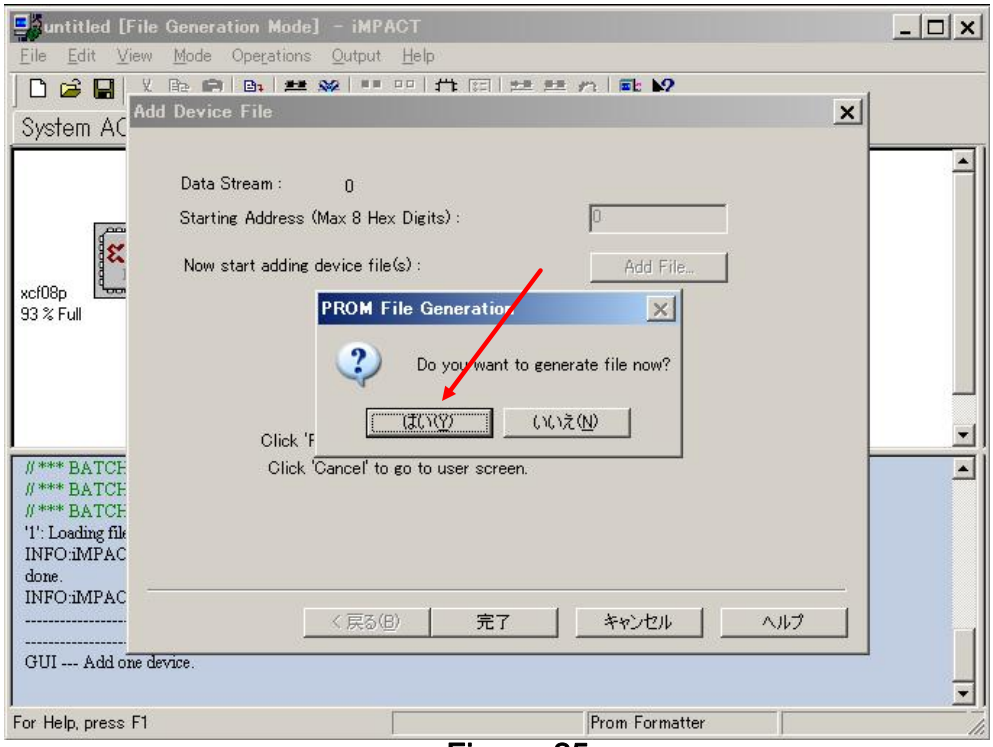


Figure.25

12) When a MCS file is successfully created, a "PROM File Generation Succeeded" character appears as shown in Figure.26.

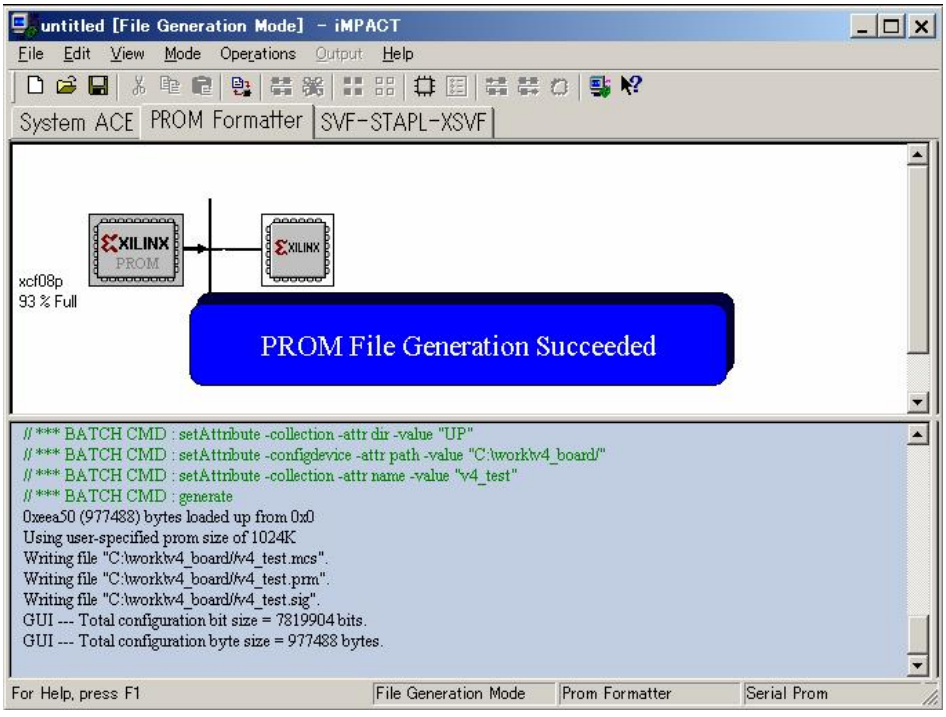


Figure.26

Downloading of a FPGA Bit Stream File (MSC File)

1) **Download a bit stream file (MSC file) to PROM (XCF08P).**
Connect a download cable (PC4 or PC3) and then turn on the power switch of the board. The following describes the download procedure.

2) On Project double-click Configure Device (iMPACT) to run iMPACT or run it in standalone mode (Figure.27).

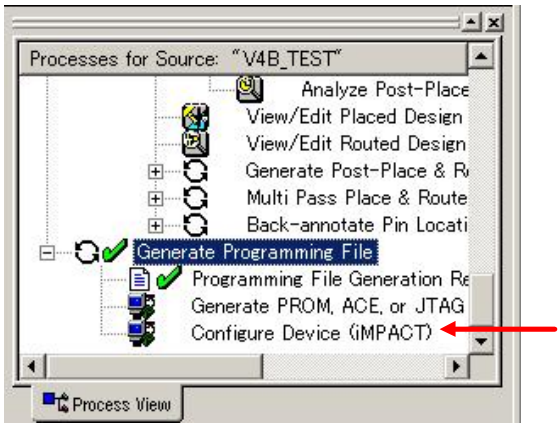


Figure.27

If iMPACT is set to run in standalone mode, select Configure Devices File and then click Next (Figure.28).

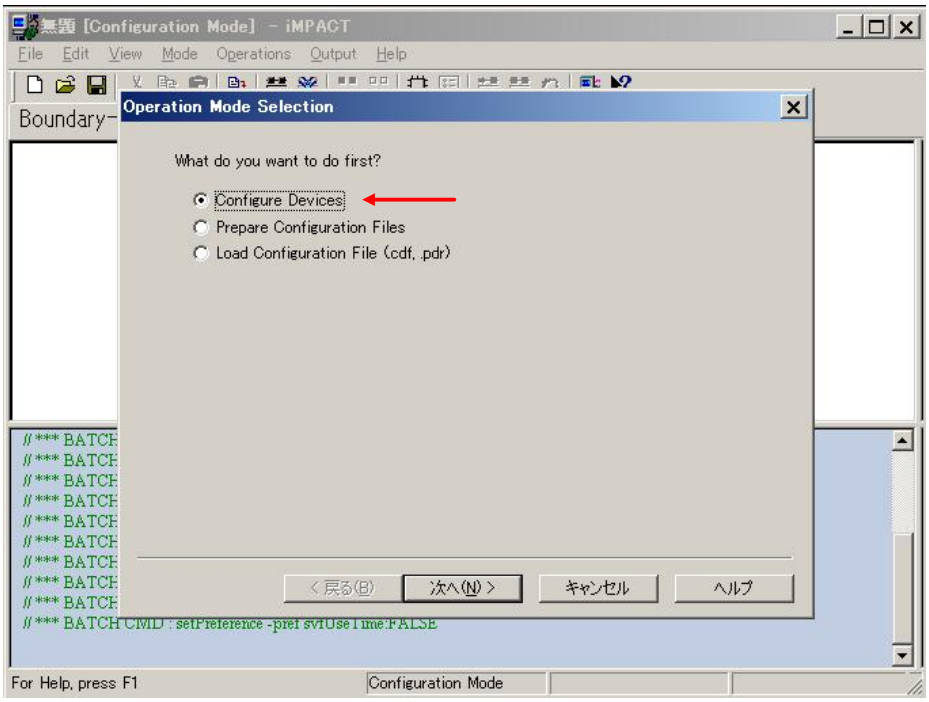


Figure.28

3) On Configure Devices select Boundary-Scan Mode and then click Next (Figure.29).

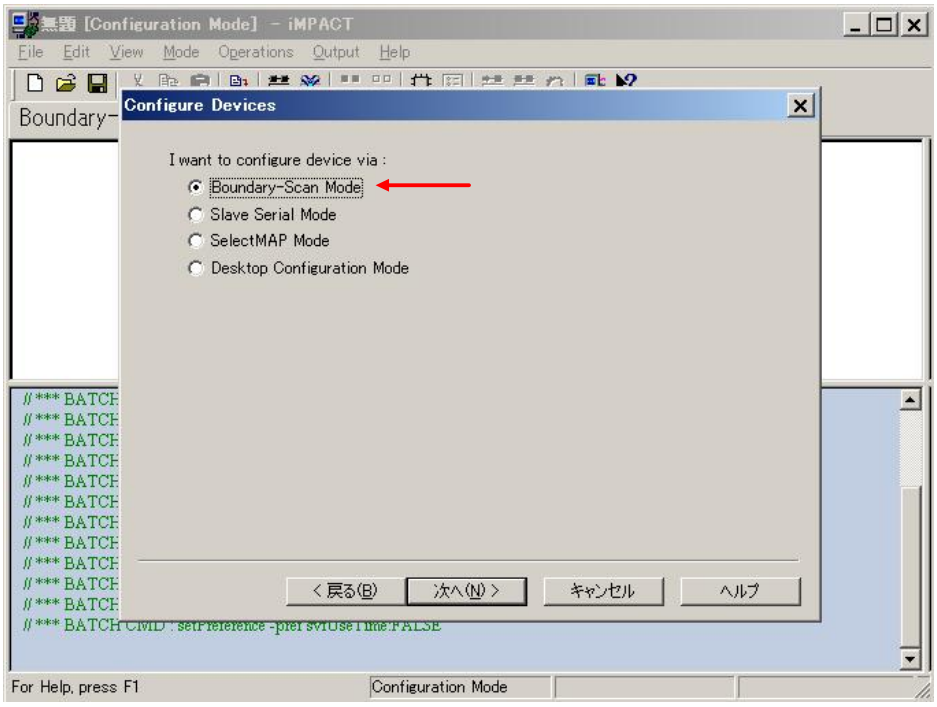


Figure.29

4) On Boundary-Scan Mode Selection select Automatically Connect to Cable and Identify Boundary-Scan Chain and then click Complete. Onboard JTAG chains are retrieved (Figure.30).

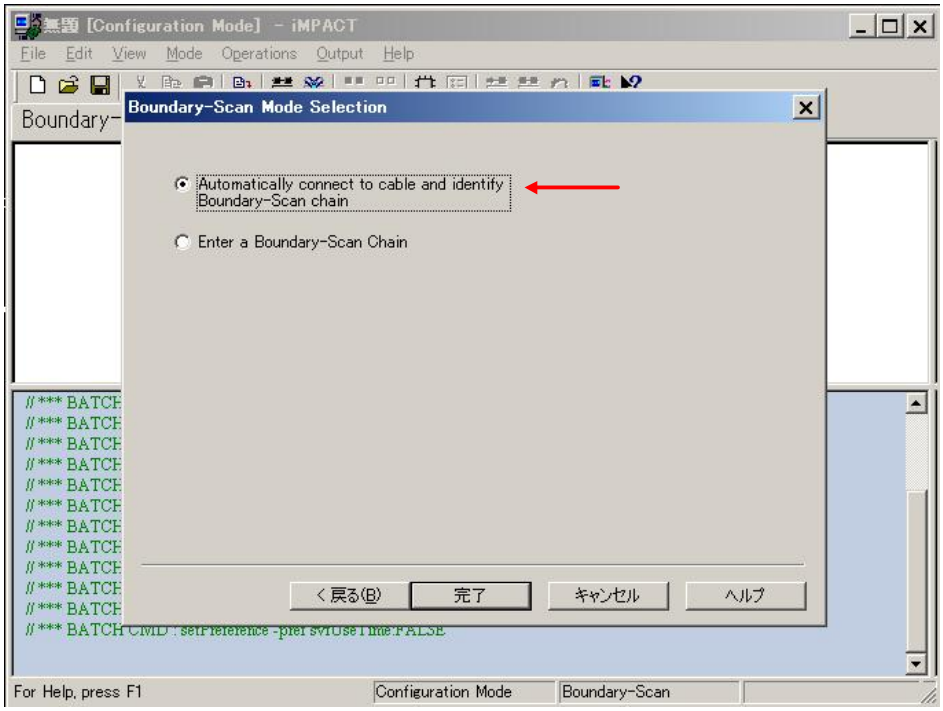


Figure.30

5) Detected devices are shown on the iMPACT window.
The board displays two devices, XCF08P(PROM) and XC3S1600E0(FPGA) as shown in Figure.31 (if FPGA is shown as UNKNOWN, refer to the Answer Database 22092). Click on the OK button on Boundary-Scan Chain Contents Summary.

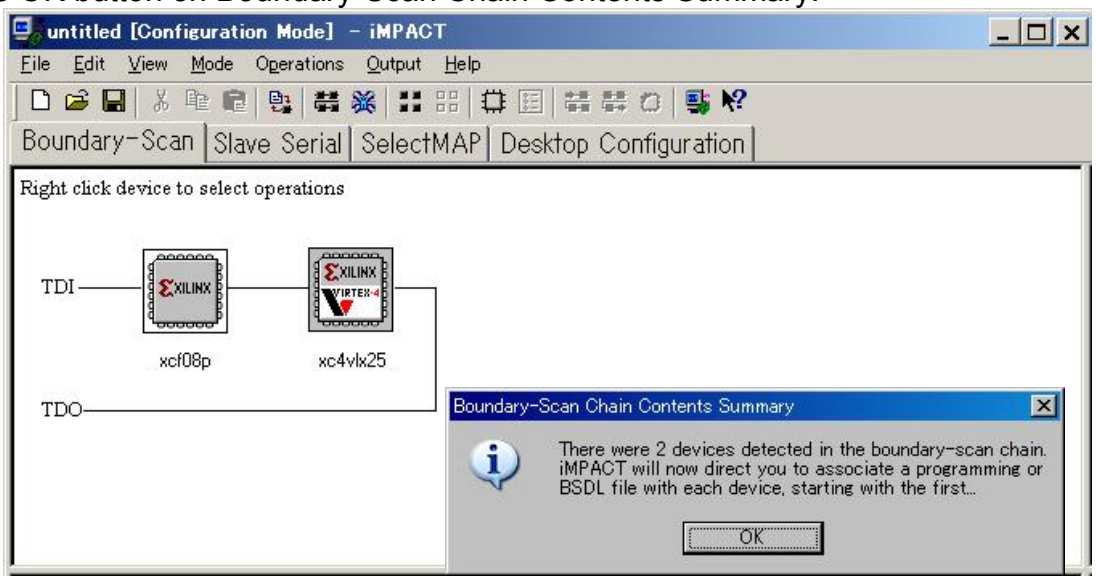


Figure.31

6) Double-click XCF08P(PROM) and then specify a bit stream file (MSC file) to be downloaded. Figure.32 shows the window after the file has been specified.

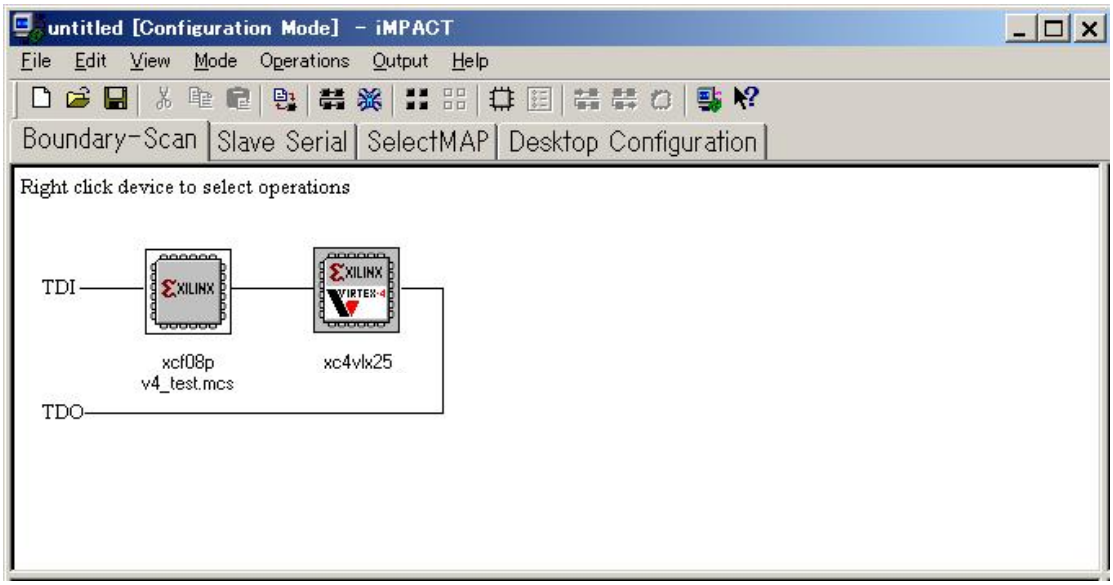


Figure.32

7) After selecting XCF08P(PROM) (it turns red), right-click to select Program… (Figure.33).

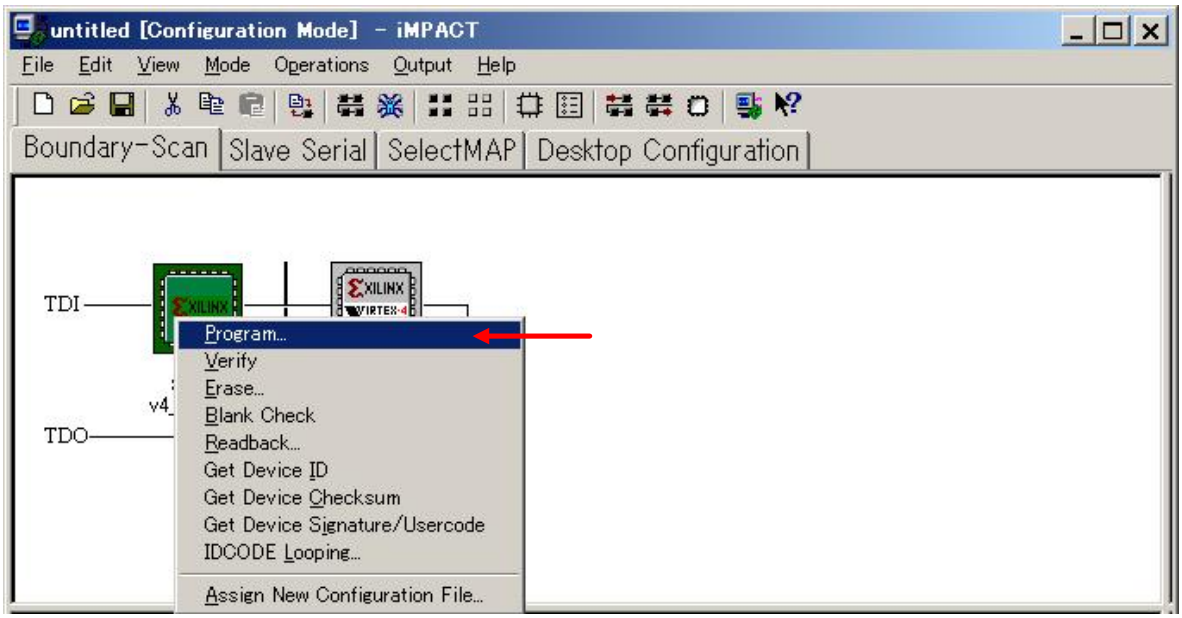


Figure.33

8) Clear the check box for **Verify** and then click on the OK button.
The board starts the downloading to XCF08P (PROM). See Figure.34.

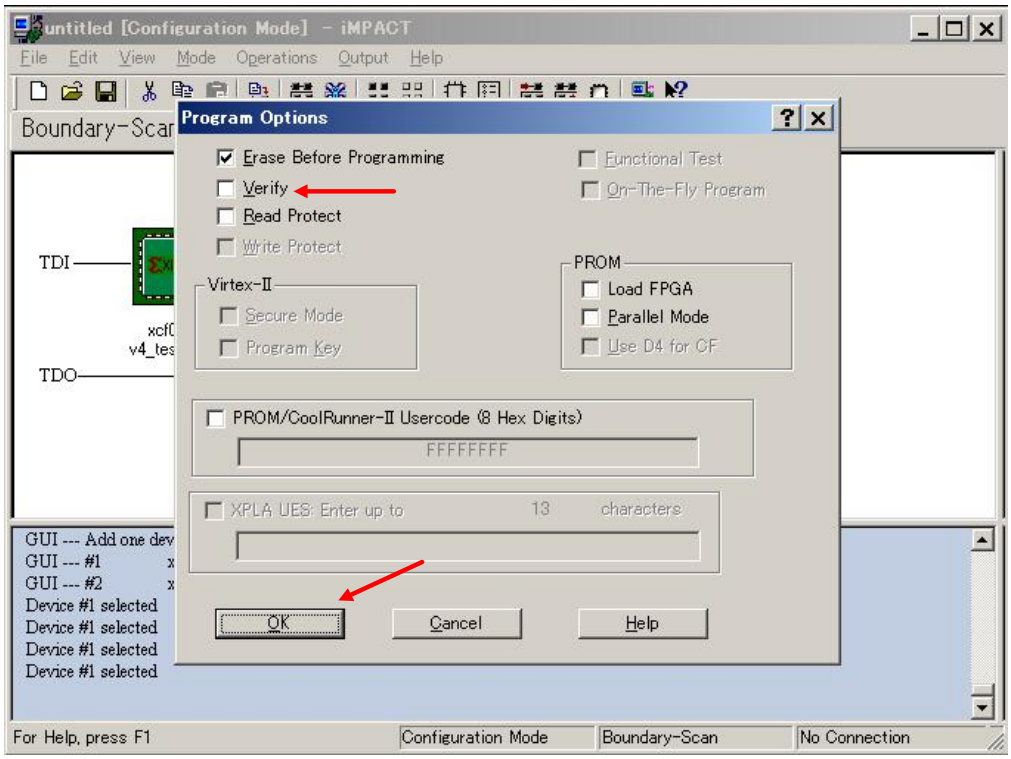


Figure.34

9) If the downloading is successfully complete, Programming Succeeded appears on the window. See Figure.35.

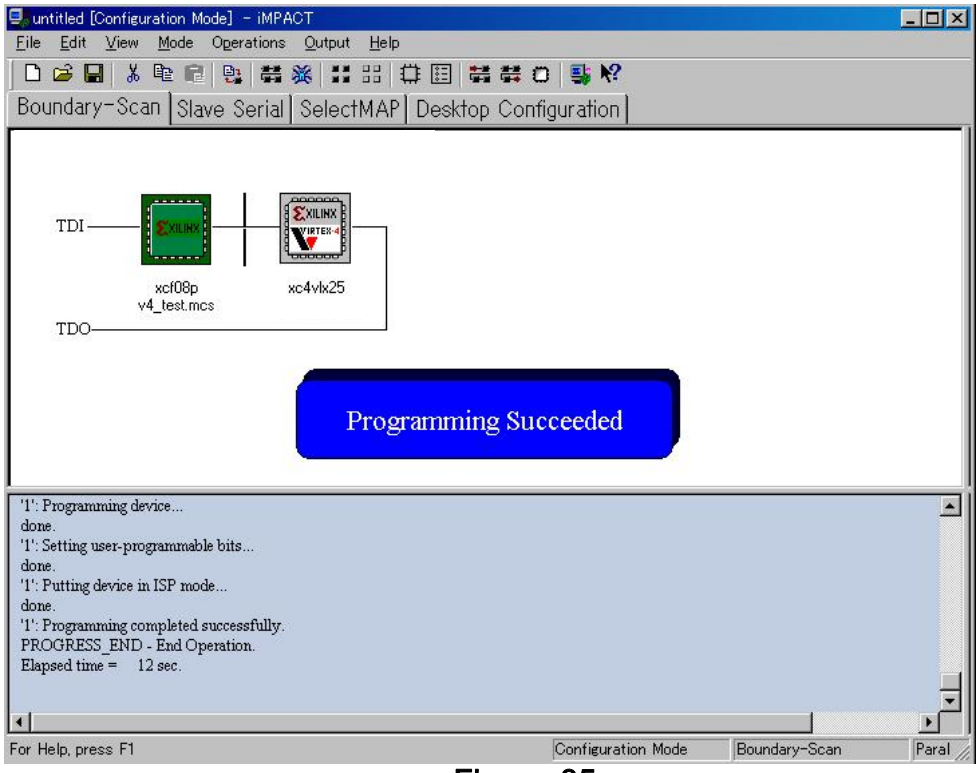
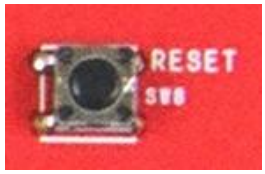


Figure.35

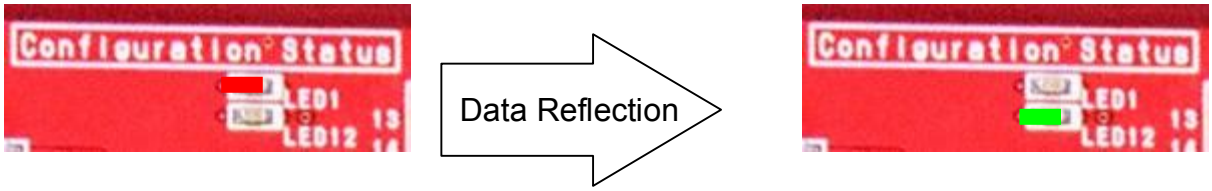
Turn off and on the board power switch or hold down the onboard reset switch (SW8) for over three seconds to relect the downloaded data to FPGA.



RESET Switch

Figure.36 Reset Switch

When the downloaded data has been reflected to FPGA, DONE LED turns from red to green.



Power off and on or hold down Reset Switch

Configuration is completed.

Figure.37 DONE LED

Revision History

2005/12/26 Rev0.0 Preliminary Version
2006/01/11 Rev1.0 Release Version
2006/02/26 Rev1.1 Pin number changed

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