

HD151011

Dual BCD Programmable Counter with Synchronous Preset Enable

REJ03D0298-0200Z
(Previous ADE-205-100 (Z))
Rev.2.00
Jul.16.2004

Description

The HD151011 has BCD decimal two digits down counter and D-type Flip Flop. The counter can set up to max 99 counts and synchronous preset ($\overline{\text{SPE}}$) input can preset the data. When the count value is 0, the next clock pulse presets the data to invert the output. D-type Flip Flop takes the counter output as clock pulse, whose data is transferred to output at the rise edge. It is applied to generate AC signal for STN type liquid crystal and general-use divider.

Features

- High speed operation
tpd (CLK or $\overline{\text{CLK}}$ to Q) = 35 ns (typ)
- High output current
Fanout of 10 LS TTL Loads
- Wide operating voltage
 $V_{\text{CC}} = 2$ to 6 V
- Low supply current ($T_a = 25^\circ\text{C}$)
 I_{CC} (Static) = 4 μA (max)

- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD151011FPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD151011TELL	TSSOP-20 pin	TTP-20DAV	T	ELL (2,000 pcs/reel)

Note: Please consults the sales office for the above package availability.

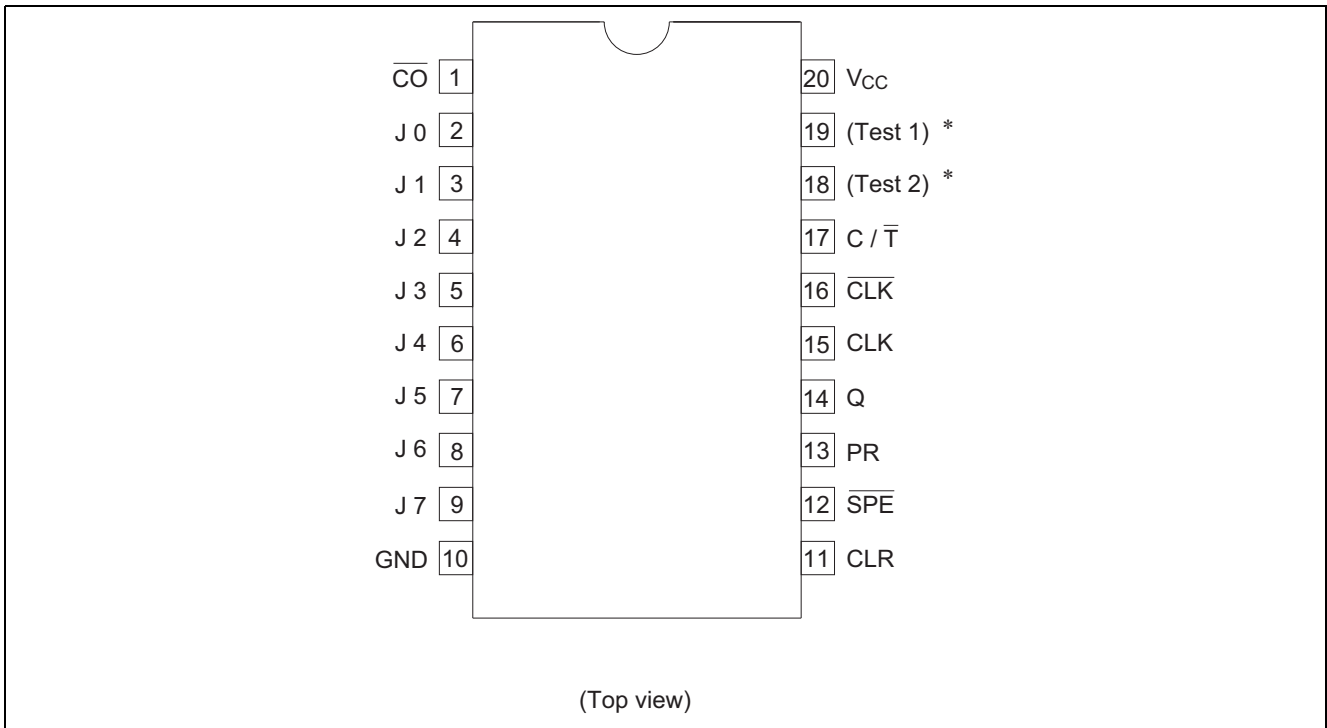
Function Table

Control Inputs				Mode	Operation Description
CLR	PR	SPE	C/T		
H	H	H	X	Generally count	Down count at the rise edge of clock (CLK) Down count at the fall edge of clock ($\overline{\text{CLK}}$)
X	X	L	X	Synchronous preset	Jn data is preset at the rise of clock (CLK), the fall of clock ($\overline{\text{CLK}}$)
—	—	—	H	—	Clock inputs (CLK, $\overline{\text{CLK}}$) is CMOS level
—	—	—	L	—	Clock inputs (CLK, $\overline{\text{CLK}}$) is TTL level
L	H	—	—	Initialize of Q output	Initialize of Q = "L"
H	L	—	—	Initialize of Q output	Initialize of Q = "H"

Note: 1. Synchronous preset ($\overline{\text{SPE}}$) input can set max 99 down counts.
 2. When the count value is 0, the next clock pulse presets the data to invert the output.
 3. CLR and PR inputs initialize output state.
 4. Clock inputs (CLK, $\overline{\text{CLK}}$) is selectable CMOS level ($V_{\text{CC}} = 2.0$ to 6.0 V) and TTL level ($V_{\text{CC}} = 4.5$ to 5.5V) (Jn, C/T, PR, CLR and SPE inputs are CMOS level)
 Don't set data exceeding 99 to Jn. (J0 : LSB, J7 : MSB)

H : High level
 L : Low level
 X : Immaterial
 — : Irrespective of condition

Pin Arrangement



Pin Description

Pin Name		Pin Description	
Input pins	J0 to J7	Count data input for option	
	$\overline{C/T}$	Level change input for CLK, \overline{CLK} (CMOS level or TTL level)	
	CLK, \overline{CLK}	Clock inputs	CLK : Rise edge trigger \overline{CLK} : Fall edge trigger
	SPE	Preset input for Jn data	
	PR	Preset input for D-type Flip Flop (Initialize "L" at Q output)	
	CLR	Clear input for D-type Flip Flop (Initialize "H" at Q output)	
Output pins	\overline{CO}	Output for BCD decimal counter	
	Q	Output for D-type Flip Flop	

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input/output voltage	V_{IN}/V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
V_{CC} , GND current	I_{CC}, I_{GND}	± 50	mA
Output current/pin	I_{OUT}	± 25	mA
Power dissipation	P_T	757	mW
Storage temperature	Tstg	-65 to 150	°C
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 20	mA

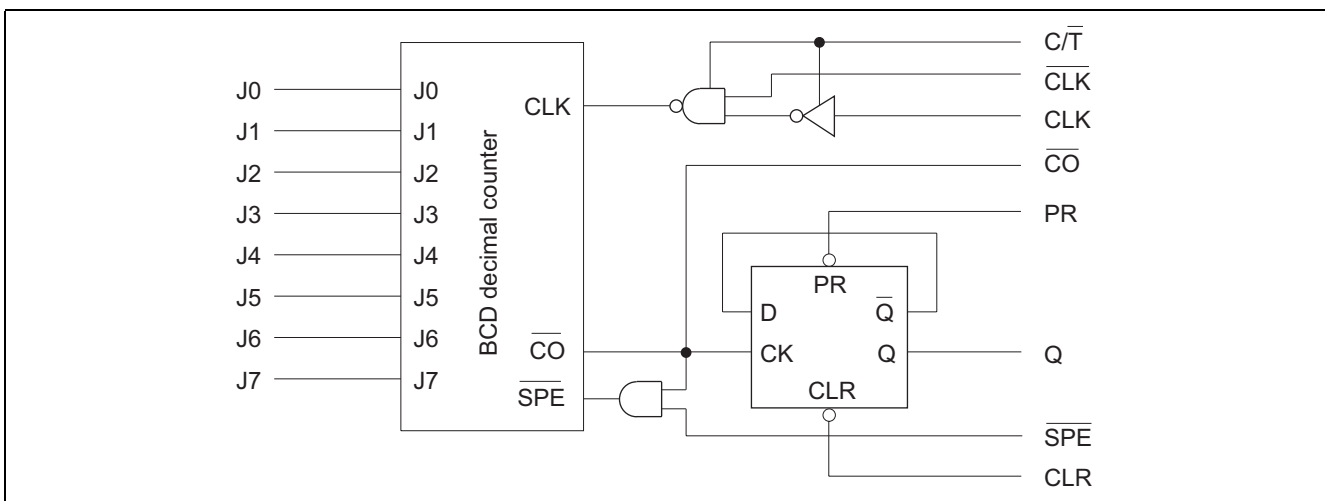
- Notes: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.
2. All voltage values except for differential input voltage are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	
Supply voltage	V_{CC}	2	—	6	V	
Input/output voltage	V_{IN}/V_{OUT}	0	—	V_{CC}	V	
Operating temperature	T_{opr}	-40	—	+85	°C	
Input rise/fall time*1	$V_{CC} = 2.5\text{ V}$	t_r, t_f	0	—	1000	ns
	$V_{CC} = 4.5\text{ V}$		0	—	500	
	$V_{CC} = 5.5\text{ V}$		0	—	400	

- Note: 1. This item guarantees maximum limit when one input switches.

Logic Diagram



Electrical Characteristics

Item	Sym- bol	V _{CC}	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions				
			Min	Typ	Max	Min	Max						
High level input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V	J0 to J7 C/T, $\overline{\text{SPE}}$ PR, CLR				
		4.5	3.15	—	—	3.15	—						
		6.0	4.2	—	—	4.2	—						
				2.0	1.5	—	—		1.5	—		CLK, CLK	C/T = V _{IH}
				4.5	3.15	—	—		3.15	—			
				6.0	4.2	—	—		4.2	—			
				4.5 to 5.5	2.0	—	—		2.0	—		C/T = V _{IL}	
Low level input voltage	V _{IL}	2.0	—	—	0.5	—	0.5	V	J0 to J7 C/T, $\overline{\text{SPE}}$ PR, CLR				
		4.5	—	—	1.35	—	1.35						
		6.0	—	—	1.8	—	1.8						
				2.0	—	—	0.5		—	0.5		CLK, CLK	C/T = V _{IH}
				4.5	—	—	1.35		—	1.35			
				6.0	—	—	1.8		—	1.8			
				4.5 to 5.5	—	—	0.8		—	0.8		C/T = V _{IL}	
High level output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -20 mA			
		4.5	4.4	4.5	—	4.4	—						
		6.0	5.9	6.0	—	5.9	—						
		4.5	4.18	4.31	—	4.13	—			I _{OH} = -4 mA			
		6.0	5.68	5.80	—	5.63	—			I _{OH} = -5.2 mA			
Low level output voltage	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20 mA			
		4.5	—	0.0	0.1	—	0.1						
		6.0	—	0.0	0.1	—	0.1						
		4.5	—	0.17	0.26	—	0.33			I _{OL} = 4 mA			
		6.0	—	0.18	0.26	—	0.33			I _{OL} = 5.2 mA			
Input capacitance	I _{IN}	6.0	—	—	±0.1	—	±1.0	μA	V _{IN} = V _{CC} or GND				
Supply current	I _{CC}	6.0	—	—	4.0	—	40.0	μA	V _{IN} = V _{CC} or GND				

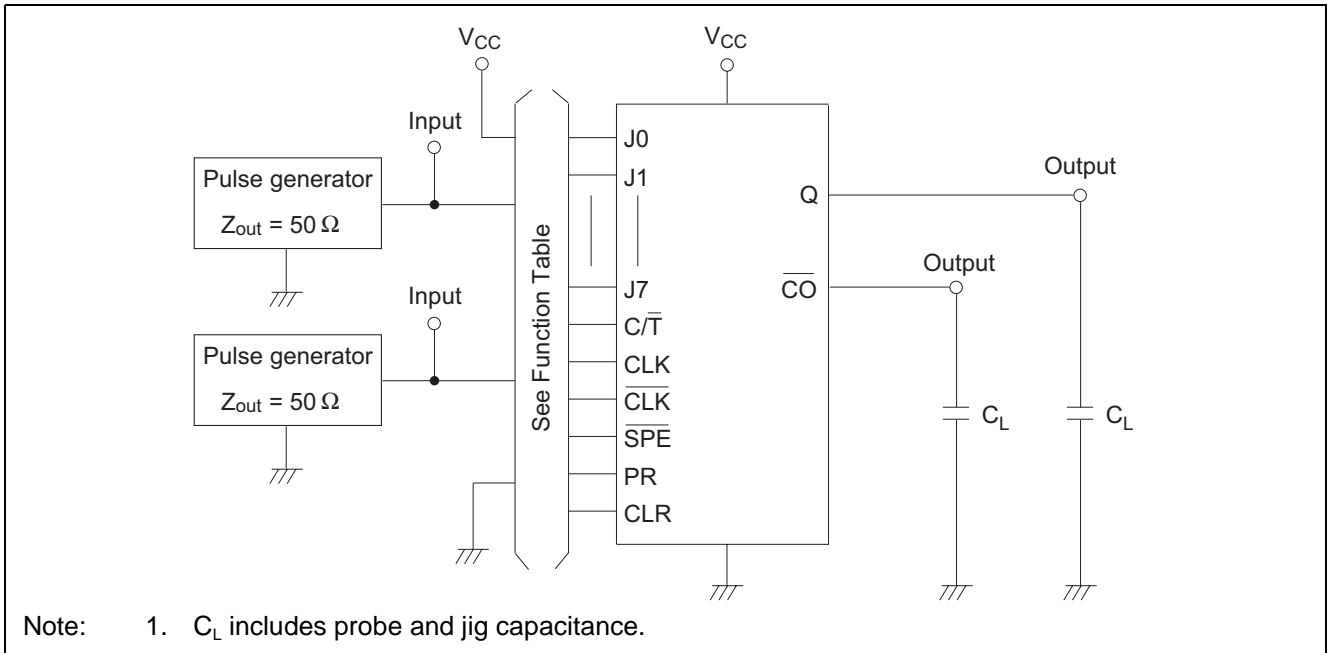
Switching Characteristics ($C_L = 50 \text{ pF}$, $t_r = t_f = 6 \text{ ns}$)

Item	Sym- bol	V_{CC}	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	4	—	3	MHz	
		4.5	—	36	20	—	16		
		6.0	—	—	24	—	19		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	30	75	—	95	ns	
		4.5	—	8	15	—	19		
		6.0	—	7	13	—	16		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	250	—	318	ns	CLK or $\overline{\text{CLK}}$ to $\overline{\text{CO}}$
		4.5	—	30	50	—	63		CLK or $\overline{\text{CLK}}$ to Q
		6.0	—	—	45	—	53		
	t_{PLH} t_{PHL}	2.0	—	—	300	—	380	ns	PR or $\overline{\text{CLK}}$ to Q
		4.5	—	35	60	—	75		
		6.0	—	—	53	—	65		
	t_{PLH} t_{PHL}	2.0	—	—	150	—	185	ns	
		4.5	—	18	30	—	38		
		6.0	—	—	25	—	32		
Pulse width (CLK, $\overline{\text{CLK}}$, PR, CLR)	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time (J_n - CLK, CLK) (SPE, CLK, CLK)	t_s	2.0	100	—	—	125	—	ns	
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time (J_n - CLK, CLK) (SPE, CLK, CLK)	t_h	2.0	15	—	—	15	—	ns	
		4.5	10	—	—	10	—		
		6.0	5	—	—	5	—		
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance*1	C_{PD}	—	—	48	—	—	—	pF	

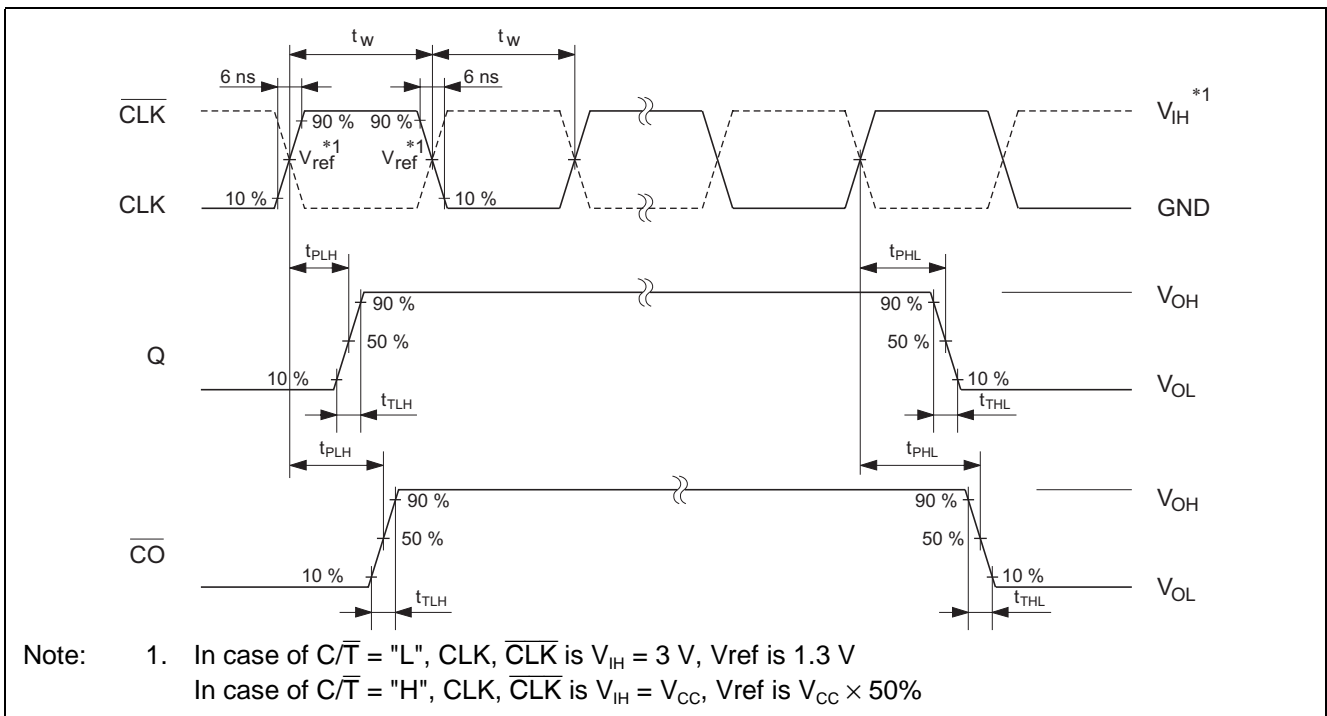
Note: 1. CPD is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

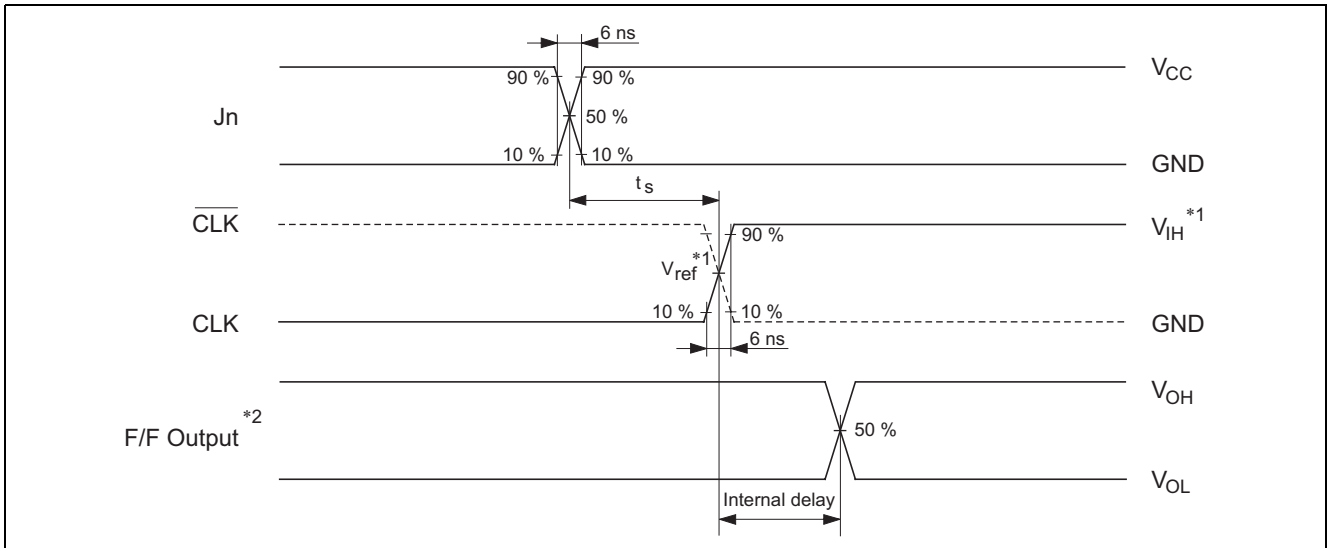
Test Circuit



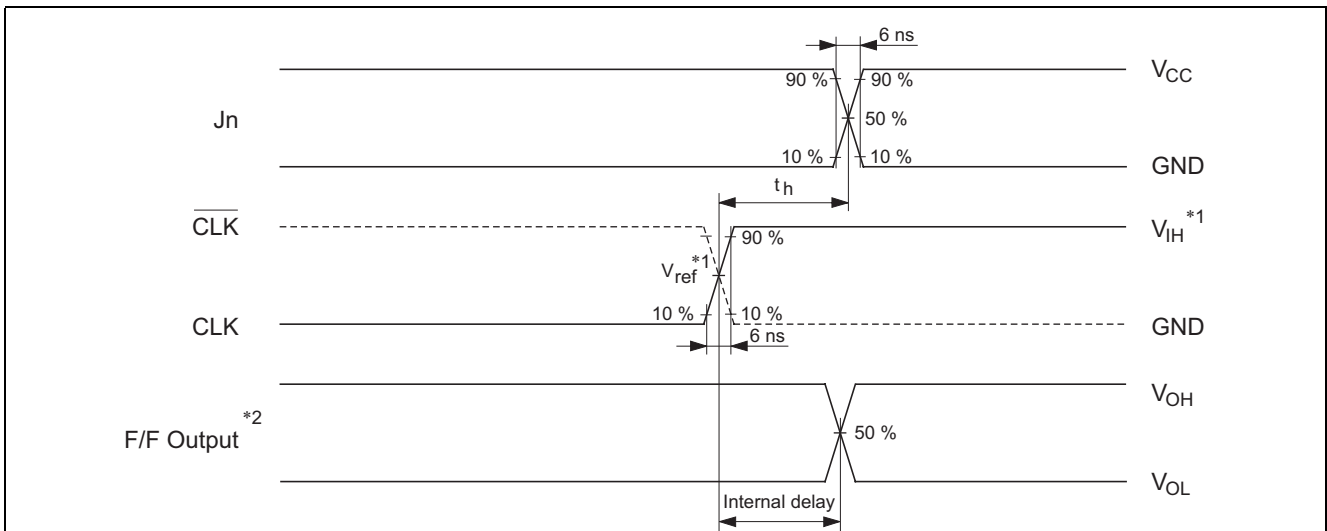
Waveforms – 1



Waveforms – 2

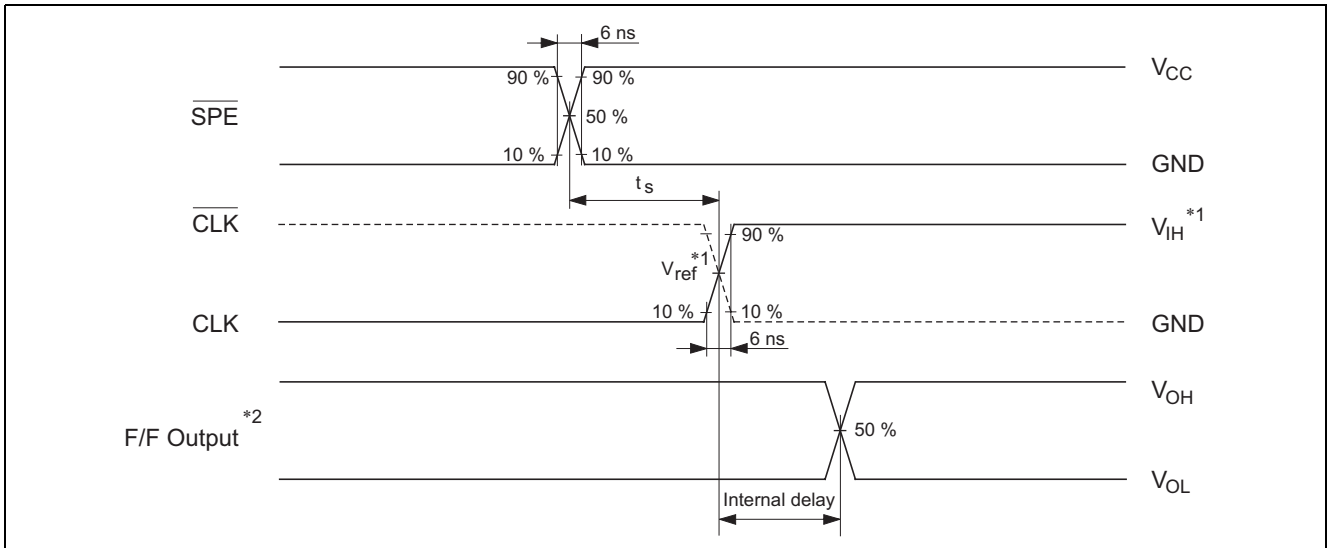


Waveforms – 3

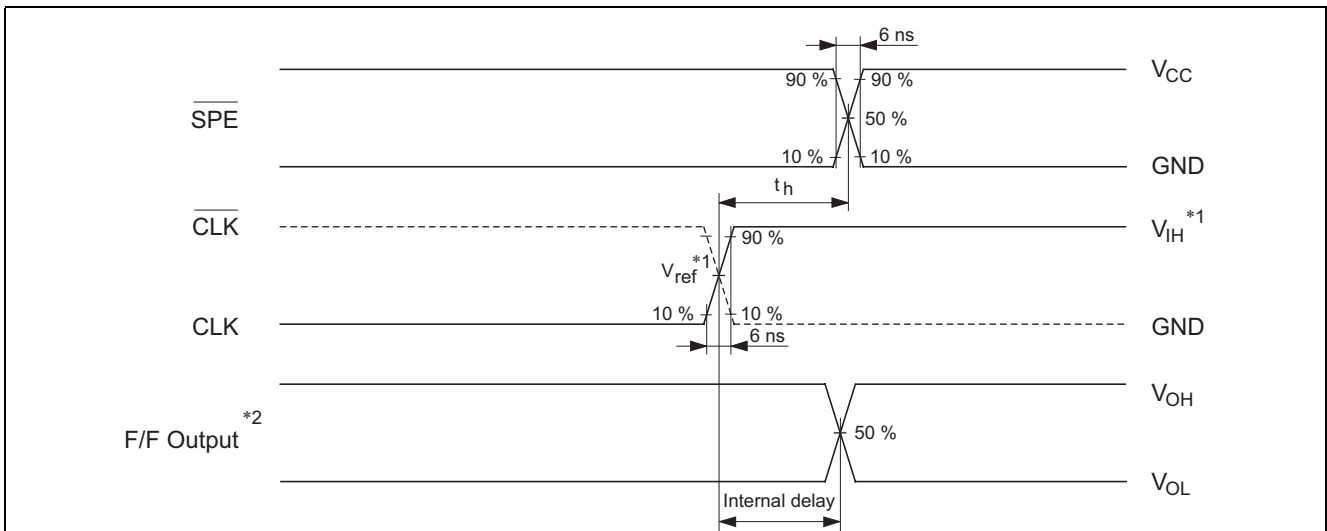


- Notes:
1. In case of $C/\bar{T} = "L"$, CLK, \overline{CLK} is $V_{IH} = 3\text{ V}$, V_{ref} is 1.3 V
 In case of $C/\bar{T} = "H"$, CLK, \overline{CLK} is $V_{IH} = V_{CC}$, V_{ref} is $V_{CC} \times 50\%$
 2. F/F output is internal signal of IC.

Waveforms – 4

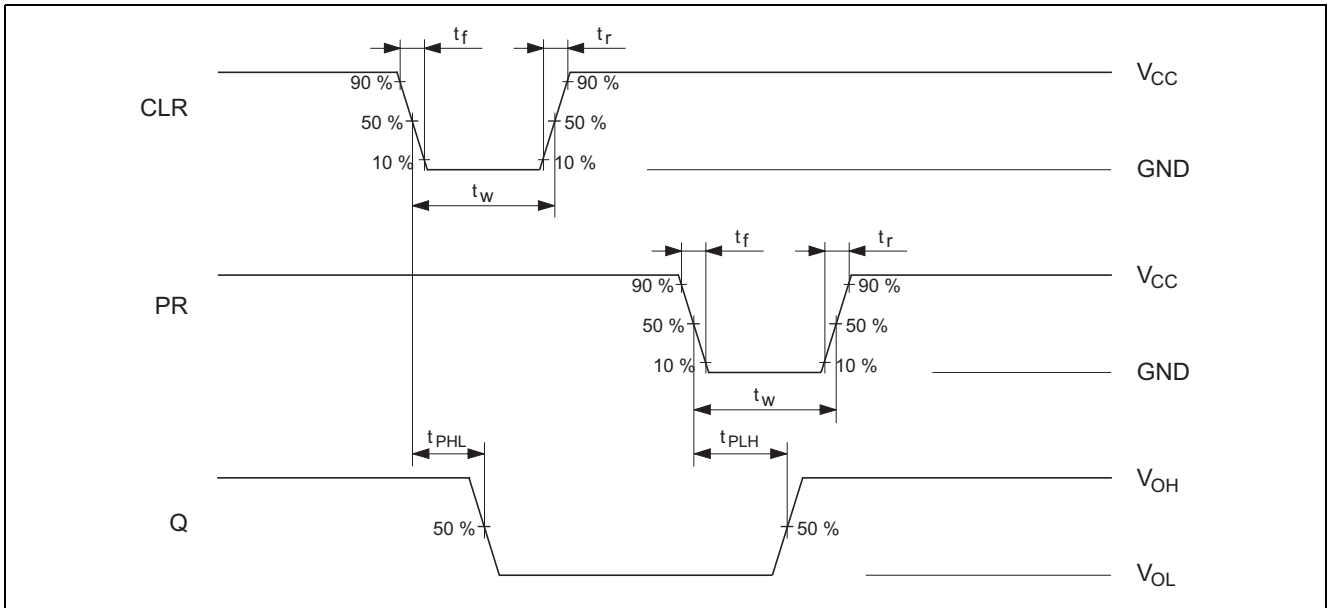


Waveforms – 5

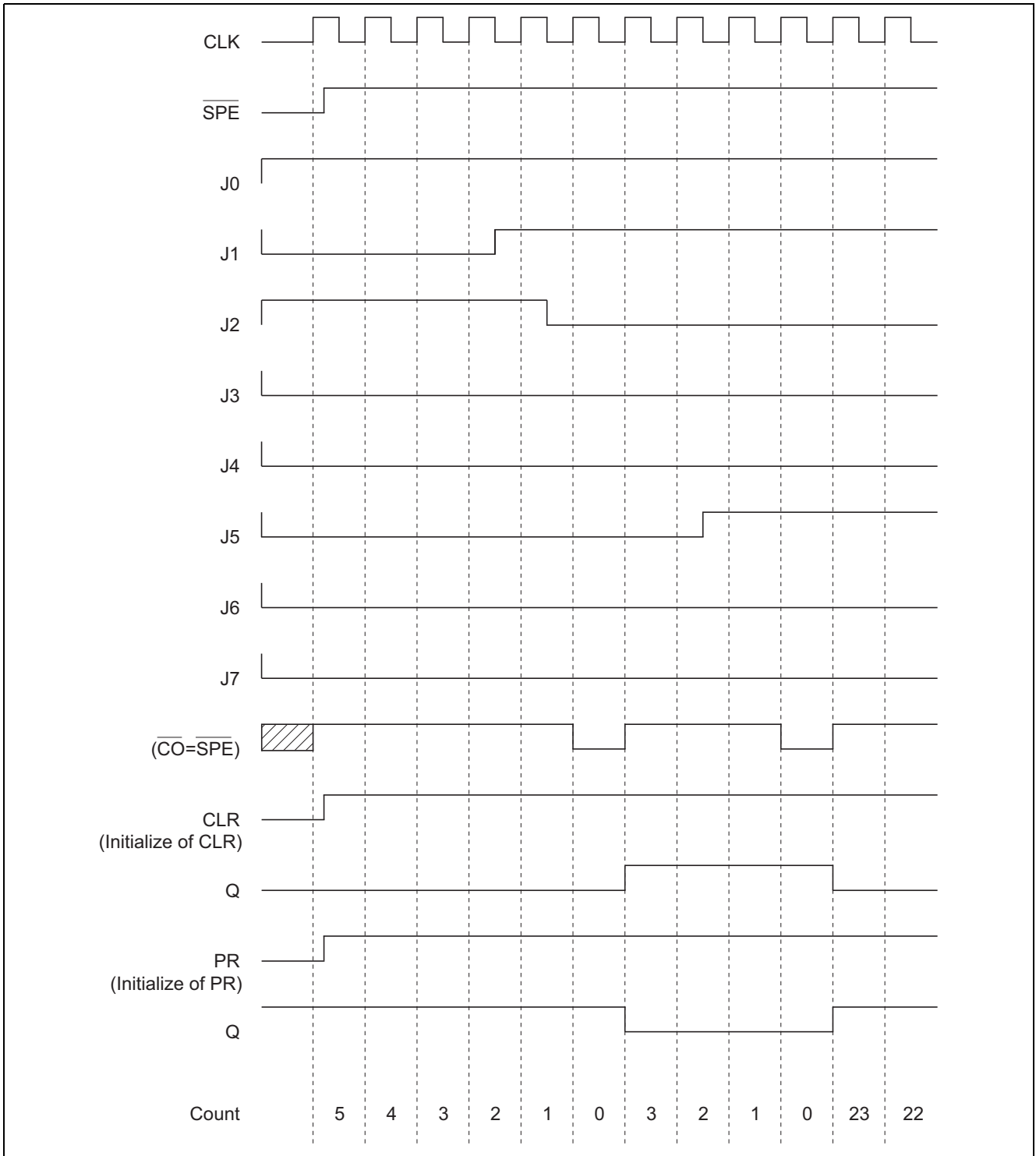


- Notes:
1. In case of $C/\overline{T} = "L"$, CLK , $\overline{\text{CLK}}$ is $V_{IH} = 3 \text{ V}$, V_{ref} is 1.3 V
 In case of $C/\overline{T} = "H"$, CLK , $\overline{\text{CLK}}$ is $V_{IH} = V_{CC}$, V_{ref} is $V_{CC} \times 50\%$
 2. F/F output is internal signal of IC.

Waveforms – 6



Timing Chart

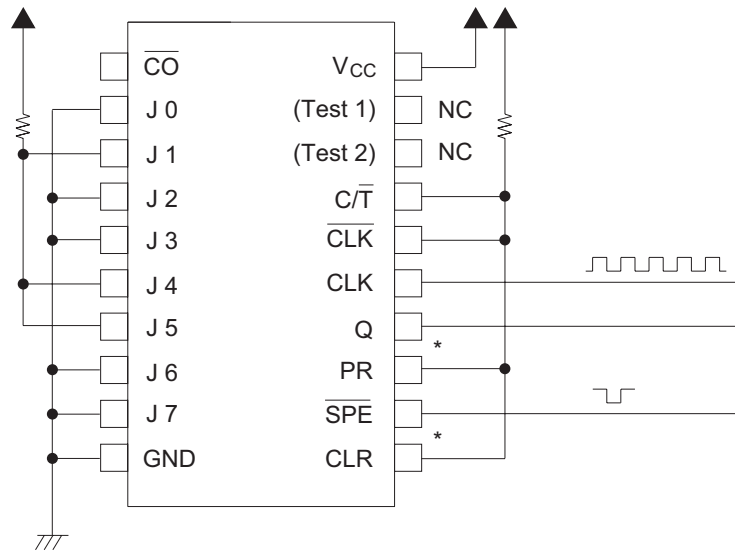


Example of Application Circuit

AC Signal Generator for STN Type Liquid Crystal Panel

CLK ($\overline{\text{CLK}}$) : CMOS level input

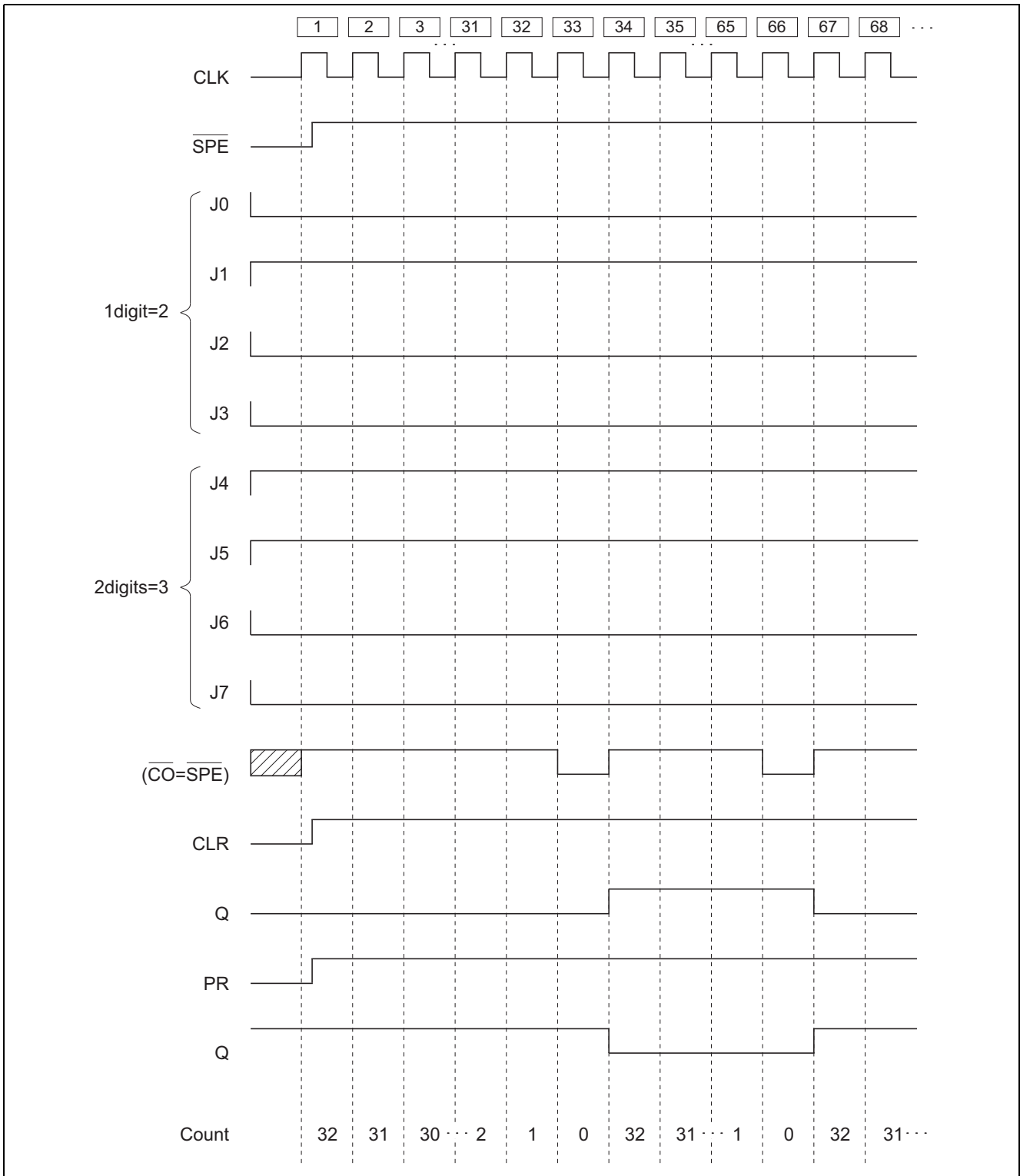
Initialize counter : 32



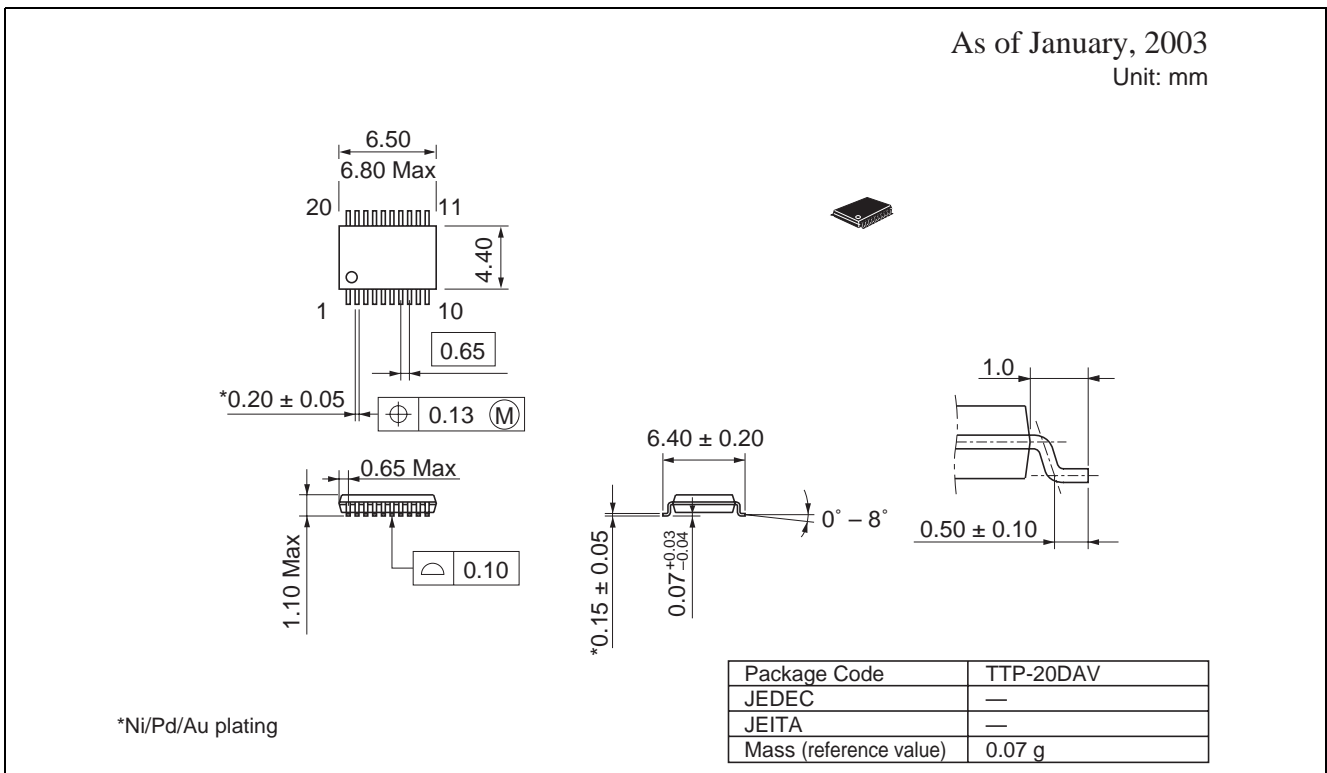
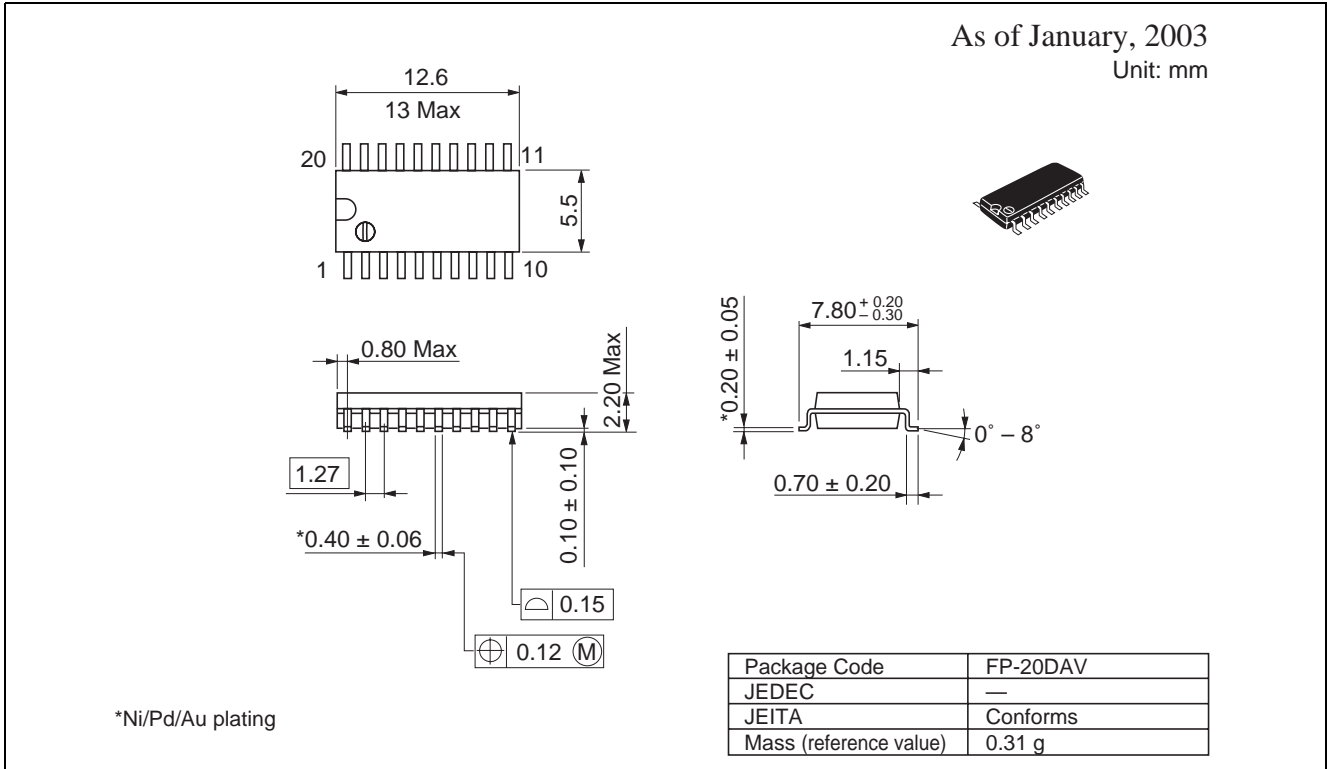
Note: When initializing output D-F/F apply "L"

Timing Chart

Example of AC Signal Generator



Package Dimensions



Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
 2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001