

HSC88

Silicon Schottky Barrier Diode for Various Detector, Mixer

REJ03G0624-0100
(Previous: ADE-208-826)
Rev.1.00
Apr 12, 2005

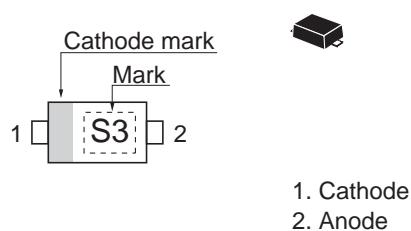
Features

- Low capacitance. ($C = 0.8 \text{ pF}$ max)
- Low forward voltage.
- Ultra small Flat Lead Package (UFP) is suitable for surface mount design.

Ordering Information

Type No.	Cathode Mark	Package Name	Package Code (Previous Code)
HSC88	S3	UFP	PWSF0002ZA-A (UFP)

Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	V _R	10	V
Average rectified current	I _o	15	mA
Junction temperature	T _j	125	°C
Storage temperature	T _{stg}	-55 to +125	°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Forward voltage	V _{F1}	0.350	—	0.420	V	I _F = 1 mA
	V _{F2}	0.500	—	0.580		I _F = 10 mA
Reverse current	I _{R1}	—	—	0.2	μA	V _R = 2 V
	I _{R2}	—	—	10		V _R = 10 V
Capacitance	C	—	—	0.80	pF	V _R = 0 V, f = 1 MHz
ESD-Capability * ¹	—	30	—	—	Ω	C = 200 pF, Both forward and reverse direction 1 pulse.

Note: 1. Failure criterion ; I_R ≥ 0.4μA at V_R = 2 V

Main Characteristic

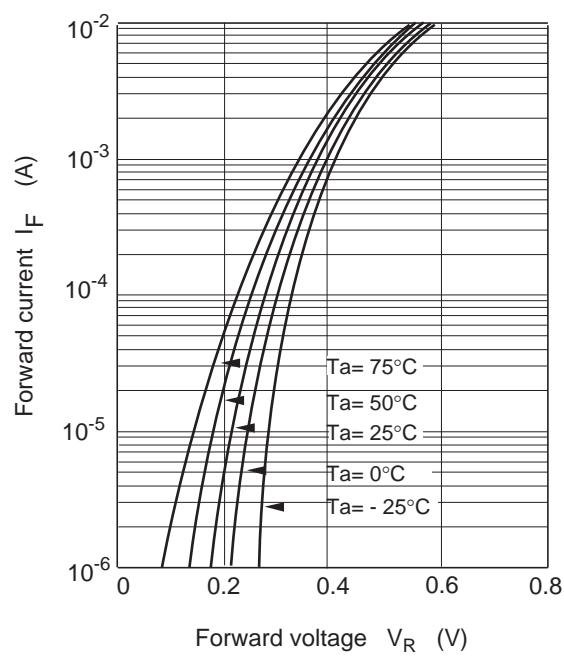


Fig.1 Forward current vs. Forward voltage

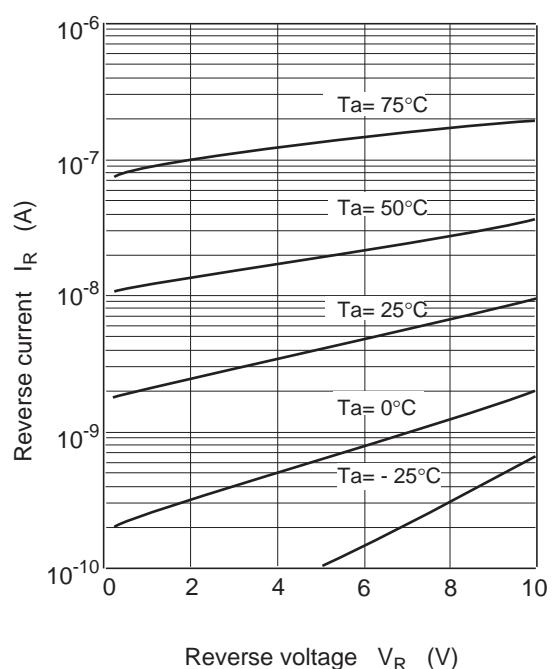


Fig.2 Reverse current vs. Reverse voltage

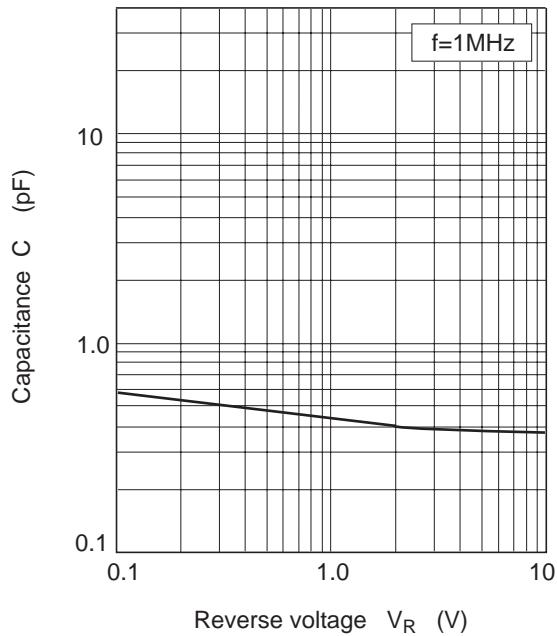
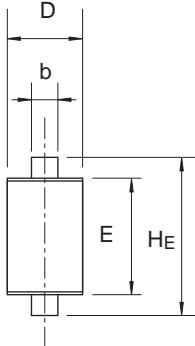


Fig.3 Capacitance vs. Reverse voltage

Package Dimensions

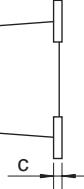
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SC-79	PWSF0002ZA-A	UFP / UFPV	0.0016g



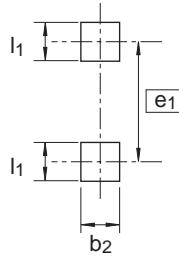
3D perspective view of the package showing dimensions D, b, E, and H_E .



Top view of the package showing dimension A.



Side view of the package showing dimension c.



Detailed view of the lead frame showing dimensions l_1 , b_2 , and e_1 .

Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.50	0.60	0.70
b	0.25	0.30	0.35
c	0.08	—	0.18
D	0.70	0.80	0.90
E	1.10	1.20	1.30
H_E	1.50	1.60	1.70
b_2	—	0.80	—
e_1	—	1.70	—
l_1	—	0.60	—

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