

# HM62V16100I Series

Wide Temperature Range Version  
16 M SRAM (1-Mword  $\times$  16-bit)

REJ03C0060-0200Z

Rev. 2.00

Oct.06.2003

## Description

The HM62V16100I Series is 16-Mbit static RAM organized 1-Mword  $\times$  16-bit. HM62V16100I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has the package variations of 48-bump chip size package with 0.75 mm bump pitch and 48-pin plastic TSOPI for high density surface mounting.

## Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 45/55 ns (max)
- Power dissipation:
  - Active: 9 mW/MHz (typ)
  - Standby: 1.5  $\mu$ W (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
  - 2 chip selection for battery backup
- Temperature range:  $-40$  to  $+85^{\circ}\text{C}$

## HM62V16100I Series

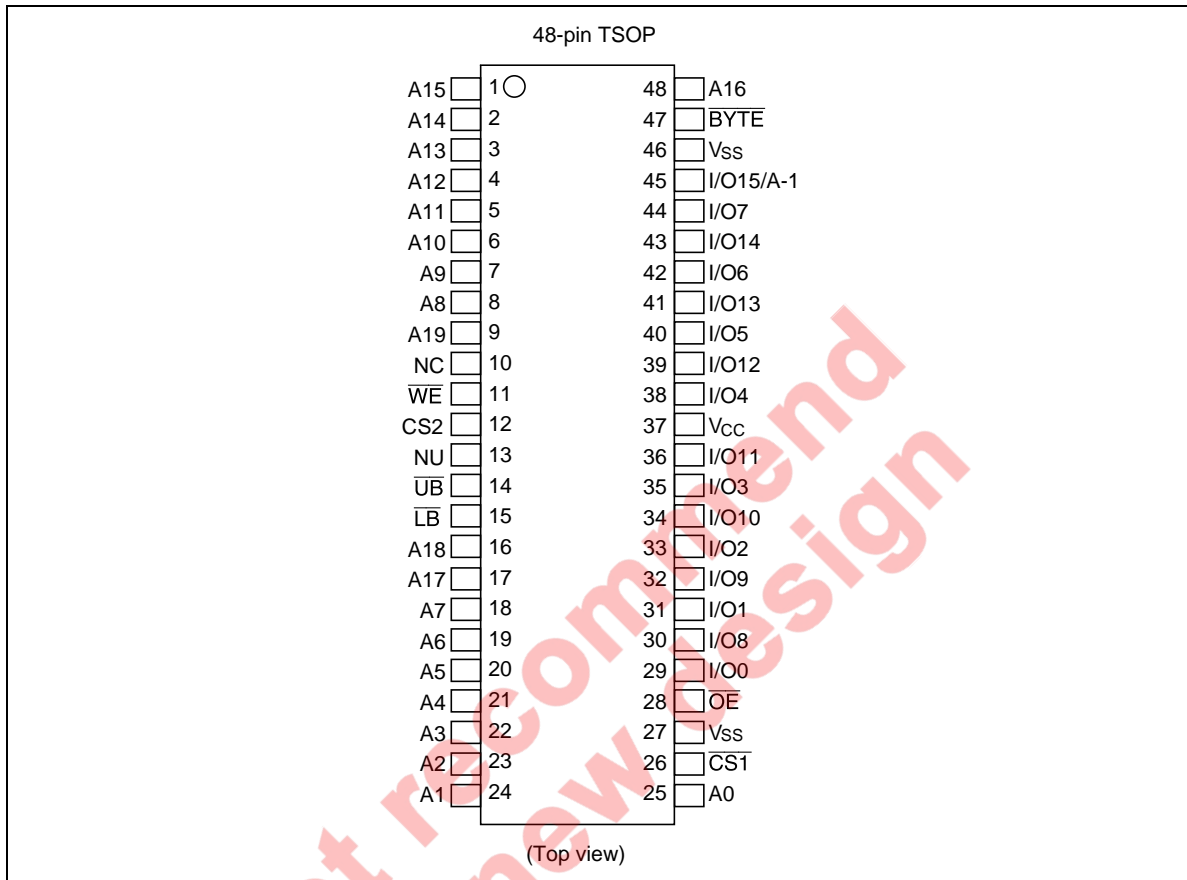
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### Ordering Information

Type No.	Access time	Package
HM62V16100LTI-4	45 ns	48-pin plastic TSOPI (normal-bend type) (TFP-48DA)
HM62V16100LTI-4SL	45 ns	
HM62V16100LTI-5SL	55 ns	
HM62V16100LBPI-4	45 ns	48-bump CSP with 0.75 mm bump pitch (TBP-48F)
HM62V16100LBPI-4SL	45 ns	
HM62V16100LBPI-5SL	55 ns	

Not recommend  
for new design

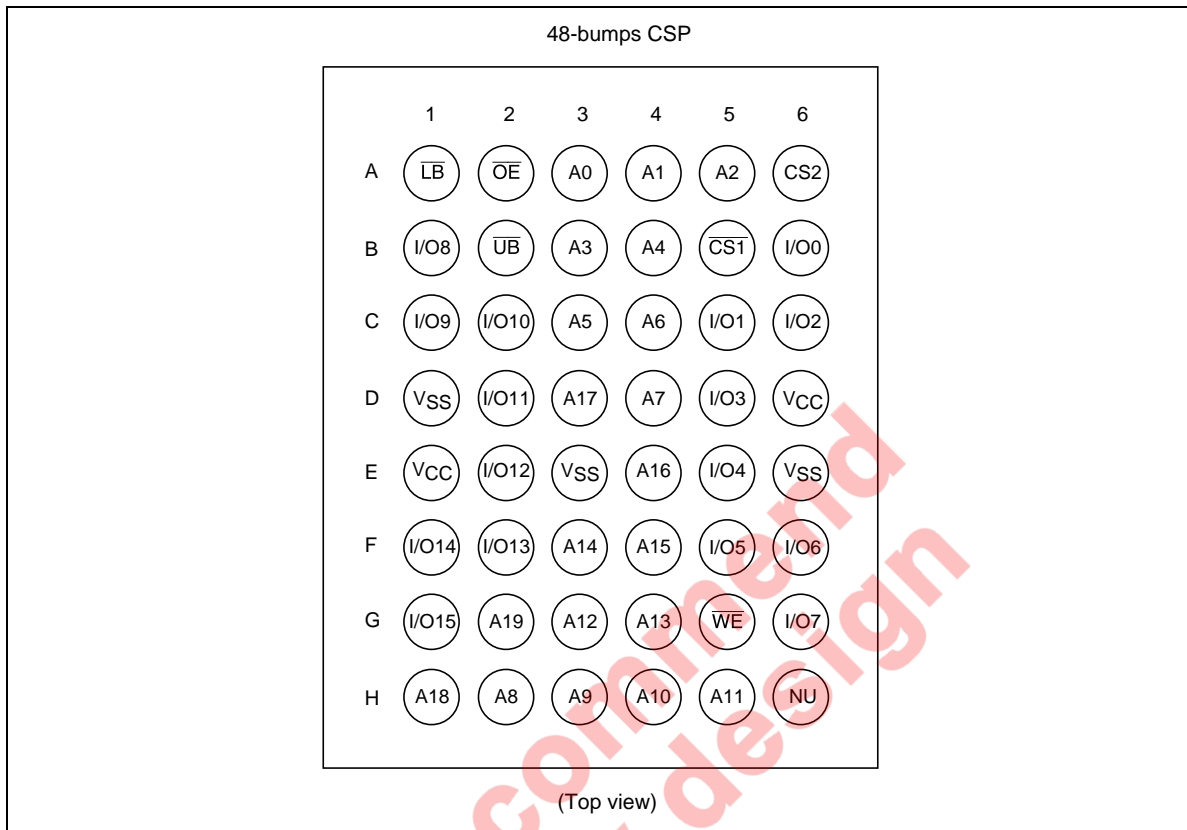
## Pin Arrangement



**Pin Description (TSOP)**

Pin name	Function
A0 to A19	Address input (word mode)
A-1 to A19	Address input (byte mode)
I/O0 to I/O15	Data input/output
$\overline{\text{CS1}}$	Chip select 1
$\overline{\text{CS2}}$	Chip select 2
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
$\overline{\text{LB}}$	Lower byte select
$\overline{\text{UB}}$	Upper byte select
$\overline{\text{BYTE}}$	Byte enable
$V_{\text{CC}}$	Power supply
$V_{\text{SS}}$	Ground
NC	No connection
NU* <sup>1</sup>	Not used (test mode pin)

Note: 1. This pin should be connected to a ground ( $V_{\text{SS}}$ ), or not be connected (open).

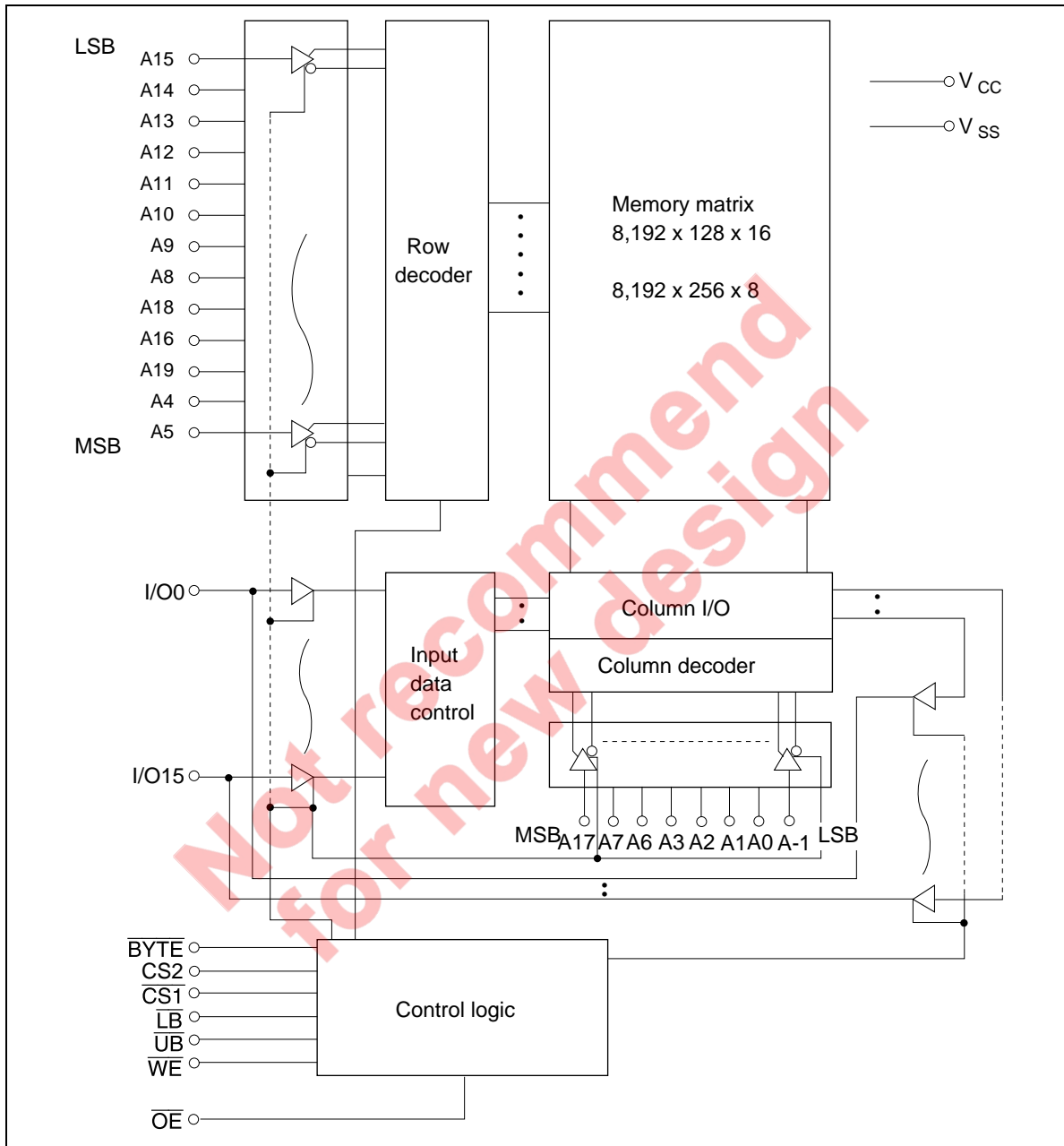


### Pin Description (CSP)

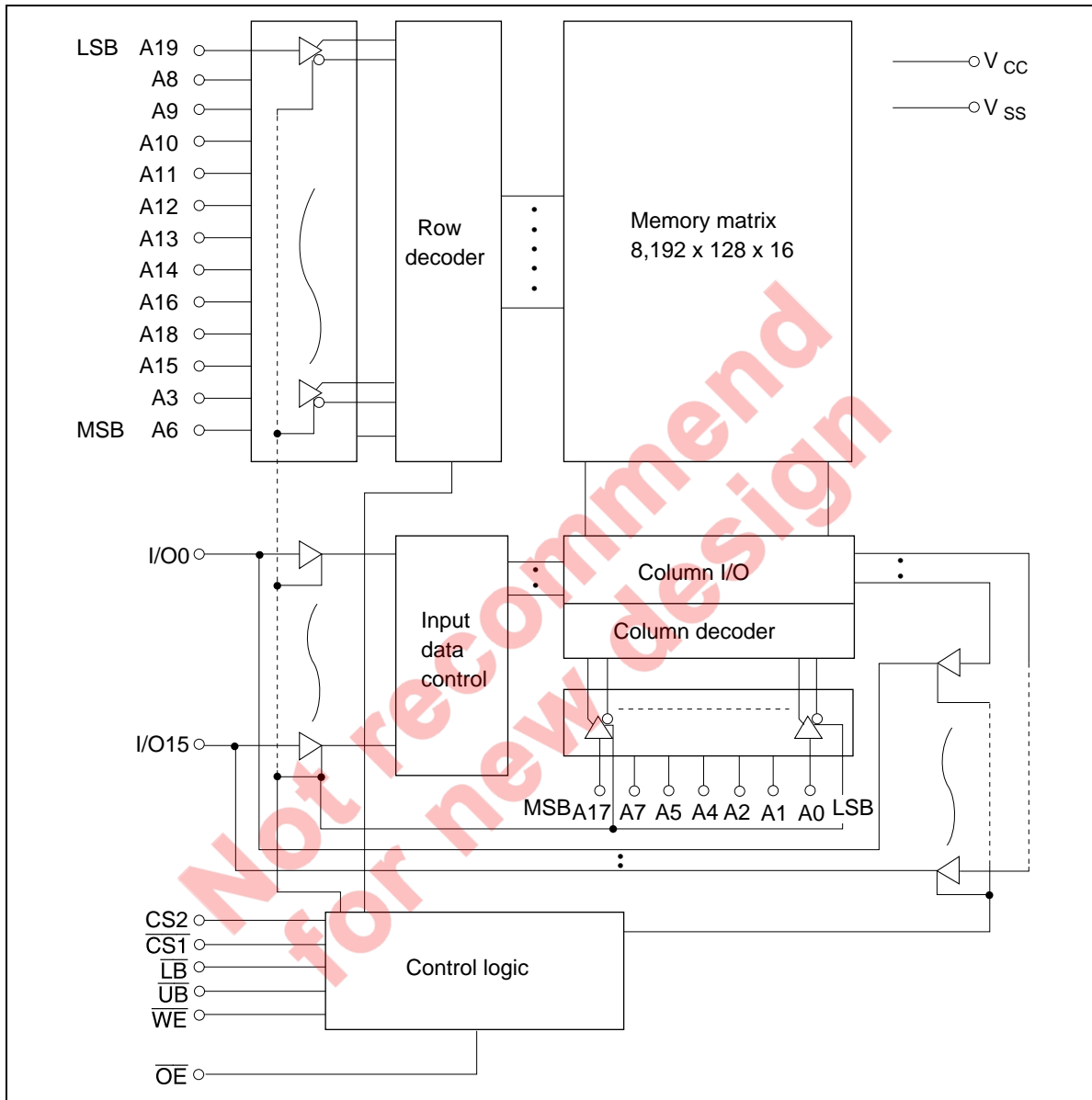
Pin name	Function
A0 to A19	Address input
I/O0 to I/O15	Data input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
LB	Lower byte select
UB	Upper byte select
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NU <sup>*1</sup>	Not used (test mode pin)

Note: 1. This pin should be connected to a ground (V<sub>SS</sub>), or not be connected (open).

## Block Diagram (TSOP)



# Block Diagram (CSP)



## Operation Table (TSOP)

## Byte mode

$\overline{\text{CS1}}$	CS2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{UB}}$	$\overline{\text{LB}}$	$\overline{\text{BYTE}}$	I/O0 to I/O7	I/O8 to I/O14	I/O15	Operation
H	x	x	x	x	x	L	High-Z	High-Z	High-Z	Standby
x	L	x	x	x	x	L	High-Z	High-Z	High-Z	Standby
L	H	H	L	x	x	L	Dout	High-Z	A-1	Read
L	H	L	x	x	x	L	Din	High-Z	A-1	Write
L	H	H	H	x	x	L	High-Z	High-Z	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , x:  $V_{IH}$  or  $V_{IL}$

## Word mode

$\overline{\text{CS1}}$	CS2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{UB}}$	$\overline{\text{LB}}$	$\overline{\text{BYTE}}$	I/O0 to I/O7	I/O8 to I/O14	I/O15	Operation
H	x	x	x	x	x	H	High-Z	High-Z	High-Z	Standby
x	L	x	x	x	x	H	High-Z	High-Z	High-Z	Standby
x	x	x	x	H	H	H	High-Z	High-Z	High-Z	Standby
L	H	H	L	L	L	H	Dout	Dout	Dout	Read
L	H	H	L	H	L	H	Dout	High-Z	High-Z	Lower byte read
L	H	H	L	L	H	H	High-Z	Dout	Dout	Upper byte read
L	H	L	x	L	L	H	Din	Din	Din	Write
L	H	L	x	H	L	H	Din	High-Z	High-Z	Lower byte write
L	H	L	x	L	H	H	High-Z	Din	Din	Upper byte write
L	H	H	H	x	x	H	High-Z	High-Z	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , x:  $V_{IH}$  or  $V_{IL}$



## Operation Table (CSP)

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	−0.5 to +4.6	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	−0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Storage temperature range	$T_{stg}$	−55 to +125	°C
Storage temperature range under bias	$T_{bias}$	−40 to +85	°C

Notes: 1.  $V_T$  min: −2.0 V for pulse half-width ≤ 10 ns.

2. Maximum voltage is +4.6 V.

## DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	2.7	3.0	3.6	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{IL}$	−0.3	—	0.6	V	1
Ambient temperature range	$T_a$	−40	—	+85	°C	

Note: 1.  $V_{IL}$  min: −2.0 V for pulse half-width ≤ 10 ns.

## DC Characteristics

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions* <sup>2</sup>
Input leakage current	$ I_{IL} $	—	—	1	$\mu A$	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	$\mu A$	$\overline{CS1} = V_{IH} \text{ or } CS2 = V_{IL} \text{ or}$ $\overline{OE} = V_{IH} \text{ or } \overline{WE} = V_{IL} \text{ or}$ $\overline{LB} = \overline{UB} = V_{IH}, V_{I/O} = V_{SS} \text{ to } V_{CC}$
Operating current	$I_{CC}$	—	—	20	mA	$\overline{CS1} = V_{IL}, CS2 = V_{IH},$ Others = $V_{IH}/V_{IL}, I_{I/O} = 0 \text{ mA}$
Average operating current	$I_{CC1}$ (READ)	—	22	35	mA	Min. cycle, duty = 100%, $I_{I/O} = 0 \text{ mA}, \overline{CS1} = V_{IL}, CS2 = V_{IH},$ $\overline{WE} = V_{IH},$ Others = $V_{IH}/V_{IL}$
	$I_{CC1}$	—	30	50	mA	Min. cycle, duty = 100%, $I_{I/O} = 0 \text{ mA}, \overline{CS1} = V_{IL}, CS2 = V_{IH},$ Others = $V_{IH}/V_{IL}$
	$I_{CC2}^{*5}$ (READ)	—	3	8	mA	Cycle time = 70 ns, duty = 100%, $I_{I/O} = 0 \text{ mA}, \overline{CS1} = V_{IL}, CS2 = V_{IH},$ $\overline{WE} = V_{IH},$ Others = $V_{IH}/V_{IL}$ Address increment scan or decrement scan
	$I_{CC2}^{*5}$	—	20	30	mA	Cycle time = 70 ns, duty = 100%, $I_{I/O} = 0 \text{ mA}, \overline{CS1} = V_{IL}, CS2 = V_{IH},$ Others = $V_{IH}/V_{IL}$ Address increment scan or decrement scan
	$I_{CC3}$	—	3	8	mA	Cycle time = 1 $\mu s$ , duty = 100%, $I_{I/O} = 0 \text{ mA}, \overline{CS1} \leq 0.2 \text{ V},$ $CS2 \geq V_{CC} - 0.2 \text{ V}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}, V_{IL} \leq 0.2 \text{ V}$
Standby current	$I_{SB}$	—	0.1	0.5	mA	$CS2 = V_{IL}$
Standby current	$I_{SB1}^{*3}$	—	0.5	25	$\mu A$	$0 \text{ V} \leq V_{in}$ (1) $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$ or (2) $\overline{CS1} \geq V_{CC} - 0.2 \text{ V},$ $CS2 \geq V_{CC} - 0.2 \text{ V}$ or (3) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2 \text{ V},$ $CS2 \geq V_{CC} - 0.2 \text{ V},$ $\overline{CS1} \leq 0.2 \text{ V}$ Average value
	$I_{SB1}^{*4}$	—	0.5	8	$\mu A$	
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1 \text{ mA}$
	$V_{OH}$	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100 \mu A$
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2 \text{ mA}$
	$V_{OL}$	—	—	0.2	V	$I_{OL} = 100 \mu A$

## HM62V16100I Series

- Notes:
1. Typical values are at  $V_{CC} = 3.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  and not guaranteed.
  2.  $\overline{\text{BYTE}}$  pin supported by only TSOP type.  
 $\overline{\text{BYTE}} \geq V_{CC} - 0.2\text{ V}$  or  $\overline{\text{BYTE}} \leq 0.2\text{ V}$
  3. This characteristic is guaranteed only for L-version.
  4. This characteristic is guaranteed only for L-SL version.
  5.  $I_{CC2}$  is the value measured while the valid address is increasing or decreasing by one bit.  
Word mode: LSB (least significant bit) is A0.  
Byte mode: LSB (least significant bit) is A-1.

## Capacitance

( $T_a = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	—	8	pF	$V_{in} = 0\text{ V}$	1
Input/output capacitance	$C_{i/o}$	—	—	10	pF	$V_{i/o} = 0\text{ V}$	1

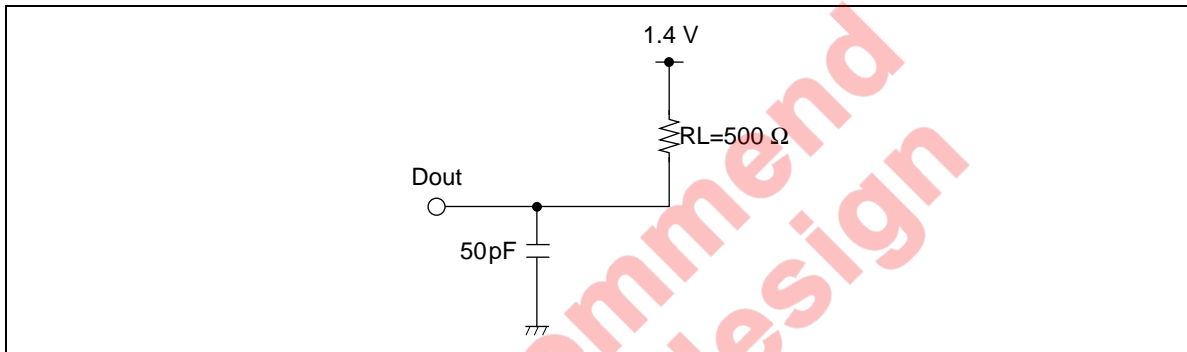
Note: 1. This parameter is sampled and not 100% tested.

## AC Characteristics

( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7$  V to  $3.6$  V, unless otherwise noted.)

### Test Conditions

- Input pulse levels:  $V_{IL} = 0.4$  V,  $V_{IH} = 2.4$  V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.4 V
- Output load: See figures (Including scope and jig)



## HM62V16100I Series

### Read Cycle

		HM62V16100I					
		-4		-5			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t <sub>RC</sub>	45	—	55	—	ns	
Address access time	t <sub>AA</sub>	—	45	—	55	ns	
Chip select access time	t <sub>ACS1</sub>	—	45	—	55	ns	
	t <sub>ACS2</sub>	—	45	—	55	ns	
Output enable to output valid	t <sub>OE</sub>	—	30	—	35	ns	
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns	
LB, UB access time	t <sub>BA</sub>	—	45	—	55	ns	
Chip select to output in low-Z	t <sub>CLZ1</sub>	10	—	10	—	ns	2, 3
	t <sub>CLZ2</sub>	10	—	10	—	ns	2, 3
LB, UB enable to low-Z	t <sub>BLZ</sub>	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t <sub>CHZ1</sub>	0	20	0	20	ns	1, 2, 3
	t <sub>CHZ2</sub>	0	20	0	20	ns	1, 2, 3
LB, UB disable to high-Z	t <sub>BHZ</sub>	0	15	0	20	ns	1, 2, 3
Output disable to output in high-Z	t <sub>OHZ</sub>	0	15	0	20	ns	1, 2, 3

### Write Cycle

		HM62V16100I					
		-4		-5			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t <sub>WC</sub>	45	—	55	—	ns	
Address valid to end of write	t <sub>AW</sub>	45	—	50	—	ns	
Chip selection to end of write	t <sub>CW</sub>	45	—	50	—	ns	5
Write pulse width	t <sub>WP</sub>	35	—	40	—	ns	4
LB, UB valid to end of write	t <sub>BW</sub>	45	—	50	—	ns	
Address setup time	t <sub>AS</sub>	0	—	0	—	ns	6
Write recovery time	t <sub>WR</sub>	0	—	0	—	ns	7
Data to write time overlap	t <sub>DW</sub>	25	—	25	—	ns	
Data hold from write time	t <sub>DH</sub>	0	—	0	—	ns	
Output active from end of write	t <sub>OW</sub>	5	—	5	—	ns	2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	15	0	20	ns	1, 2
Write to output in high-Z	t <sub>WHZ</sub>	0	15	0	20	ns	1, 2

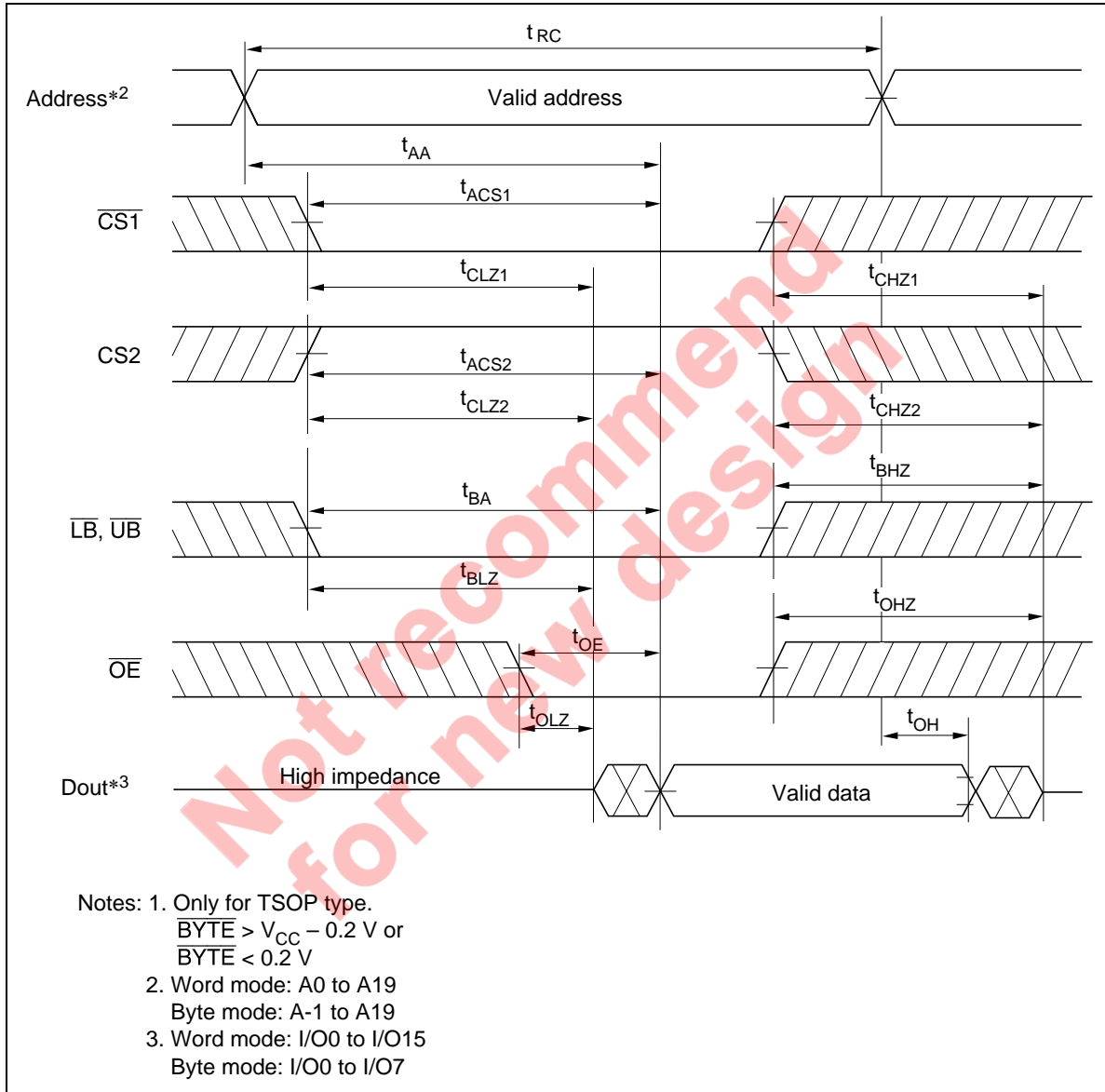
Byte Control

		HM62V16100I					
		-4		-5			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
BYTE setup time	t <sub>BS</sub>	5	—	5	—	ms	8
BYTE recovery time	t <sub>BR</sub>	5	—	5	—	ms	8

- Notes:
1.  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  4. A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2, a low  $\overline{WE}$  and a low  $\overline{LB}$  or a low  $\overline{UB}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high,  $\overline{WE}$  going low and  $\overline{LB}$  going low or  $\overline{UB}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low,  $\overline{WE}$  going high and  $\overline{LB}$  going high or  $\overline{UB}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  5.  $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
  6.  $t_{AS}$  is measured from the address valid to the beginning of write.
  7.  $t_{WR}$  is measured from the earliest of  $\overline{CS1}$  or  $\overline{WE}$  going high or CS2 going low to the end of write cycle.
  8. Byte control supported by only TSOP type.

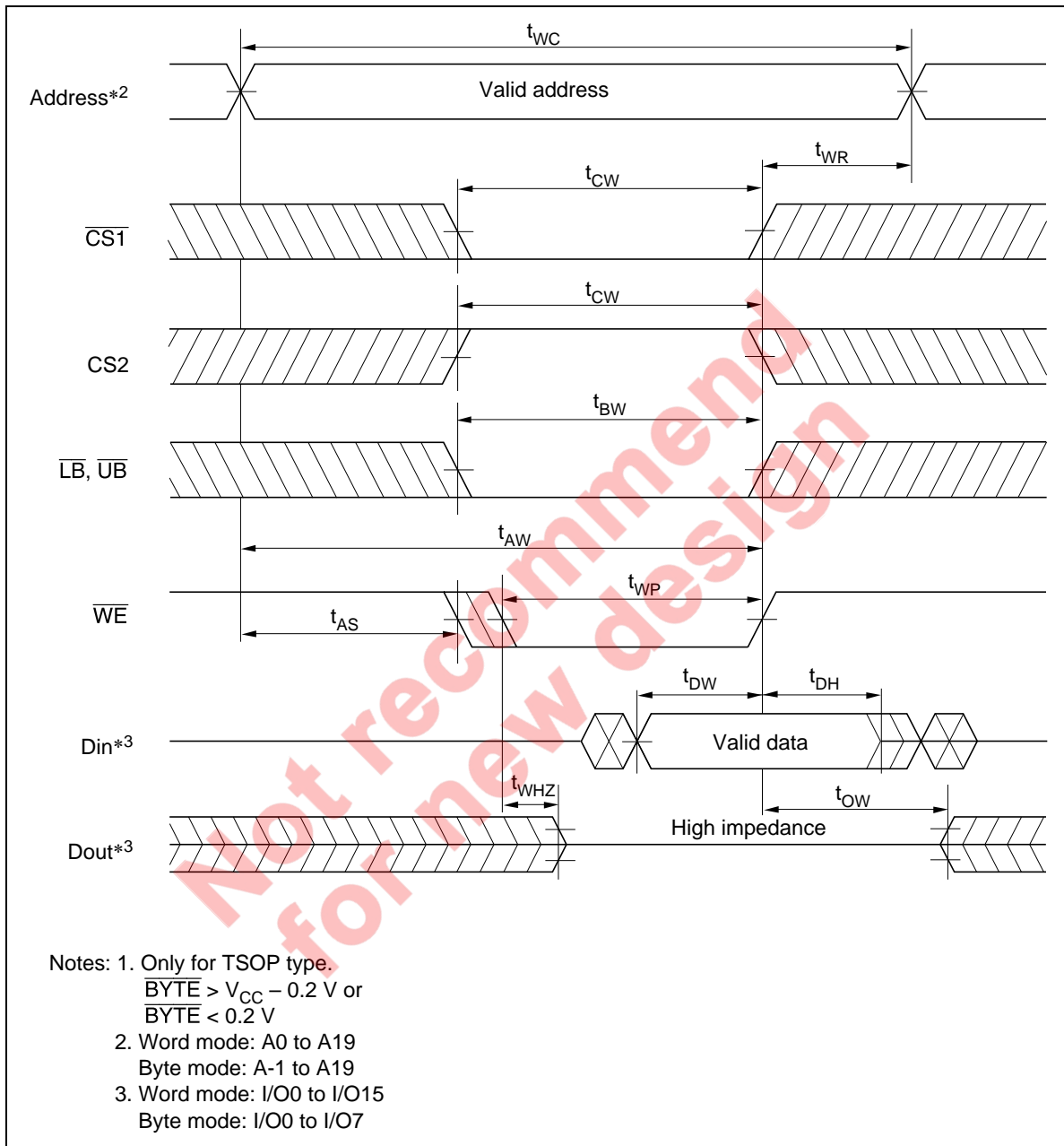
## Timing Waveform

### Read Cycle\*<sup>1</sup>



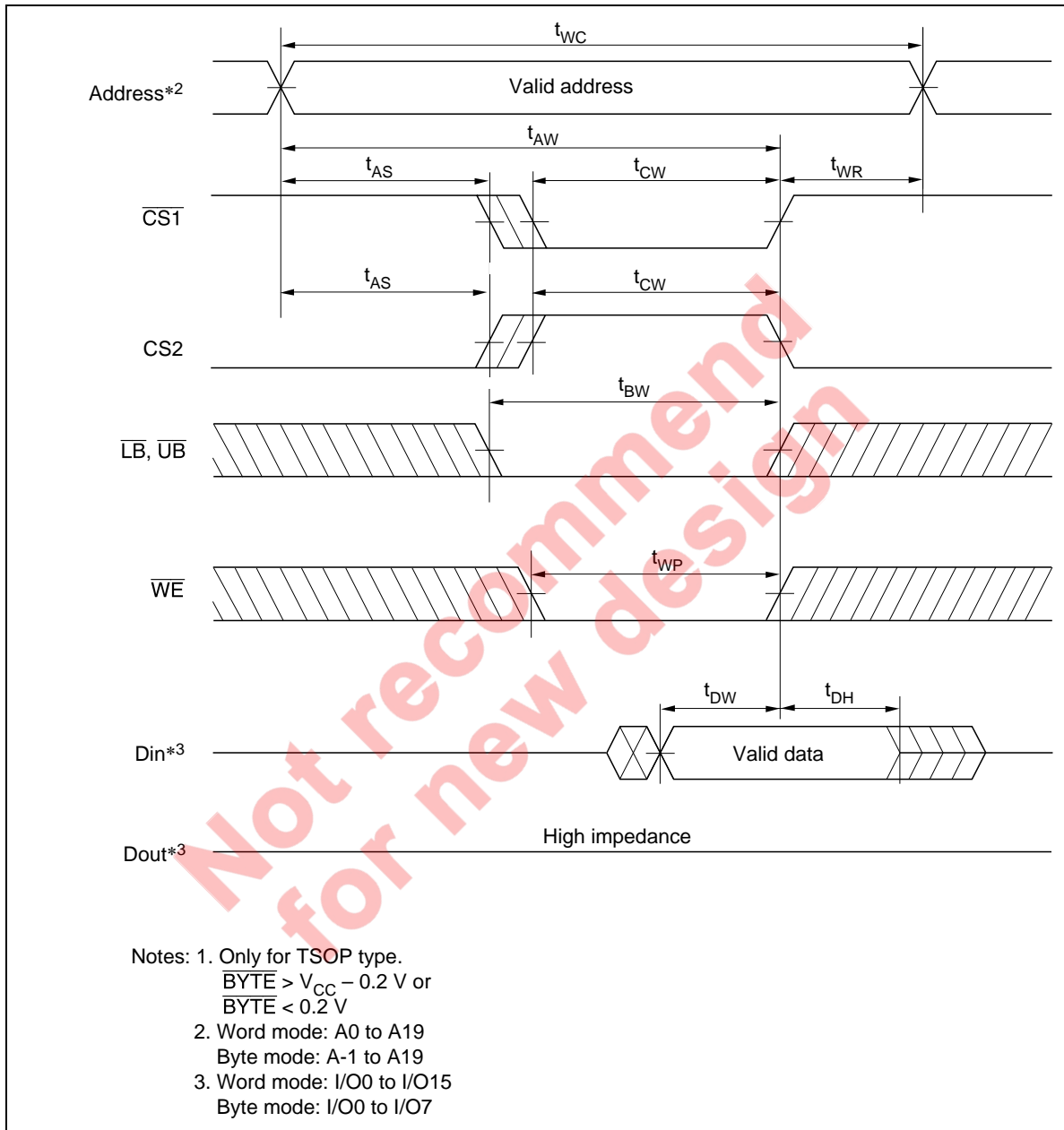
## HM62V16100I Series

### Write Cycle (1)\*<sup>1</sup> ( $\overline{\text{WE}}$ Clock)



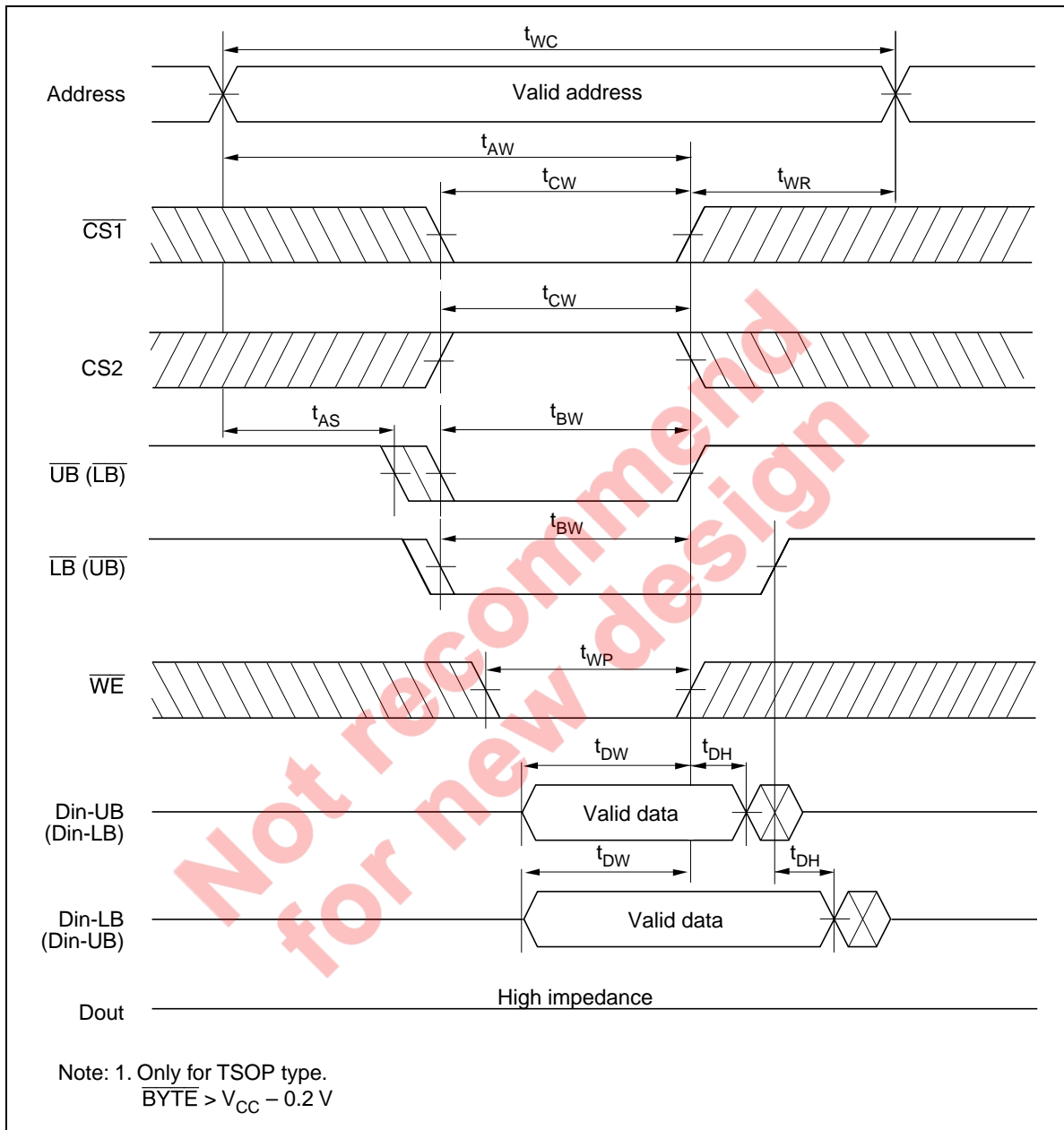


Write Cycle (2)\*<sup>1</sup> ( $\overline{CS1}$ , CS2 Clock,  $\overline{OE} = V_{IH}$ )

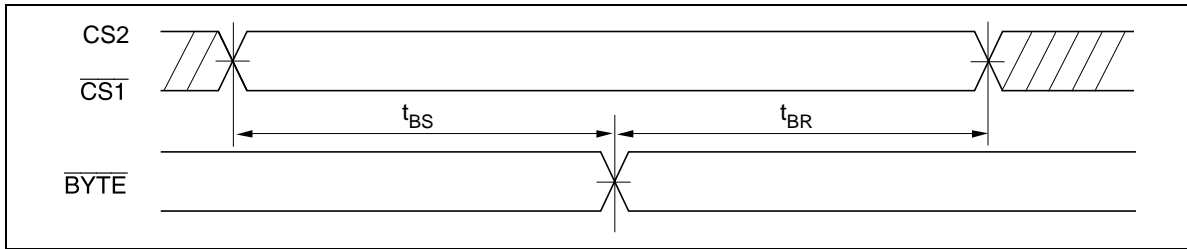


## HM62V16100I Series

Write Cycle (3)\*<sup>1</sup> ( $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  Clock,  $\overline{\text{OE}} = V_{\text{IH}}$ )



Byte Control (TSOP)



Not recommend  
for new design

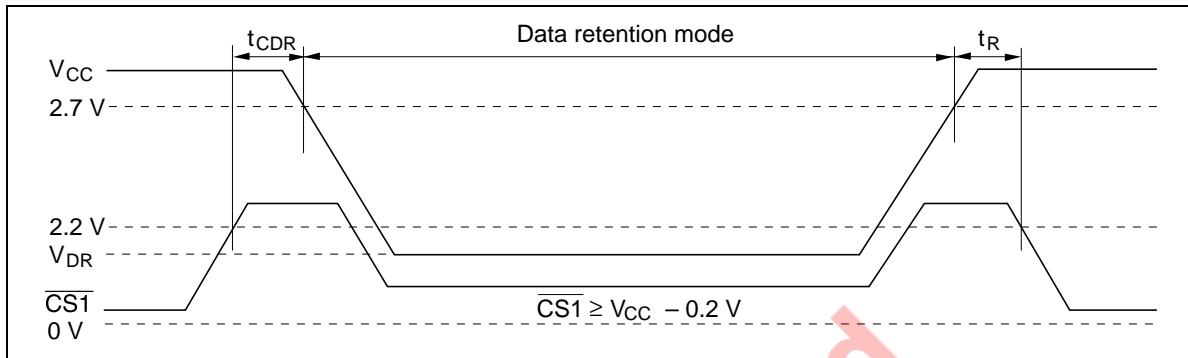
Low  $V_{CC}$  Data Retention Characteristics

(Ta = -40 to +85°C)

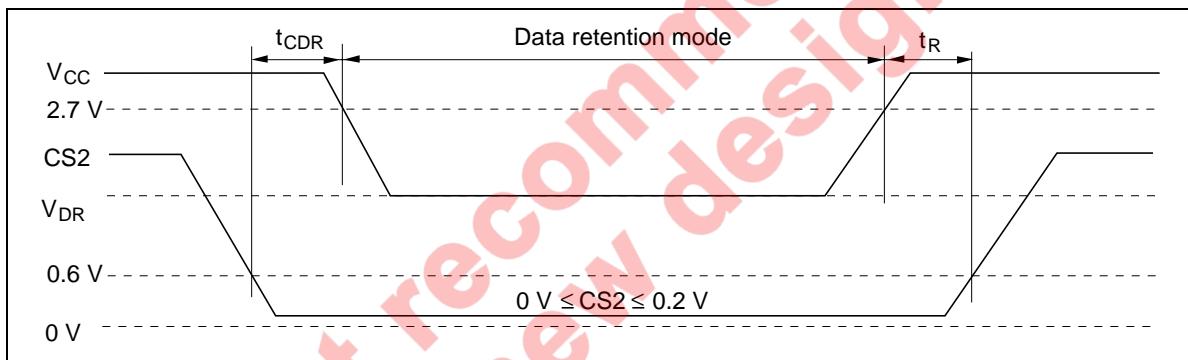
Parameter	Symbol	Min	Typ <sup>*5</sup>	Max	Unit	Test conditions <sup>*3,4</sup>
$V_{CC}$ for data retention	$V_{DR}$	1.5	—	3.6	V	Vin ≥ 0 V (1) $0\text{ V} \leq \text{CS2} \leq 0.2\text{ V}$ or (2) $\text{CS2} \geq V_{CC} - 0.2\text{ V}$ , $\text{CS1} \geq V_{CC} - 0.2\text{ V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{CC} - 0.2\text{ V}$ , $\text{CS2} \geq V_{CC} - 0.2\text{ V}$ , $\text{CS1} \leq 0.2\text{ V}$
Data retention current	$I_{CCDR}^{*1}$	—	0.5	25	μA	$V_{CC} = 3.0\text{ V}$ , Vin ≥ 0 V (1) $0\text{ V} \leq \text{CS2} \leq 0.2\text{ V}$ or (2) $\text{CS2} \geq V_{CC} - 0.2\text{ V}$ , $\text{CS1} \geq V_{CC} - 0.2\text{ V}$ or (3) $\overline{\text{LB}} = \overline{\text{UB}} \geq V_{CC} - 0.2\text{ V}$ , $\text{CS2} \geq V_{CC} - 0.2\text{ V}$ , $\text{CS1} \leq 0.2\text{ V}$ Average value
	$I_{CCDR}^{*2}$	—	0.5	8	μA	
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveforms
Operation recovery time	$t_R$	5	—	—	ms	

- Notes: 1. This characteristic is guaranteed only for L-version.  
 2. This characteristic is guaranteed only for L-SL version.  
 3.  $\overline{\text{BYTE}}$  pin supported by only TSOP type.  
 $\overline{\text{BYTE}} \geq V_{CC} - 0.2\text{ V}$  or  $\overline{\text{BYTE}} \leq 0.2\text{ V}$   
 4. CS2 controls address buffer,  $\overline{\text{WE}}$  buffer,  $\overline{\text{CS1}}$  buffer,  $\overline{\text{OE}}$  buffer,  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{CS1}}$ ,  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$ , I/O) can be in the high impedance state. If  $\overline{\text{CS1}}$  controls data retention mode, CS2 must be  $\text{CS2} \geq V_{CC} - 0.2\text{ V}$  or  $0\text{ V} \leq \text{CS2} \leq 0.2\text{ V}$ . The other input levels (address,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$ , I/O) can be in the high impedance state.  
 5. Typical values are at  $V_{CC} = 3.0\text{ V}$ , Ta = +25°C and not guaranteed.

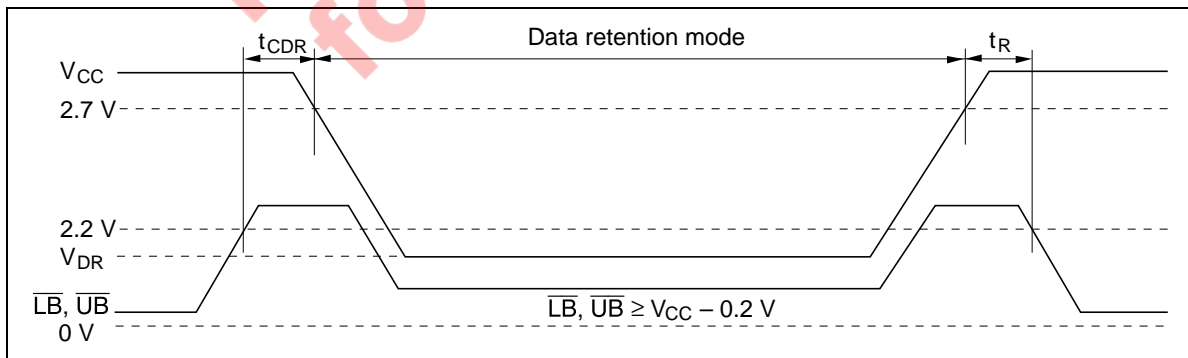
Low  $V_{CC}$  Data Retention Timing Waveform (1) ( $\overline{CS1}$  Controlled)



Low  $V_{CC}$  Data Retention Timing Waveform (2) ( $CS2$  Controlled)



Low  $V_{CC}$  Data Retention Timing Waveform (3) ( $\overline{LB}$ ,  $\overline{UB}$  Controlled)



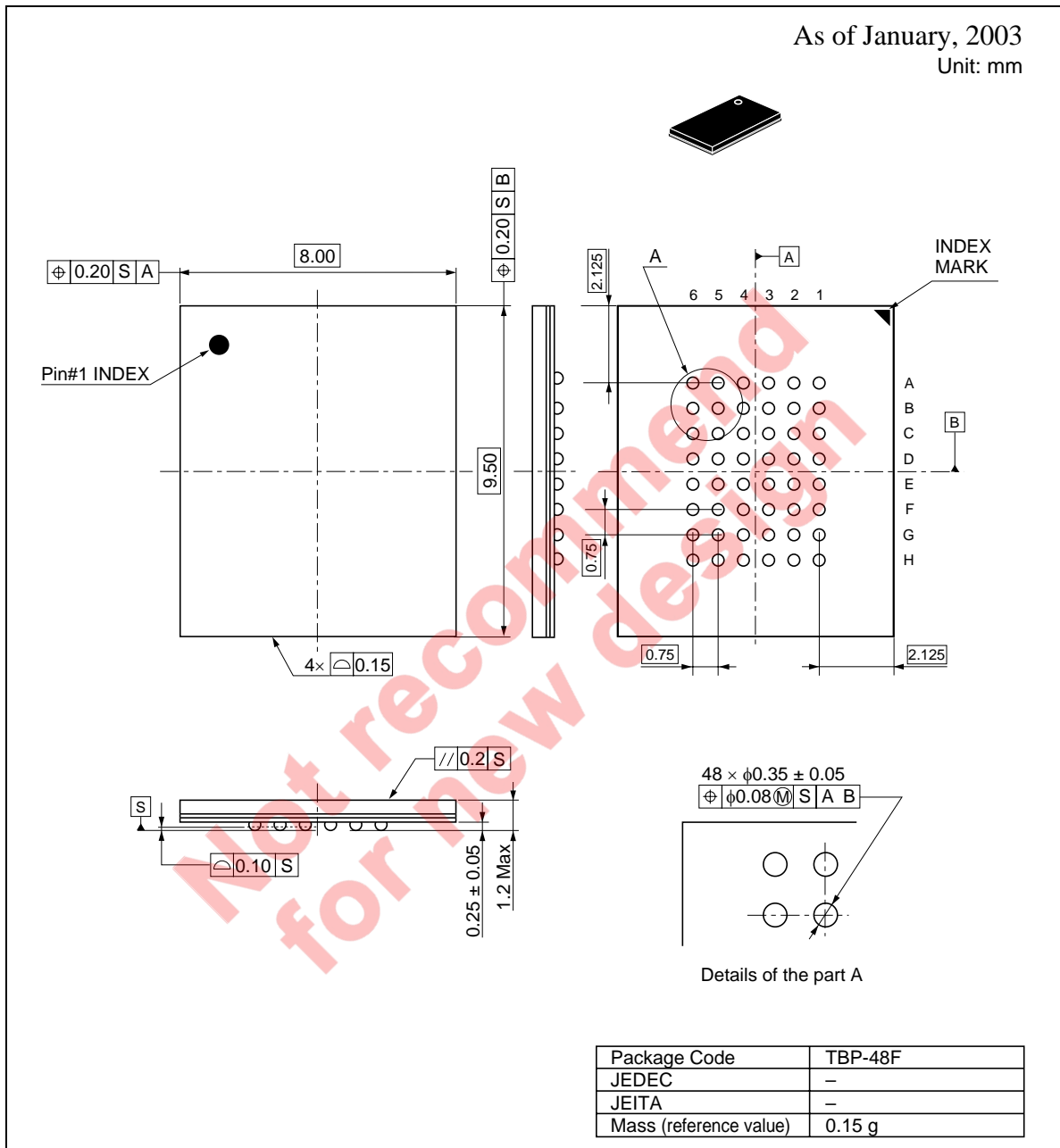


# HM62V16100I Series

## HM62V16100LBPI Series (TBP-48F)

As of January, 2003

Unit: mm



## Revision History

## HM62V16100I Series Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.0	Sep. 21, 2001	—	Initial issue
1.00	Jun.19, 2003	—	Deletion of Preliminary
2.00	Oct.06, 2003	—	Deletion of HM62V16100LT1-5, HM62V16100LBPI-5

Not recommend  
for new design



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