

HAT2129H

Silicon N Channel Power MOS FET Power Switching

REJ03G0049-0500

Rev.5.00

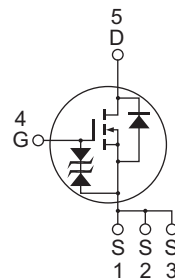
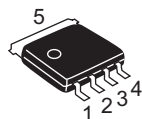
Sep 20, 2005

Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 6 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline

RENESAS Package code: PTZZ0005DA-A)
(Package name: LFPAK)



1, 2, 3 Source
4 Gate
5 Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	30	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	120	A
Body-drain diode reverse drain current	I_{DR}	30	A
Avalanche current	I_{AP} ^{Note 3}	20	A
Avalanche energy	E_{AR} ^{Note 3}	32	mJ
Channel dissipation	P_{ch} ^{Note2}	20	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. $T_c = 25^\circ\text{C}$

3. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

Electrical Characteristics

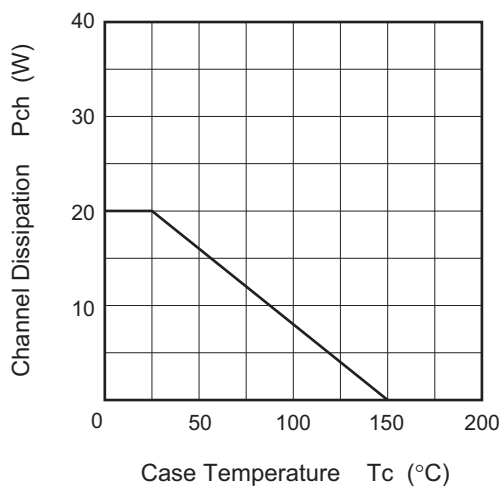
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	6.0	7.5	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	7.0	9.5	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 7 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	24	40	—	S	$I_D = 15 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	3200	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	450	—	pF	
Reverse transfer capacitance	C_{rss}	—	260	—	pF	
Total gate charge	Q_g	—	46	—	nC	$V_{DD} = 10 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 30 \text{ A}$
Gate to source charge	Q_{gs}	—	13.5	—	nC	
Gate to drain charge	Q_{gd}	—	7.5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	22	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$, $V_{DD} \cong 10 \text{ V}$, $R_L = 0.67 \text{ }\Omega$, $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	33	—	ns	
Turn-off delay time	$t_{d(off)}$	—	67	—	ns	
Fall time	t_f	—	11	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.84	1.10	V	$I_F = 30 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 30 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu\text{s}$

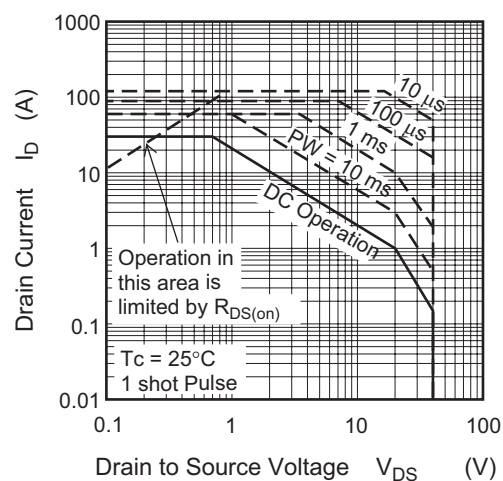
Notes: 4. Pulse test

Main Characteristics

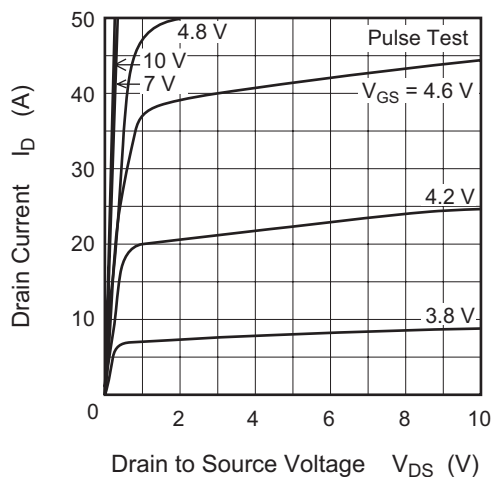
Power vs. Temperature Derating



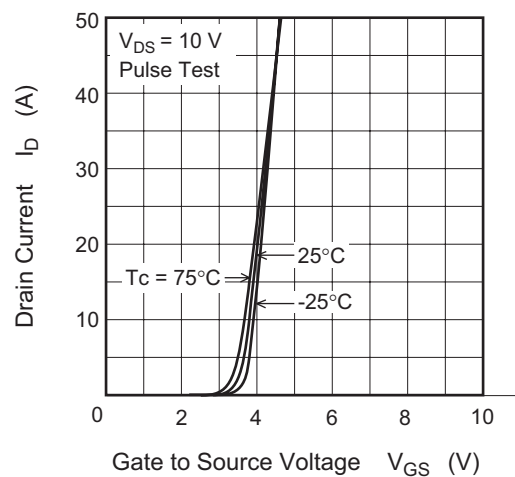
Maximum Safe Operation Area



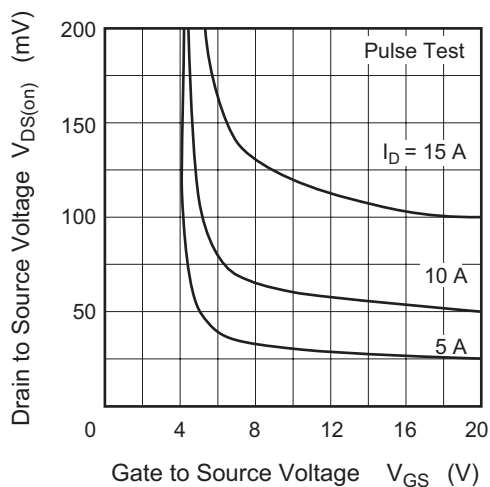
Typical Output Characteristics



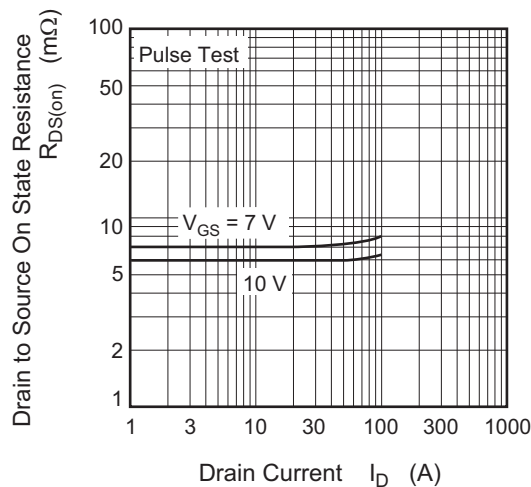
Typical Transfer Characteristics

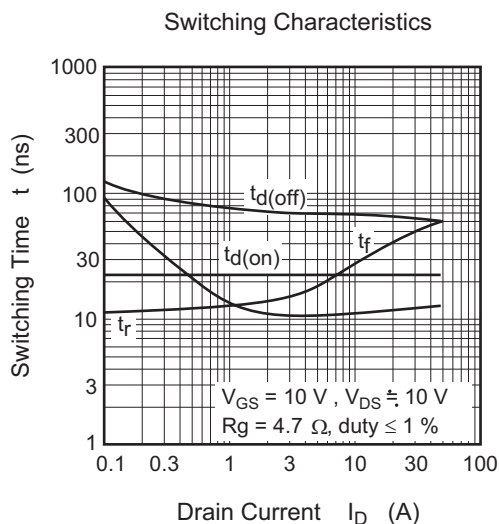
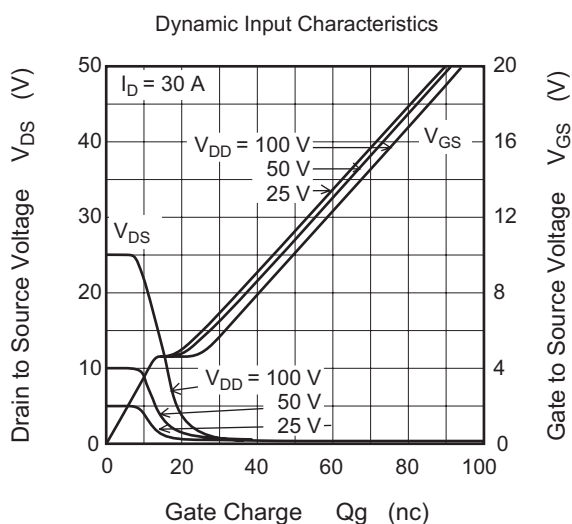
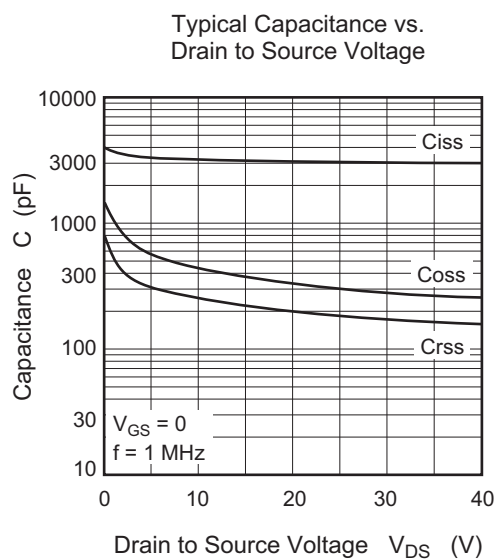
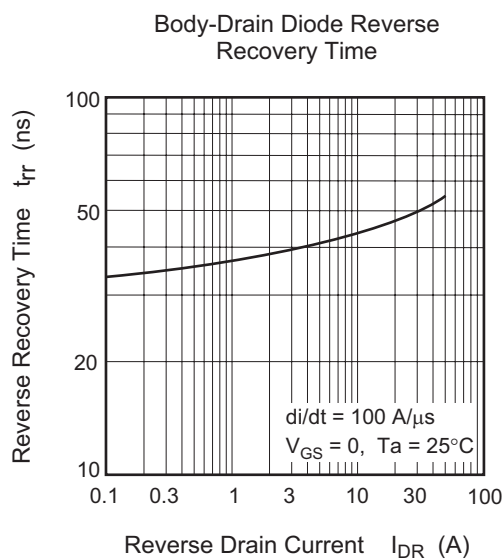
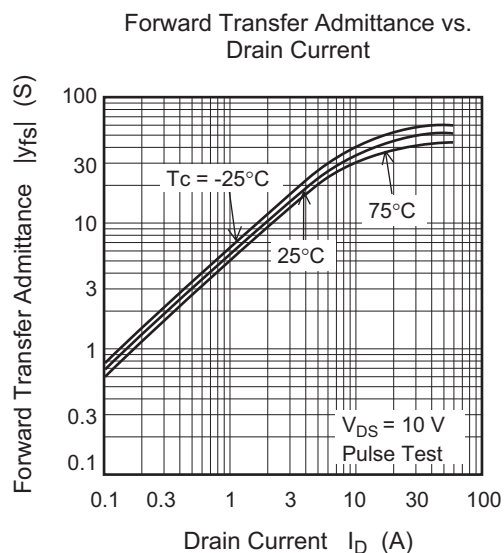
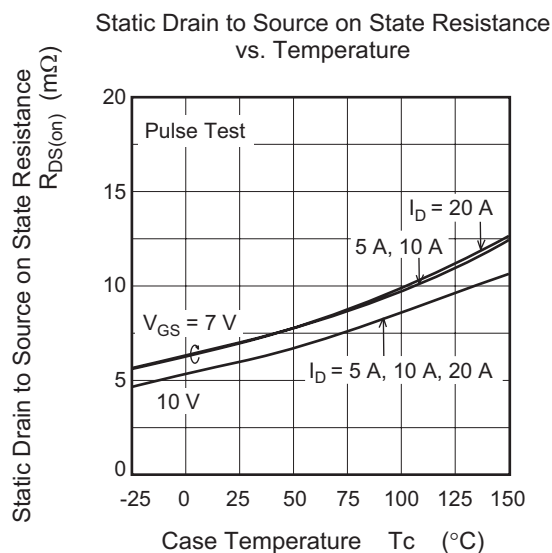


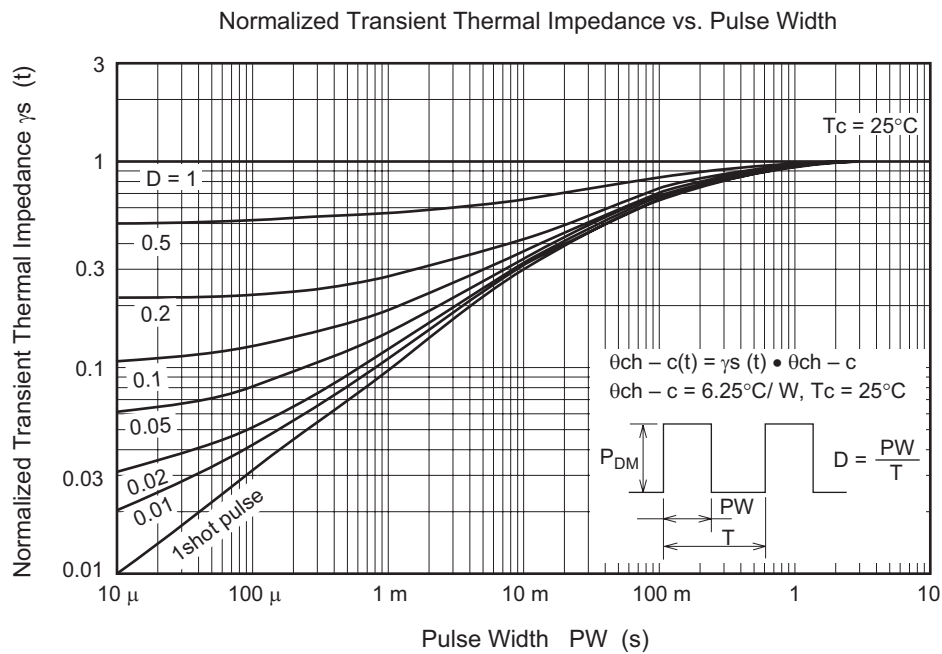
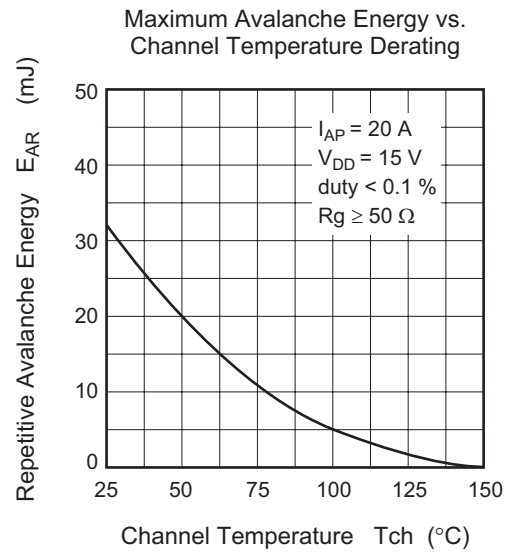
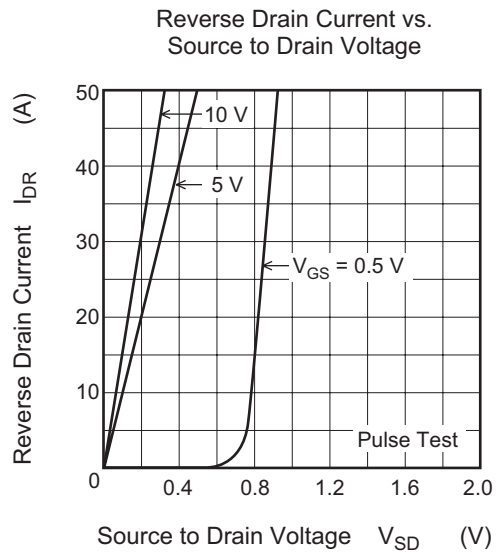
Drain to Source Saturation Voltage vs. Gate to Source Voltage



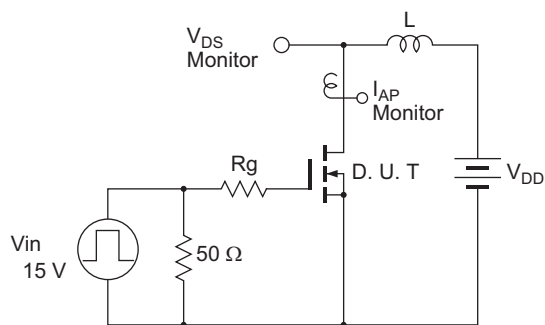
Static Drain to Source on State Resistance vs. Drain Current



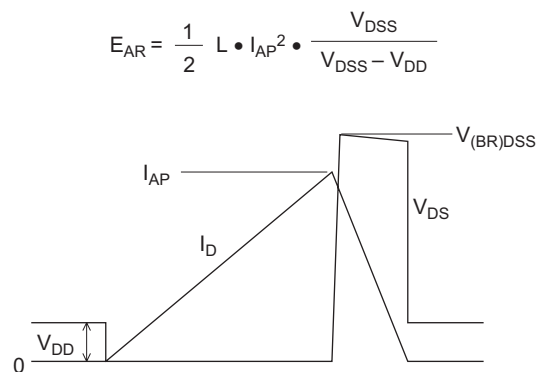




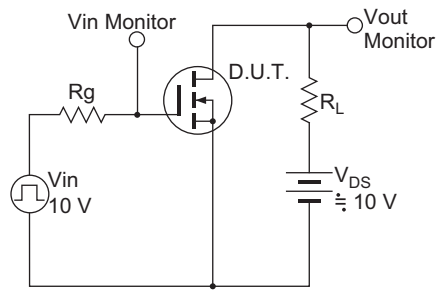
Avalanche Test Circuit



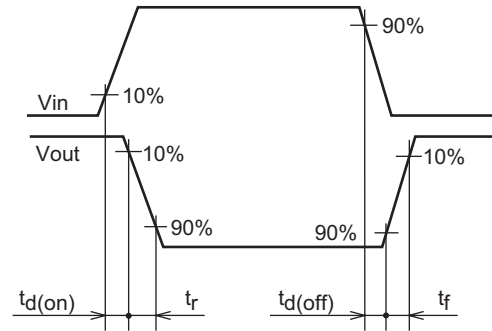
Avalanche Waveform



Switching Time Test Circuit



Switching Time Waveform



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