

HAT1043M

Silicon P Channel Power MOS FET Power Switching

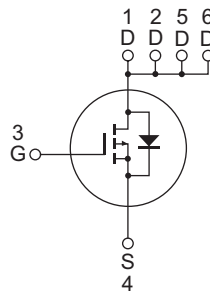
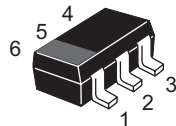
REJ03G1151-0600
(Previous: ADE-208-754D)
Rev.6.00
Sep 07, 2005

Features

- Low on-resistance
- Low drive current
- High density mounting
- 2.5 V gate drive device can be driven from 3 V source

Outline

RENESAS Package code: PTSP0006FA-A
(Package name: TSOP-6)



4 Source
3 Gate
1, 2, 5, 6 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DS}	-20	V
Gate to source voltage	V_{GS}	±12	V
Drain current	I_D	-4.4	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	-17.6	A
Body-drain diode reverse drain current	I_{DR} ^{Note 2}	-4.4	A
Channel dissipation	$P_{ch(pulse)}$ ^{Note 2}	2.0	W
Channel dissipation	$P_{ch(continuous)}$ ^{Note 3}	1.05	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. When using the alumina ceramic board (50 × 50 × 0.7 mm), $PW \leq 5 s$, $T_a = 25^\circ C$ 3. When using the alumina ceramic board (50 × 50 × 0.7 mm), $T_a = 25^\circ C$

Electrical Characteristics

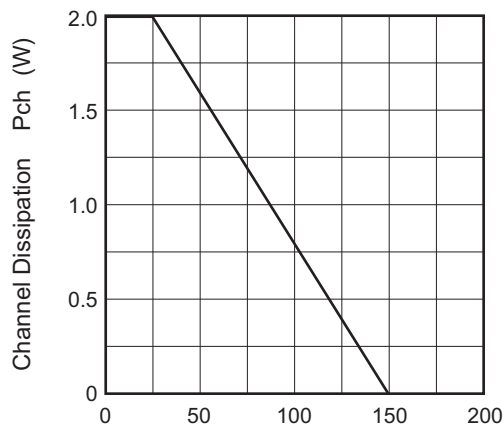
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -10 mA$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	$V_{GS} = \pm 12 V$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -20 V$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$I_D = -1 mA$, $V_{DS} = -10 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	55	65	mΩ	$I_D = -3 A$, $V_{GS} = -4.5 V$ ^{Note 4}
	$R_{DS(on)}$	—	85	110	mΩ	$I_D = -3 A$, $V_{GS} = -2.5 V$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	4	7	—	S	$I_D = -3 A$, $V_{DS} = -10 V$ ^{Note 4}
Input capacitance	C_{iss}	—	750	—	pF	$V_{DS} = -10 V$ $V_{GS} = 0$ $f = 1 MHz$
Output capacitance	C_{oss}	—	310	—	pF	
Reverse transfer capacitance	C_{rss}	—	220	—	pF	
Total gate charge	Q_g	—	11	—	nC	$V_{DD} = -10 V$ $V_{GS} = -4.5 V$ $I_D = -4.4 A$
Gate to source charge	Q_{gs}	—	2	—	nC	
Gate to drain charge	Q_{gd}	—	3.5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = -4.5 V$, $I_D = -3 A$, $R_L = 3.3 \Omega$
Rise time	t_r	—	100	—	ns	
Turn-off delay time	$t_{d(off)}$	—	85	—	ns	
Fall time	t_f	—	100	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.95	-1.23	V	$I_F = -4.4 A$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = -4.4 A$, $V_{GS} = 0$ $di_F/dt = -20 A/\mu s$

Note: 4. Pulse test

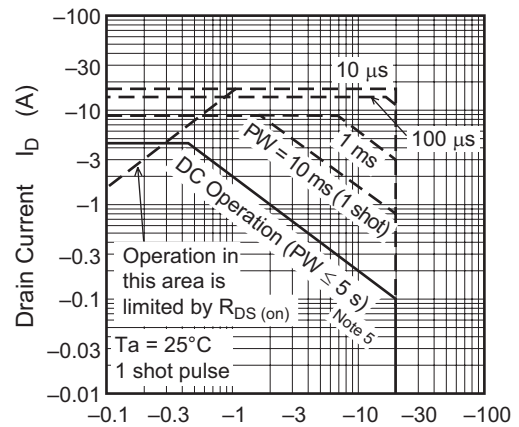
Main Characteristics

Power vs. Temperature Derating



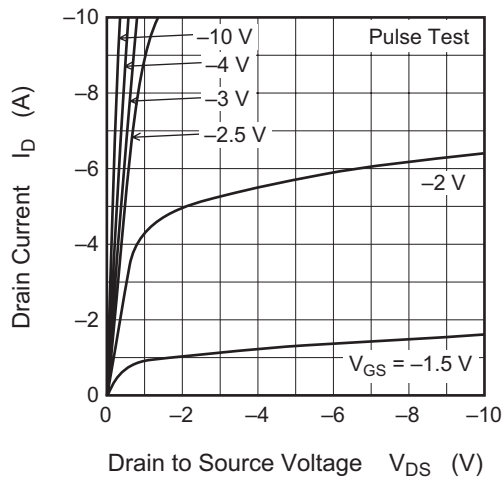
Ambient Temperature T_a (°C)
 Test Condition:
 When using the alumina ceramic board
 (50 × 50 × 0.7 mm), ($PW \leq 5$ s)

Maximum Safe Operation Area

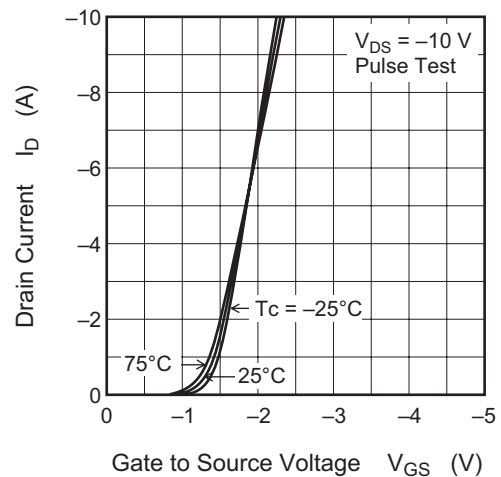


Drain to Source Voltage V_{DS} (V)
 Note 5:
 When using the alumina ceramic board
 (50 × 50 × 0.7 mm)

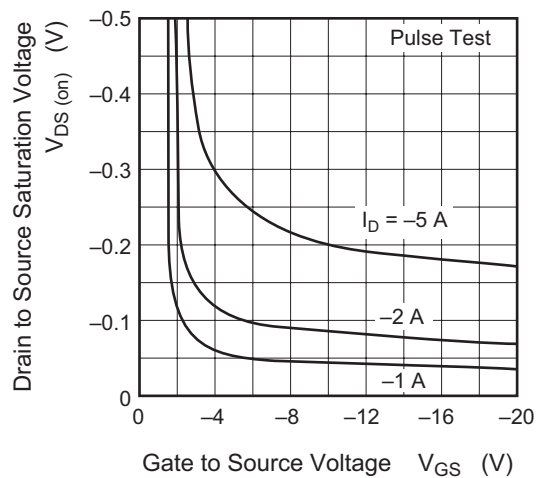
Typical Output Characteristics



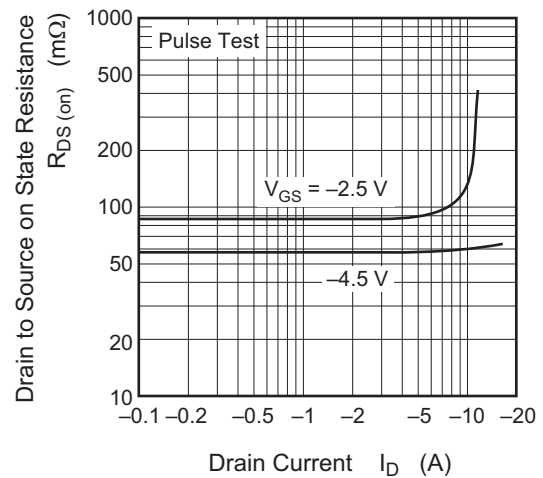
Typical Transfer Characteristics

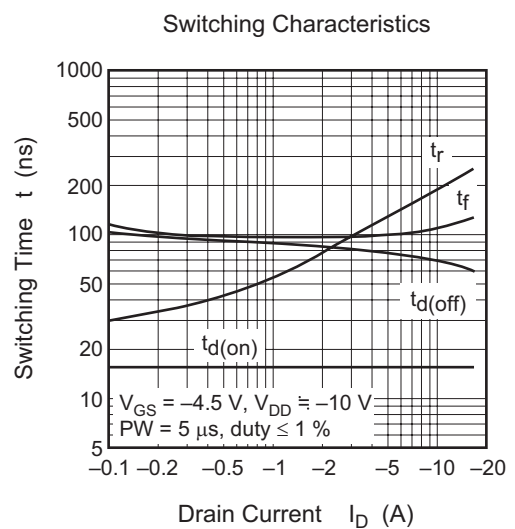
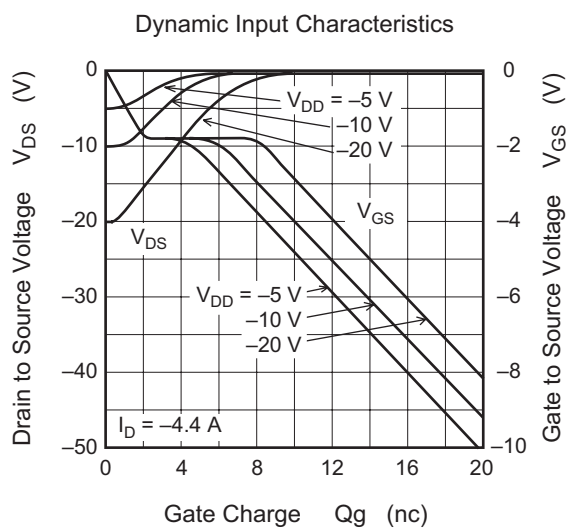
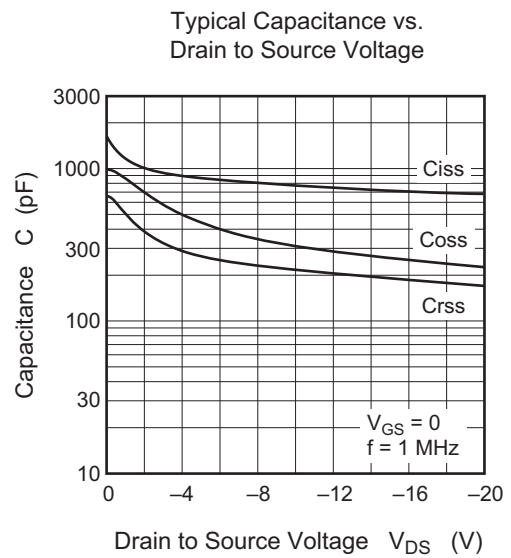
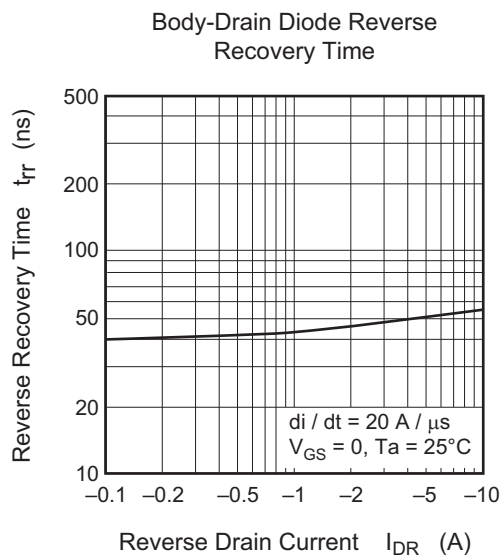
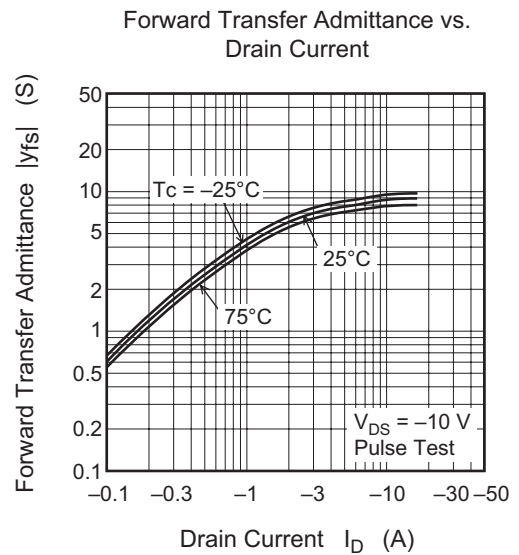
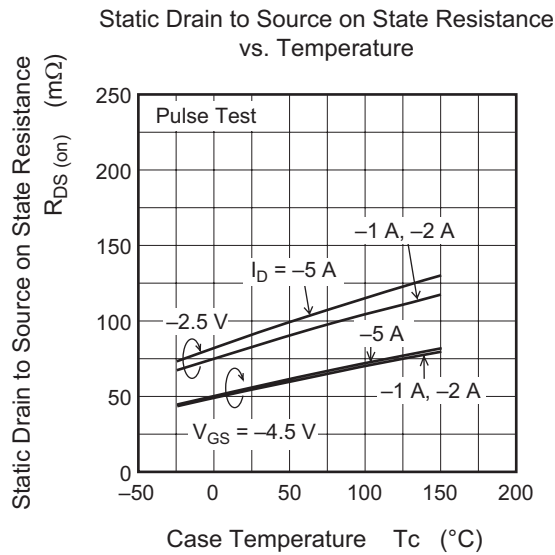


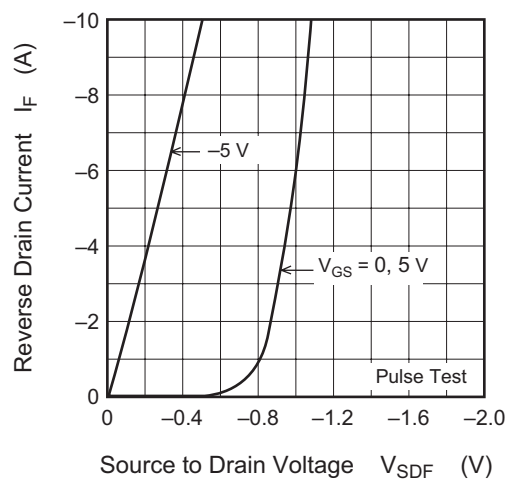
Drain to Source Saturation Voltage vs. Gate to Source Voltage



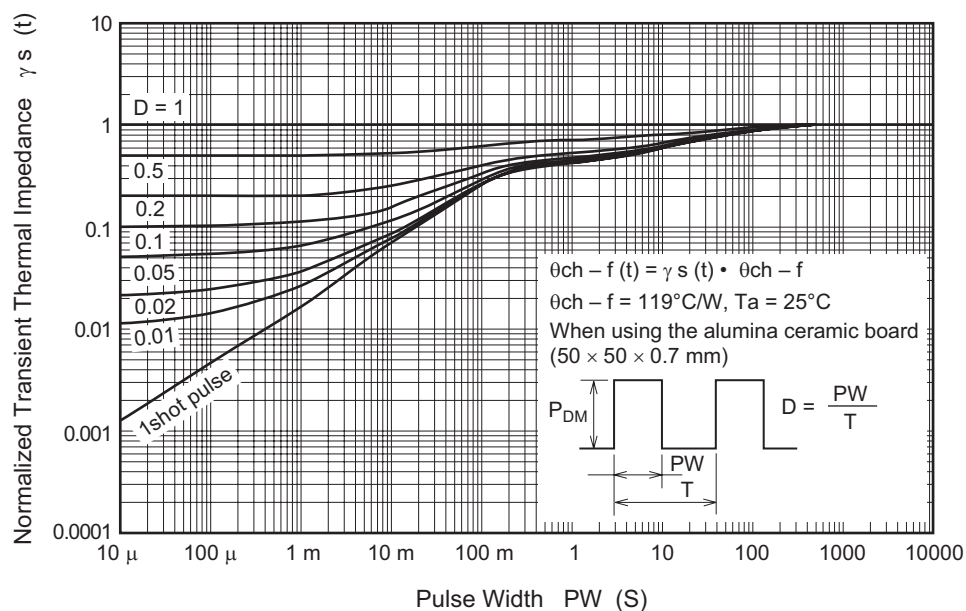
Static Drain to Source on State Resistance vs. Drain Current



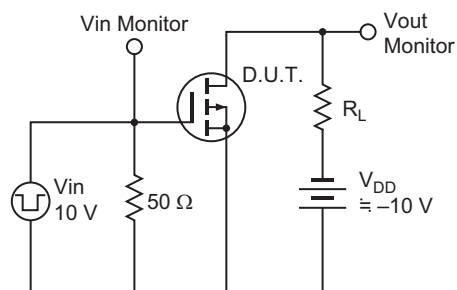


Reverse Drain Current vs.
Source to Drain Voltage

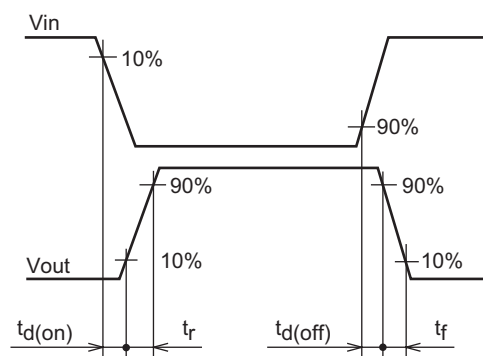
Normalized Transient Thermal Impedance vs. Pulse Width



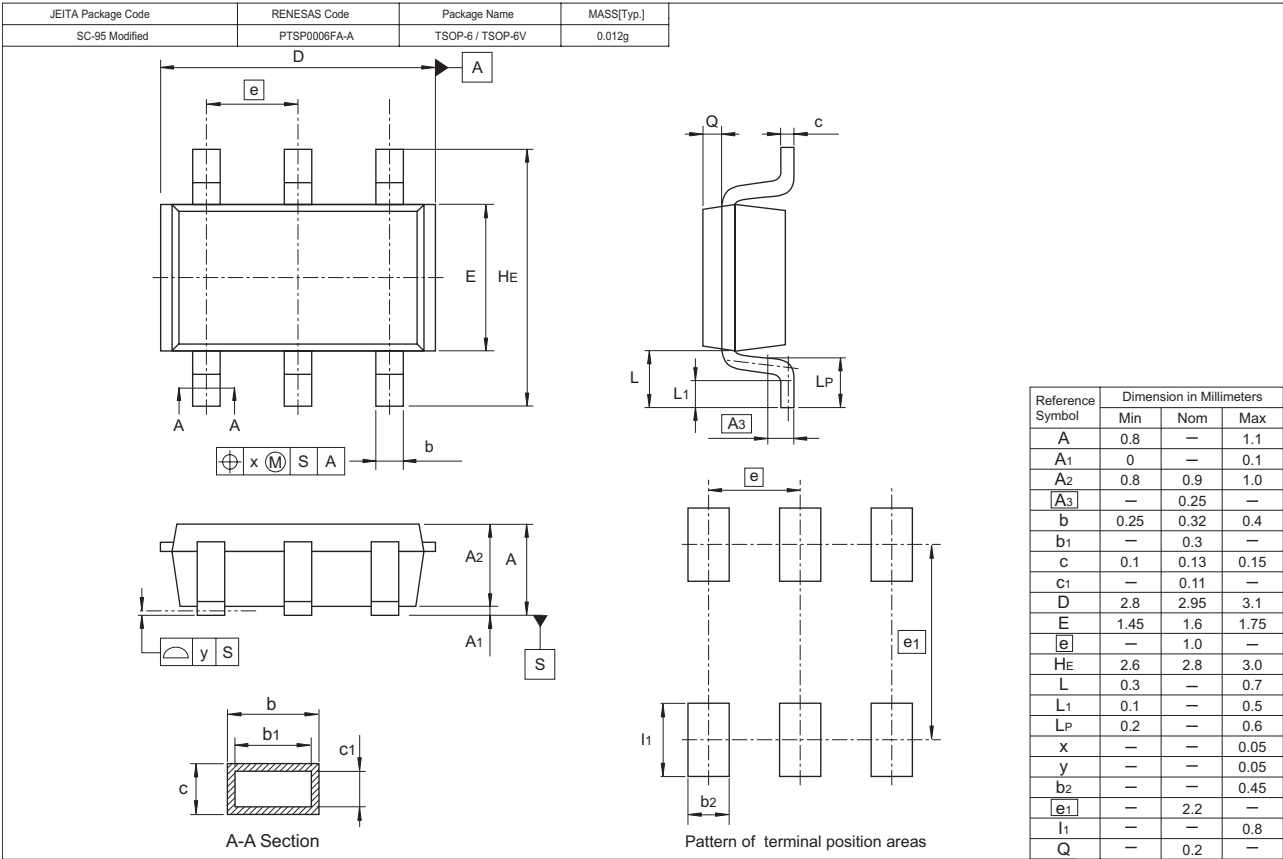
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAT1043M-EL-E	3000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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