

No.	AEC-Q200 Test Item	Specifications	AEC-Q200 Test Method
1	Pre-and Post-Stress Electrical Test	—	
2	High Temperature Exposure (Storage)	The measured and observed characteristics should satisfy the specifications in the following table.	Sit the capacitor for 1000±12 hours at 150±3°C. Let sit for 24±2 hours at room temperature, then measure.
	Appearance	No marking defects	
	Capacitance Change	Within ±2.5% or ±0.25pF (Whichever is larger)	
	Q	Q≥1000	
	I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)	
	Temperature Cycle	The measured and observed characteristics should satisfy the specifications in the following table.	Fix the capacitor to the supporting jig in the same manner and under the same conditions as (19). Perform the 1000 cycles according to the 4 heat treatments listed in the following table. Let sit for 24±2 hours at room temperature, then measure.
	Appearance	No marking defects	
	Capacitance Change	Within ±2.5% or ±0.25pF (Whichever is larger)	
Q	Q≥1000		
3	I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)	
4	Destructive Physical Analysis	No defects or abnormalities	Per EIA-469
5	Moisture Resistance	The measured and observed characteristics should satisfy the specifications in the following table.	Apply the 24 hour heat (25 to 65°C) and humidity (80 to 98%) treatment shown below, 10 consecutive times. Let sit for 24±2 hours at room temperature, then measure.
	Appearance	No marking defects	
	Capacitance Change	Within ±3.0% or ±0.3pF (Whichever is larger)	
	Q	Q≥350	
	I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)	
6	Biased Humidity	The measured and observed characteristics should satisfy the specifications in the following table.	Apply the rated voltage and DC1.3+0.2/-0V (add 6.8kΩ resistor) at 85±3°C and 80 to 85% humidity for 1000±12 hours. Remove and let sit for 24±2 hours at room temperature, then measure. The charge/discharge current is less than 50mA.
	Appearance	No marking defects	
	Capacitance Change	Within ±3.0% or ±0.3pF (Whichever is larger)	
	Q	Q≥200	
	I.R.	More than 1,000MΩ or 50MΩ · μF (Whichever is smaller)	
7	Operational Life	The measured and observed characteristics should satisfy the specifications in the following table.	Apply 120% of the rated voltage for 1000±12 hours at 125±3°C. Let sit for 24±2 hours at room temperature, then measure. The charge/discharge current is less than 50mA.
	Appearance	No marking defects	
	Capacitance Change	Within ±3.0% or ±0.3pF (Whichever is larger)	
	Q	Q≥350	
	I.R.	More than 1,000MΩ or 50MΩ · μF (Whichever is smaller)	
8	External Visual	No defects or abnormalities	Visual inspection
9	Physical Dimension	Within the specified dimensions	Using calipers

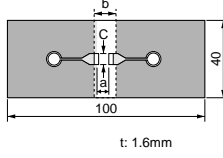
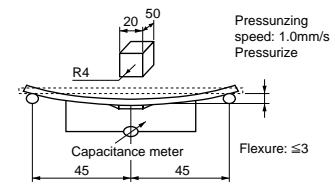
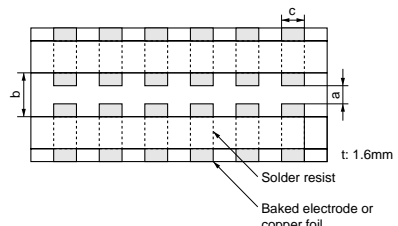
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No.	AEC-Q200 Test Item		Specifications	AEC-Q200 Test Method
10	Resistance to Solvents	Appearance	No marking defects	Per MIL-STD-202 Method 215 Solvent 1 : 1 part (by volume) of isopropyl alcohol 3 parts (by volume) of mineral spirits Solvent 2 : Terpene defluxer Solvent 3 : 42 parts (by volume) of water 1 part (by volume) of propylene glycol monomethylether 1 part (by volume) of monoethanolomine
		Capacitance Change	Within the specified tolerance	
		Q	$Q \geq 1000$	
		I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)	
11	Mechanical Shock	Appearance	No marking defects	Three shocks in each direction should be applied along 3 mutually perpendicular axes of the test specimen (18 shocks). The specified test pulse should be Half-sine and should have a duration : 0.5ms, peak value: 1500g and velocity change: 4.7m/s.
		Capacitance Change	Within the specified tolerance	
		Q	$Q \geq 1000$	
		I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)	
12	Vibration	Appearance	No defects or abnormalities	Solder the capacitor to the test jig (glass epoxy board) in the same manner and under the same conditions as (19). The capacitor should be subjected to a simple harmonic motion having a total amplitude of 1.5mm, the frequency being varied uniformly between the approximate limits of 10 and 2000Hz. The frequency range, from 10 to 2000Hz and return to 10Hz, should be traversed in approximately 20 minutes. This motion should be applied for 12 items in each 3 mutually perpendicular directions (total of 36 times).
		Capacitance Change	Within the specified tolerance	
		Q	$Q \geq 1000$	
		I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)	
13	Resistance to Soldering Heat		The measured and observed characteristics should satisfy the specifications in the following table.	Immerse the capacitor in a eutectic solder solution at 260±5°C for 10±1 seconds. Let sit at room temperature for 24±2 hours, then measure.
	Appearance	No marking defects		
	Capacitance Change	Within the specified tolerance		
	Q	$Q \geq 1000$		
	I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)		
14	Thermal Shock		The measured and observed characteristics should satisfy the specifications in the following table.	Fix the capacitor to the supporting jig in the same manner and under the same conditions as (19). Perform the 300 cycles according to the two heat treatments listed in the following table (Maximum transfer time is 20 seconds). Let sit for 24±2 hours at room temperature, then measure.
	Appearance	No marking defects		
	Capacitance Change	Within ±2.5% or ±0.25pF (Whichever is larger)		
	Q	$Q \geq 1000$		
	I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)		
15	ESD	Appearance	No marking defects	Per AEC-Q200-004
		Capacitance Change	Within the specified tolerance	
		Q	$Q \geq 1000$	
		I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)	
16	Solderability		95% of the terminations is to be soldered evenly and continuously.	(a) Preheat at 155°C for 4 hours. After preheating, immerse the capacitor in a solution of ethanol (JIS-K-8101) and rosin (JIS-K-5902) (25% rosin in weight proportion). Immerse in eutectic solder solution for 5+0/-0.5 seconds at 235±5°C.
				(b) Should be placed into steam aging for 8 hours±15 minutes. After preheating, immerse the capacitor in a solution of ethanol (JIS-K-8101) and rosin (JIS-K-5902) (25% rosin in weight proportion). Immerse in eutectic solder solution for 5+0/-0.5 seconds at 235±5°C.
				(c) Should be placed into steam aging for 8 hours±15 minutes. After preheating, immerse the capacitor in a solution of ethanol (JIS-K-8101) and rosin (JIS-K-5902) (25% rosin in weight proportion). Immerse in eutectic solder solution for 120 ±5 seconds at 260±5°C.

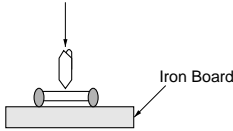
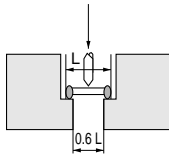
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No.	AEC-Q200 Test Item	Specifications	AEC-Q200 Test Method
17	Electrical Characterization	Appearance	No defects or abnormalities
		Capacitance Change	Within the specified tolerance
		Q	$Q \geq 1000$
		I.R.	<p>25°C More than 100,000MΩ or 1,000MΩ · μF (Whichever is smaller)</p> <p>Max. Operating Temperature...125°C More than 10,000MΩ or 100MΩ · μF (Whichever is smaller)</p>
		Dielectric Strength	No failure
18	Board Flex	Appearance	No marking defects
		Capacitance Change	Within ±5.0% or ±0.5pF (Whichever is larger)
		Q	$Q \geq 1000$
		I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)
			 <p>Fig. 1</p>
19	Terminal Strength	Appearance	No marking defects
		Capacitance Change	Within the specified tolerance
		Q	$Q \geq 1000$
		I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)
			 <p>Fig. 2</p>
19	Terminal Strength	Appearance	No marking defects
		Capacitance Change	Within the specified tolerance
		Q	$Q \geq 1000$
		I.R.	More than 10,000MΩ or 500MΩ · μF (Whichever is smaller)
			 <p>Fig. 3</p>

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No.	AEC-Q200 Test Item		Specifications	AEC-Q200 Test Method												
20	Beam Load Test		<p>The chip endure following force.</p> <p>< Chip L dimension : 2.5mm max. > Chip thickness > 0.5mm rank : 20N Chip thickness ≤ 0.5mm rank : 8N</p> <p>< Chip L dimension : 3.2mm min. > Chip thickness < 1.25mm rank : 15N Chip thickness ≥ 1.25mm rank : 54.5N</p>	<p>Place the capacitor in the beam load fixture as Fig. 4. Apply a force. < Chip L dimension: 2.5mm max. ></p>  <p>< Chip L dimension: 3.2mm min. ></p>  <p>Fig. 4</p> <p>Speed supplied the Stress Load : 2.5mm / s</p>												
	21	Capacitance Temperature Characteristics	Capacitance Change	<p>-750±120 ppm/°C (Temp. Range: +25 to +125°C) -750±120, -347 ppm/°C (Temp. Range: -55 to +25°C)</p>	<p>The capacitance change should be measured after 5 min. at each specified temperature stage. The temperature coefficient is determined using the capacitance measured in step 3 as a reference. When cycling the temperature sequentially from step1 through 5 the capacitance should be within the specified tolerance for the temperature coefficient. The capacitance drift is calculated by dividing the differences between the maximum and minimum measured values in steps 1, 3 and 5 by the capacitance value in step 3.</p> <table><tr><th>Step</th><th>Temperature (°C)</th></tr><tr><td>1</td><td>25±2</td></tr><tr><td>2</td><td>-55±3</td></tr><tr><td>3</td><td>25±2</td></tr><tr><td>4</td><td>125±3</td></tr><tr><td>5</td><td>25±2</td></tr></table>	Step	Temperature (°C)	1	25±2	2	-55±3	3	25±2	4	125±3	5
Step			Temperature (°C)													
1	25±2															
2	-55±3															
3	25±2															
4	125±3															
5	25±2															
		Capacitance Drift	<p>Within ±0.2% or ±0.05 pF (Whichever is larger)</p>													