To: Digi-Key	Issue No. :	EZJ08090102
	Date of Issue:	September 01.2008
	Classification:	■ New □ Changed □

PRODUCT SPECIFICATION FOR APPROVAL

Product Description : Multilayer Varistor Chip Type

Product Part Number : EZJZ0V80015D / EZJZ0V500AA [EIA:0402]

EZJZ1V500AA / EZJZ1V800AA [EIA:0603] EZJZ1V270EA / EZJZ1V270RA [EIA:0603]

Customers Part Number :

Country of Origin : Japan

Applications : Consumer Type Electric Equipment

Prepared by : Engineering Section

Capacitor Business Unit Phone: +81-123-23-8149 (Direct)

Panasonic Electronic Devices Co.,Ltd. Fax : +81-123-22-4191 (Direct)

25.Kohata-nishinaka..Uji City , Kyoto, Japan

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Title : Engineer

Phone: +81-774-32-1111(Representative)

Authorized by : Y. Sakaguchi

Title: Manager of Engineering

If there is a question, please ask the engineering section about it directly.



CLASSIFICA	SPECIFICATIONS	No. 151S-EZJ-SZB028E
SUBJECT	Multilayer Varistor, Chip Type EIA:0402size Individual Specification	PAGE 1 of 1
	EZJZ0V80015D	DATE 5 June, 2006

This specification applies to Multilayer Varistor, Chip Type EZJZ series, size 0402(EIA).

2. Style and Dimensions

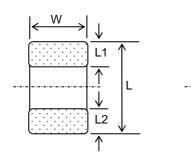
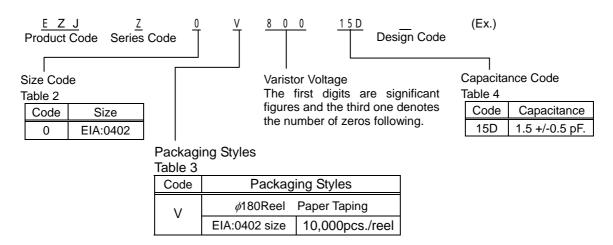


Table 1	
Symbol	Dimensions(mm)
L	1.00 +/- 0.05
W	0.50 +/- 0.05
Т	0.50 +/- 0.05
L1,L2	0.2 +/- 0.1

3. Operating Temperature Range / Storage Temperature Range

- 40 to 85 °C

4. Explanation of Part Numbers



5. Part Number and Individual Specification

Part Number	Maximum Allowable Voltage	Varistor Voltage at 1mA	Capacitance at 1MHz	Maximum ESD IEC61000-4-2
EZJZ0V80015D	DC 5 V	64 ~ 96 V	1.5 +/- 0.5 pF.	8kV

	APPROVAL	CHECK	DESIGN
Panasonic Electronic Devices Co., Ltd.	Y.Sakaguti	T.Kawamura	Y.Sasaki

CLASSIFICA	SPECIFIC	CATIONS		No. 151S-EZJ-SZB029E
SUBJECT	Multilayer Varistor, Chip Type	EIA:0402size	Individual Specification	PAGE 1 of 1
	EZJZ0V500AA		DATE 5 June, 2006	

This specification applies to Multilayer Varistor, Chip Type EZJZ series, size 0402(EIA).

2. Style and Dimensions

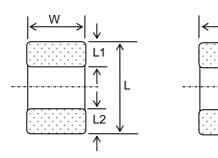
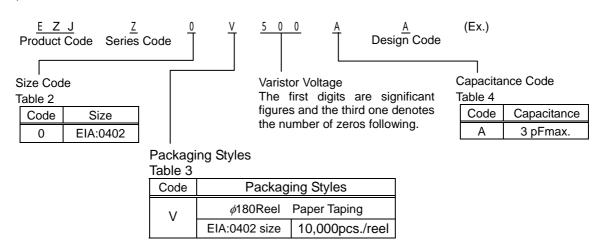


Table 1	
Symbol	Dimensions(mm)
L	1.00 +/- 0.05
W	0.50 +/- 0.05
Т	0.50 +/- 0.05
1112	0.2 +/- 0.1

3. Operating Temperature Range / Storage Temperature Range

- 40 to 85 °C

4. Explanation of Part Numbers



5. Part Number and Individual Specification

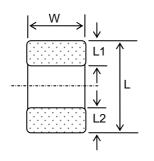
Part Number	Maximum Allowable Voltage	Varistor Voltage at 1mA	Capacitance at 1MHz	Maximum ESD IEC61000-4-2
EZJZ0V500AA	DC 5 V	40 ~ 60 V	3 pFmax.	8kV

	APPROVAL	CHECK	DESIGN
Panasonic Electronic Devices Co., Ltd.	Y.Sakaguti	T.Kawamura	Y.Sasaki

CLASSIFICAT	TION SPECIFICATIONS	No. 151S-EZJ-SZC030E
SUBJECT	Multilayer Varistor, Chip Type EIA:0603size Individual Specif	ication PAGE 1 of 1
	EZJZ1V500AA	

This specification applies to Multilayer Varistor, Chip Type EZJZ series, size 0603(EIA).

2. Style and Dimensions



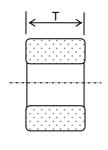


Table 1	
Symbol	Dimensions(mm)
L	1.6 +/- 0.1
W	0.8 +/- 0.1
Т	0.8 +/- 0.1
L1,L2	0.3 +/- 0.2

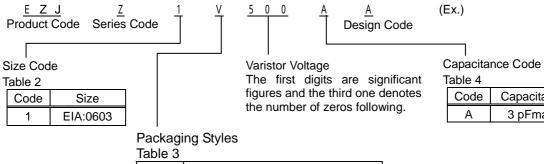
Capacitance

3 pFmax.

3. Operating Temperature Range / Storage Temperature Range

-40 to 85 °C

4. Explanation of Part Numbers



Code	Packaging Styles	
V	<i>∮</i> 180Reel	Paper Taping
V	EIA:0603 size	4,000pcs./reel

5. Part Number and Individual Specification

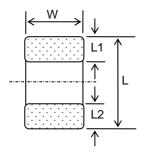
Part Number	Maximum Allowable Voltage	Varistor Voltage at 1mA	Capacitance at 1MHz	Maximum ESD IEC61000-4-2
EZJZ1V500AA	DC 5 V	40 ~ 60 V	3 pFmax.	8 kV

	APPROVAL	CHECK	DESIGN
Panasonic Electronic Devices Co., Ltd.	Y.Sakaguti	T.Kawamura	Y.Sasaki

CLASSIFICA	TION SPECIFI	CATIONS	No. 151S-EZJ-SZC031E	
SUBJECT	Multilayer Varistor, Chip Type	EIA:0603size	Individual Specification	PAGE 1 of 1
	EZJZ1V800AA			DATE 5 June, 2006

This specification applies to Multilayer Varistor, Chip Type EZJZ series, size 0603(EIA).

2. Style and Dimensions



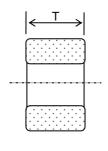
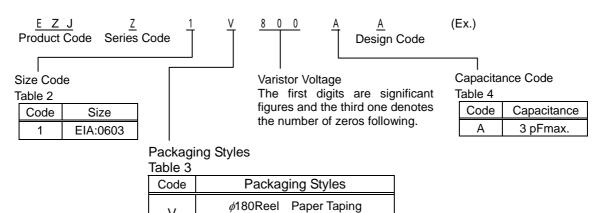


Table 1	
Symbol Dimensions(mm	
L	1.6 +/- 0.1
W	0.8 +/- 0.1
Т	0.8 +/- 0.1
L1,L2	0.3 +/- 0.2

3. Operating Temperature Range / Storage Temperature Range

- 40 to 85 °C

4. Explanation of Part Numbers



EIA:0603 size

5. Part Number and Individual Specification

Part Number	Maximum Allowable Voltage	Varistor Voltage at 1mA	Capacitance at 1MHz	Maximum ESD IEC61000-4-2
EZJZ1V800AA	DC 18 V	64 ~ 96 V	3 pFmax.	8 kV

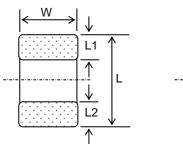
4,000pcs./reel

	APPROVAL	CHECK	DESIGN
Panasonic Electronic Devices Co., Ltd.	Y.Sakaguti	T.Kawamura	Y.Sasaki

CLASSIFICAT	TION SPECIFICA	TIONS		No. 151S-EZJ-SZC025E
SUBJECT	Multilayer Varistor, Chip Type El	IA:0603size	Individual Specification	PAGE 1 of 1
	EZJZ1V270EA		DATE 5 June, 2006	

This specification applies to Multilayer Varistor, Chip Type EZJZ series, size 0603(EIA).

2. Style and Dimensions



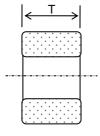
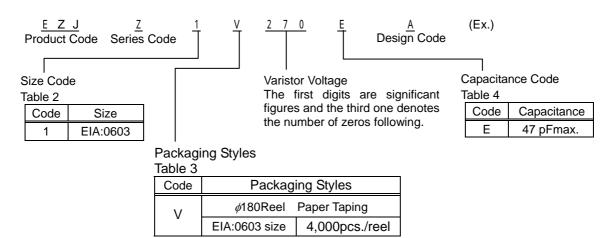


Table 1	
Symbol	Dimensions(mm)
L	1.6 +/- 0.1
W	0.8 +/- 0.1
Т	0.8 +/- 0.1
L1,L2	0.3 +/- 0.2

3. Operating Temperature Range / Storage Temperature Range

- 40 to 85 °C

4. Explanation of Part Numbers



5. Part Number and Individual Specification

Part Number	Maximum Allowable Voltage	Varistor Voltage at 1mA	Capacitance at 1MHz	Clamping Voltage at 8/20us,2A	Maximum Peak Current at 8/20us
EZJZ1V270EA	DC 16 V	25.4 ~ 30.8 V	47 pFmax.	56 Vmax.	20 A

	APPROVAL	CHECK	DESIGN
Panasonic Electronic Devices Co., Ltd.	Y.Sakaguti	T.Kawamura	Y.Sasaki

CLASSIFICAT	FION SPECIFICATIONS	No. 151S-EZJ-SZC026E
SUBJECT	Multilayer Varistor, Chip Type EIA:0603size Individual Specification	PAGE 1 of 1
	EZJZ1V270RA	DATE 5 June, 2006

This specification applies to Multilayer Varistor, Chip Type EZJZ series, size 0603(EIA).

2. Style and Dimensions

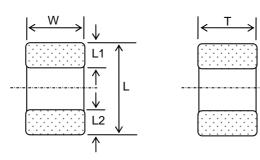
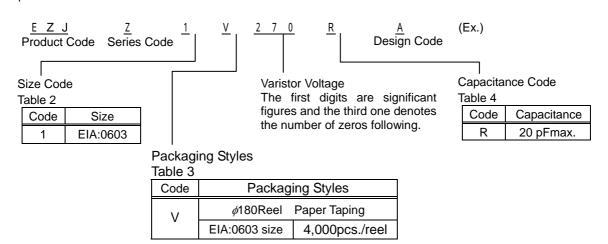


Table 1	
Symbol	Dimensions(mm)
L	1.6 +/- 0.1
W	0.8 +/- 0.1
Т	0.8 +/- 0.1
L1,L2	0.3 +/- 0.2

3. Operating Temperature Range / Storage Temperature Range

- 40 to 85 °C

4. Explanation of Part Numbers



5. Part Number and Individual Specification

Part Number	Maximum Allowable Voltage	Varistor Voltage at 1mA	Capacitance at 1MHz	Clamping Voltage at 8/20us,2A	Maximum Peak Current at 8/20us
EZJZ1V270RA	DC 16 V	25.4 ~ 30.8 V	20 pFmax.	50 Vmax.	3 A

	APPROVAL	CHECK	DESIGN
Panasonic Electronic Devices Co., Ltd.	Y.Sakaguti	T.Kawamura	Y.Sasaki

CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SZPG001E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 1 of 5
	Common Specification(EZJZ, EZJP Series)	DATE 1 Apr, 2008

1. Information

- 1- 1. Applicable laws and regulations
 - (1) Any ozone-depleting substances listed in the Montreal Protocol are not used in the manufacturing processes for parts and materials used in this product.
 - (2) PBB and PBDE are intentionally excluded from materials used in this product.
 - (3) All the materials used in this product are registered materials under the Law Concerning Examination and Regulation of Manufacture and Handling of Chemical Substances.
 - (4) This product complies with the RoHS, DIRECTIVE 2002/95/EC on the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment.
 - (5) This product is exported with export procedures under export related laws and regulations such as the Foreign Exchange and Foreign Trade Law.

1-2.Limitation in Applications

This product was designed and manufactured for general-purpose electronic equipment such as household, office, information & communication equipment. When the following applications, which are required higher reliability and safety because the trouble or malfunction of this product may threaten the lives and/or properties, are examined, separate specifications suitable for the application should be exchanged.

•Aerospace / Aircraft equipment, Warning / Antitheft equipment, Medical equipment, Transport equipment (Motor vehicles, Trains, Ship and Vessel), Highly public information processing equipment, Others equivalent to the above.

1-3. Production factory

- (1) Panasonic Electronic Devices Japan Co., Ltd.
- (2) Panasonic Electronic Devices (Tianjin) Co., Ltd. (PEDTJ)

2. Scope

- 2-1. This specification applies common specification to multilayer varistor/chip type . If there is a difference between this common specification and any individual specifications, priority shall be given to the individual specifications.
- 2- 2. This product shall be used for general-purpose electronic equipment such as audiovisual, household, office, information & communication equipment.

Unreasonable applications may accelerate performance deterioration or short/open circuits as failure modes affecting the life end. Adequate safety shall be ensured especially for product design required a high level of safety with the following considerations.

- 1) Previously examine how a single trouble in this product affects the end product.
- 2) Design a protection circuit as Failsafe-design to avoid unsafe system resulting from a single trouble with this product.

Whenever a doubt about safety arises from this product, immediately inform us for technical consultation without fail, please.

2- 3. This specification is a part of contract documents pertaining to the trade made by and between your company and Matsushita Electric Industrial Co., Ltd.

3. Part Number Code

3-1.Common Code (1)

EZJ: Multilayer Varistor, Chip Type

3-2.Series Code(2)

Z:EZJZ series , P:EZJP series

3-3.Size Code(3)

0:0402(EIA) 1:0603(EIA)

3-4.Packaging Styles Code(4)

Shown in Individual Specification.

3-5. Varistor voltage (5)

The first two digits are significant figures and third one denotes the number of zeros following.

	Note ;			
r		APPROVAL	CHECK	DESIGN
	Panasonic Electronic Devices Co., Ltd.	T.Kawamura	Y.Sasaki	Y.Sasaki

CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SZPG001E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 2 of 5
	Common Specification(EZJZ Series)	DATE 1 Apr, 2008

3-6.Capacitance Code (6)

A:3 pF R:20 pF D:27 pF E:47 pF W:56 pF F:68 pF

G:100 pF H:150 pF J:220 pF K:330 pF M: 680 pF

 $\ensuremath{\ensuremath{\mathbb{X}}}$ 3 pF or less are displayed a top 2 figures using 10 or 11 figures.

For example 2.0 pF: 20 1.5 pF: 15

3-7.Design Code (7)

A specific code shall be given for identification as individual specification or design ranking if necessary.

3-8.Special Code(8)

A specific code shall be given for identification as individual specification or design ranking if necessary.

None	Capacitance Tolerance : max.
В	Capacitance Tolerance : +/- 0.10 pF
С	Capacitance Tolerance : +/- 0.25 pF
D	Capacitance Tolerance : +/- 0.50 pF
K	Capacitance Tolerance : +/- 10 %
М	Capacitance Tolerance : +/- 20 %

4. Operating Temperature Range / Storage Temperature Range Shown in Individual Specification.

5. Test

Unless otherwise specified, all tests and measurements shall be made at a temperature of 15 to 35°C and at a relative humidity of 45 to 75%.

If results obtained are doubted, a further test should be carried out at a temperature of 25 +/- 2° C and a relative humidity of 60 to 70%.

6. Structure

The structure shall be in a monolithic form as shown in Fig.1.

Fig.1

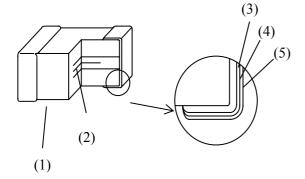


Table 1

No.	Name			
(1)	Se	miconductive Ceramics		
(2)		EZJZ series : Ag/Pd or Pt EZJP series : Pd		
(3)		Substrate Electrode (Ag)		
(4)	Terminal Electrode	Intermediate Electrode (Ni)		
(5)		External Electrode (Sn)		

L/ (O	SIFICATION		SPECIFICATIONS		No. 151S-EZJ-SZPG001
SUBJECT Multilayer Varistor , Chip Type			ultilayer Varistor , Chip Type		PAGE 3 of 5
Comr		Comr	mon Specification(EZJZ Series)		DATE 1 Apr, 2008
			Table 2		
No Contents		nts	Performance	Test	Method
1	Appearance		There shall be no defects which affect the life and use.		
2	Dimensions		Shown in Individual Specification.	With slide calipers and	d a micrometer.
3	Maximum allowable volta	age	Shown in Individual Specification.		Itage that can be applie specified operating tem
4	Varistor voltag	le	Shown in Individual Specification.	specified measuring is called Vc or Vc mA	n two terminals with the current CmA DC applie a. The measurement shappossible to avoid heat a
5	Capacitance		Shown in Individual Specification.	Measuring Frequency	Measuring Voltage
				1 MHz +/-10 %	1.0 +/-0.5 Vrms
				Our Measurement ins Table 3	strument is shown in th
6	Clamping volta	age	Shown in Individual Specification.	The maximum voltage between two termin with the specified impulse current(8/20 us).	
7	Maximum peak current		Shown in Individual Specification.	The maximum current at less than +/-10 % varistor voltage change when impulse current(8/20 us) is applied two times continuous with the interval of 5 minutes.	
8	Maximum ESD		Shown in Individual Specification.	The maximum ESD within the varistor volta change of +/-30 % when impressing 10 tim of ESD(five times of positive-negative for ea polarity) which is based on IEC61000-4-2.	
9	Bending Appearanc e		There shall be no cracks and other mechanical damage.	mm of bending shall be Bending speed: 1 mm (shown in Fig. 2)	citor on the substrate be applied for 5 seconds. n/s
				45±2 45	5±2 Unit:mm
10	0 Solderability		More than 75 % of the soldered area of both terminal electrodes shall be covered with fresh solder.	nal electrodes are cor Use solder H63A(JIS- rosin (JIS-K-5902) o concentration of abou	s solder so that both term npletely submerged. Z-3282). For the flux use f ethanol solution of a
			(continue)		

CLASSIFICATIO	N	No. 151S-EZJ-S2	ZPG001E			
SUBJECT	Multilayer Varistor , Chip Type					
	DATE 1 Apr,	2008				
Table 2						
No C	Contents Performance Test Method					
44 D		-	0 11 1 070.15.00			

			Table 2	,	
No	Contents Po		Performance	Test Method	
11	Resistance to solder heat	Appear- ance Varistor voltage	There shall be no cracks and other mechanical damage. dVc/Vc: Within +/- 10.0 %	Solder temperature: 270+/-5 °C Dipping period: 3 +/-1 s Dipping position: Up to the positioin in which both terminal hides completely.	
		voltage		Order Temperature(°C) Period (S)	
				1 80 to 100 120 to 180	
				2 150 to 200 120 to 180	
12	Tempera-	Appear-	There shall be no cracks and other	Use solder H63A(JIS-Z-3282). For the flux use rosin (JIS-K-5902) of ethanol solution of a concentration of about 25 % by weight. Use tweezers for the holder to dip the specimen. Solder the specimen to the testing jig shown	
	ture cycle	ance	mechanical damage.	in Fig.1. Condition the specimen to each tem-	
		Varistor voltage	dVc/Vc: Within +/- 10.0 %	perature from step 1 to 4 in this order for the period shown in the table below. Regarding this conditioning as one cycle, per form 5 cycles continuously.	
				Step Temperature Period (°C) (min.)	
				1 Minimum operation temperature +/- 3 30 +/-3	
				2 Room temperature 3 max.	
				3 Maximum operation temperature +/-5 30 +/-3	
				4 Room temperature 3 max.	
13	Damp Heat Laod (Moisture Resistant Loading)	Appear- ance Varistor voltage	There shall be no cracks and other mechanical damage. dVc/Vc : Within +/- 10.0 %	The specimen shall be subjected to specified conditions and then stored at room temperature and normal humidity for 1 to 2 hours. Thereafter,the change of V shall be measured. Test temperature: 40 +/-2 °C Relative humidity: 90 to 95 % Laod: Maximum allowable voltage Test period: 500 +24/0 h	
14	High Temperature Laod (High Tem-	Appear- ance Varistor voltage	There shall be no cracks and other mechanical damage. dVc/Vc: Within +/- 10.0 %	The specimen shall be subjected to specified conditions and then stored at room temperature and normal humidity for 1 to 2 hours. Thereafter,the change of V shall be measured. Test temperature: 85 +/-3 °C	
	perature Resistant Loading)			Laod : Maximum allowable voltage Test period : 500 +24/0 h	

Note ;			

CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SZPG001E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 5 of 5
	Common Specification(EZJZ Series)	DATE 1 Apr, 2008

When uncertainty occurs in the weather resistance characteristic tests (temperature cycle, moisture resistance, moisture resistant loading, high temperature resistant loading), the same tests shall be performed for the capacitor itself.

Table 3

	Our Measurement instrument
Measuring Instrument	4278A 1kHz/1MHz Capacitance Meter (Agilent Technologies)
Measuring mode	Parallel Mode
Recommended measuring jig	16034E Test Fixture (Agilent Technologies)

Fig. 1 Testing jig

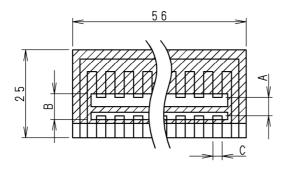


 Table 4

 Size (EIA)
 A
 B
 C

 0402
 0.5
 1.5
 0.6

 0603
 1.0
 3.0
 1.2

Unit : mm

Material: Glass epoxy board

Thickness: 1.6mm

:Copper foil (0.035mm thick)

:Solder resist

Fia. 2 Testing jig

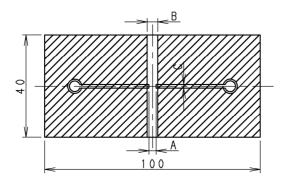


Table 5				
Type (EIA)	Α	В	С	Board Thick ness
0402	0.5	1.5	0.6	0.6
0603	1.0	3.0	1.2	1.6

Unit: mm

Material: Glass epoxy board

:Copper foil (0.035mm thick)

:Solder resist

CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SCS004E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 1 of 8
	Common Specification (Precautions for Use)	DATE 1 Apr, 2008

1. Precautions for Use

Multilayer Varistors (hereafter referred to as "Varistors") should be used for general purpose applications as countermeasures against ESD and noise found in consumer electronics (audio/visual, home, office, information & communication) equipment.

When subjected to severe electrical, environmental, and/or mechanical stress beyond the specifications, as noted in the Ratings and Conditions section, the Varistor may fail in a short circuit mode or in an open-circuit mode. This case results in a burn-out, smoke or flaming.

For products which require high safety levels, please carefully consider how a single malfunction can affect your product. In order to ensure the safety in the case of a single malfunction, please design products with fail-safe, such as setting up protecting circuits, etc.

2. Operating Conditions and Circuit Design

2- 1.Circuit Design

2-1-1. Operating Temperature and Storage Temperature

The specified "Operating Temperature Range" found in the Specification is the absolute maximum and minimum temperature rating. Every Varistor shall be operated within the specified "Operating Temperature Range". The Varistors mounted on PCB shall be stored without operating within the specified "Storage Temperature Range" in the Specifications.

2-1-2. Operating Voltage

The Varistors shall not be operated in excess of the "Maximum Allowable Voltage".

If the Varistors are operated beyond the specified Maximum allowable voltage, it may cause short and/or damage due to thermal run away.

When high frequency and steep pulse voltages are continuously used, even when less than the Maximum allowable voltage, in a circuit, please examine the reliability of the Varistor while also checking the safety and reliability of your circuit.

2-1-3. Self-heating

The surface temperature of the Varistors shall be under the specified Maximum Operating Temperature in the Specifications including the temperature rise caused by self-heating. Check temperature rise of the Varistor in your circuit.

2-1-4. Environmental Restrictions

The Varistors shall not be operated and/or stored under the following conditions.

- (1) Environmental conditions
 - (a) Under direct exposure to water or salt water.
 - (b) Under conditions where water can condense and/or dew can form.
 - (c) Under conditions containing corrosive gases such as hydrogen sulfide, sulfurous acid, chlorine and ammonia.
- (2) Mechanical conditions

Under severe conditions of vibration or impact beyond the specified conditions found in the Specifications.

Note ;				
		APPROVAL	CHECK	DESIGN
	Panasonic Electronic Devices Co., Ltd.	T.Kawamura	Y.Sasaki	Y.Sasaki
			<u>!</u>	-1

CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SCS004E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 2 of 8
	Common Specification (Precautions for Use)	DATE 1 Apr, 2008

2- 2.Design of Printed Circuit Board

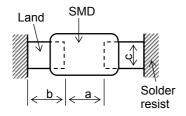
2-2-1. Selection of Printed Circuit Board

When the Varistors are mounted and soldered on an "Alumina Substrate", the substrate has influences the Varistor's reliability against "Temperature Cycles" and "Heat shock" due to the difference in the thermal expansion coefficient between them. Confirm that the actual board used does not deteriorate the characteristics of the Varistors.

2-2-2. Design of Land Pattern

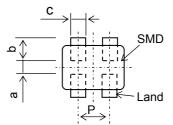
(1) Recommended land dimensions are shown below. Use the proper amount of solder in order to prevent cracking. Using too much solder places excessive stress on the Varistors.

{ Recommended land dimensions (Ex.) }



						Offic . Hilli
Size Code		Comp Dime	onent nsion	а	b	С
(EIA)	L	W	T			
0[0402]	1.0	0.5	0.5	0.4 to 0.5	0.4 to 0.5	0.4 to 0.5
1[0603]	1.6	8.0	0.8	0.8 to 1.0	0.6 to 0.8	0.6 to 0.8
2[0805]	2.0	1.25	0.8 to 1.25	0.8 to 1.2	0.8 to 1.0	0.8 to 1.0

I Init · mm



							Unit : mm
Size Code	Component Dimension		а	b	С	Р	
Code	L	W	Т				
S	1.37	1.0	0.6	0.3	0.45	0.3	0.54
(0504/2 array)	1.37	1.0	0.0	to 0.4	to 0.55	to 0.4	to 0.74

(2) The size of lands shall be designed to have equal spacing between the right and left sides. If the amount of solder on the right land is different from that on the left land, the component may be cracked by stress since the side with a larger amount of solder solidifies later during cooling.

Recommended Amount of Solder

- (a) Excessive amount
- (b) Proper amount
- (c)Insufficient amount







2-2-3. Utilizatoin of Solder Resist

- (1) Solder resist shall be utilized to equalize the amounts of solder on both sides.
- (2) Solder resist shall be used to divide the pattern for the following cases;
 - ·Components are arranged closely.
 - ·The Varistor is mounted near a component with lead wires.
 - ·The Varistor is placed near a chassis.

See the table below.

note

CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SCS004E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 3 of 8
	Common Specification (Precautions for Use)	DATE 1 Apr, 2008

Prohibited Applications and Recommended Applications Item Prohibited applications Improved applications by pattern division The lead wire of Solder resist Mixed mounting a component with with a component with lead wires lead wires Sectional view Sectional view Chassis Solder resist ✓ Solder (ground solder) Arrangement near chassis Sectional view Sectional view Soldering iron A lead wire of Solder resist Retro-fitting of Retrofitted component with lead component wires Sectional view Sectional view Land Portion to be Solder resist excessively Lateral arrangement soldered

2-2-4. Component Layout

The Varistors / components shall be placed on the PC board such that both electrodes are subjected to uniform stresses, or to position the component electrodes at right angles to the grid glove or bending line. This should be done to avoid cracking the Varistors from bending the PC board after or during placing/mounting on the PC board.

(1) To minimize mechanical stress caused by the warp or bending of a PC board, please follow the recommended Varistor's layout below.

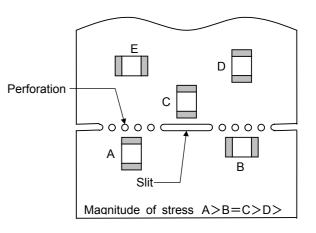
	Prohibited layout	Recommended layout
Warp of Circuit board		Layout the Varistor sideways against the stressing direction

- (2) The following layout is for your reference since mechanical stress near the dividing/breaking position of a PC board varies depending on the mounting position of the Varistors.
- (3) The magnitude of mechanical stress applied to the Varistors when the circuit board is divided is in the order of push back < slit < V-groove < perforation.

Also take into account the layout of the Varistors and the dividing/breaking method.

2-2-5. Mounting Density and Spaces

If components are arranged in too narrow a space, the components can be affected by solder bridges and solder balls. The space between components should be carefully determined.



CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SCS004E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 4 of 8
	Common Specification (Precautions for Use)	DATE 1 Apr, 2008

Precautions for Assembly

3-1.Storage

- (1) The Varistors before mounting on PCB shall be stored between 5 40°C and 20 70% RH, not under severe conditions of high temperature and humidity.
- (2) If stored in a place that is humid, dusty, or contains corrosive gasses (hydrogen sulfide, sulfurous acid, hydrogen chloride and ammonia, etc.), the solderability of terminal electrodes may deteriorate. In addition, storage in a place subjected to heating and/or exposure to direct sunlight will cause deformed tapes and reels, and components sticking to tapes, both of which can result in mounting problems.
- (3) Do not store components longer than 6 months. Check the solderability of products that have been stored for more than 6 months before use.

3-2.Adhesives for Mounting

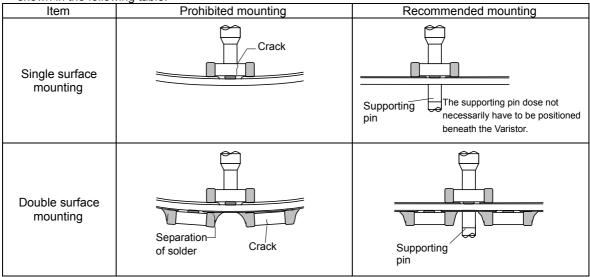
- (1) The amount and viscosity of an adhesive for mounting shall be such that the adhesive shall not flow off on the land during it's curing.
- (2) If the amount of adhesive is insufficient for mounting, the Varistor may fall off after or during soldering.
- (3) If the adhesive is too low in its viscosity, the Varistors may be out of alignment after or during soldering.
- (4) Adhesives for mounting can be cured by ultraviolet or infrared radiation. In order to prevent the terminal electrodes of the Varistors from oxidizing, the curing shall be under the following conditions: 160°C max., for 2 minutes max.
- (5) Insufficient curing may cause the Varistors to fall off after or during soldering. In addition insulation resistance between terminal electrodes may deteriorate due to moisture absorption. In order to prevent these problems, please observe proper curing conditions.

3-3. Chip Mounting Consideration

- (1) When mounting the Varistors/components on a PC board, the Varistor bodies shall be free from excessive impact loads such as mechanical impact or stress due to the positioning, pushing force and displacement of vacuum nozzles during mounting.
- (2) Maintenance and inspection of the Chip Mounter must be performed regularly.
- (3) If the bottom dead center of the vacuum nozzle is too low, the Varistor will crack from excessive force during mounting.

The following precautions and recommendations are for your reference in use.

- (a) Set and adjust the bottom dead center of the vacuum nozzles to the upper surface of the PC board after correcting the warp of the PC board.
- (b) Set the pushing force of the vacuum nozzle during mounting to 1 to 3 N in static load.
- (c) For double surface mounting, apply a supporting pin on the rear surface of the PC board to suppress the bending of the PC board in order to minimize the impact of the vacuum nozzles. Typical examples are shown in the following table.



(d) Adjust the vacuum nozzles so that their bottom dead center during mounting is not too low.

CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SCS004E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 5 of 8
	Common Specification (Precautions for Use)	DATE 1 Apr, 2008

- (4) The closing dimensions of the positioning chucks shall be controlled. Maintenance and replacement of positioning chucks shall be performed regularly to prevent chipping or cracking of the Varistors caused by mechanical impact during positioning due to worn positioning chucks.
- (5) Maximum stroke of the nozzle shall be adjusted so that the maximum bending of PC board does not exceed 0.5mm at 90mm span. The PC board shall be supported by an adequate number of supporting pins.

3-4. Selection of Soldering Flux

Soldering flux may seriously affect the performance of the Varistors. The following shall be confirmed before use.

- (1) The soldering flux should have a halogen based content of 0.1 wt. % (converted to chlorine) or below. Do not use soldering flux with strong acid.
- (2) When applying water-soluble soldering flux, wash the Varistors sufficiently because the soldering flux residue on the surface of PC boards may deteriorate the insulation resistance on the Varistors' surface.

3-5.Soldering

3-5-1. Flow soldering

For flow soldering, abnormal and large thermal and mechanical stress, caused by the "Temperature Gradient" between the mounted Varistors and melted solder in a soldering bath may be applied directly to the Varistors, resulting in failure and damage of the Varistors,

Therefore It is essential that soldering process follow these recommended conditions.

(1) Application of Soldering flux:

The soldering flux shall be applied to the mounted Varistors thinly and uniformly by foaming method.

(2) Preheating:

The mounted Varistors/Components shall be preheated sufficiently so that the "Temperature Gradient" between the Varistors/Components and the melted solder shall be 150 °C max.

(3) Immersion into Soldering bath:

The Varistors shall be immersed into a soldering bath of 240 to 260 °C for 3 to 5 seconds.

(4) Gradual Cooling:

The Varistors shall be cooled gradually to room ambient temperature with the cooling temperature rates of 8 °C/s max. from 250°C to 170°C and 4 °C/s max. from 170°C to 130°C.

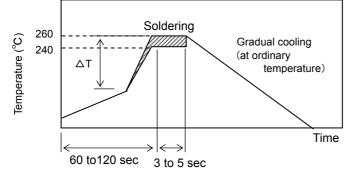
(5) Flux Cleaning:

When the Varistors are immersed into a cleaning solvent, be sure that the surface temperature of devices do not exceed 100 °C.

(6) Performing flow soldering once under the conditions shown in the figure below [Recommended profile of Flow soldering (Ex)] will not cause any problems.

However, pay attention to the possible warp and bending of the PC board.

Recommended profile for Flow Soldering [Ex.]



(Allowable temperature difference)		
Size	Temp. Tol.	
0603	ΔT ≦ 150 °C	

For products specified in individual specifications, avoid flow soldering

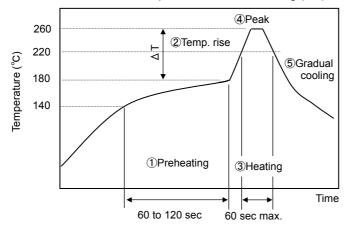
3-5-2. Reflow soldering

The reflow soldering temperature conditions are each temperature curves of Preheating, Temp. rise, Heating, Peak and Gradual cooling. Large temperature difference caused by rapid heat application to the Varistors may lead to excessive thermal stresses, contributing to the thermal cracks. The Preheating temperature requires controlling with great care so that tombstone phenomenon may be prevented.

CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SCS004E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 6 of 8
	Common Specification (Precautions for Use)	DATE 1 Apr, 2008

Item	Temperature	Period or Speed
①Preheating	140 to 180 ℃	60 to 120 sec
②Temp. rise	Preheating temp. to Peak temp.	2 to 5 °C/sec
③Heating	220 ℃ min.	60 sec max.
<pre>④Peak</pre>	260 °C max.	10 sec max.
⑤Gradual cooling	Peak temp. to 140 $^{\circ}\!\mathrm{C}$	1 to 4 ℃/sec

Recommended profile of Reflow soldering (Ex.)



⟨ Allowable temperature difference ∆T⟩		
Size Temp. Tol.		
0402 to 0805 0504	ΔT≦ 150 °C	

The rapid cooling (forced cooling) during Gradual cooling part should be avoided, because this may cause defects such as the thermal cracks, etc.When the Varistors are immersed into a cleaning solvent, make sure that the surface temperatures of the devices do not exceed 100°C.

Performing reflow soldering twice under the conditions shown in the figure above [Recommended profile of Reflow soldering (EX)] will not cause any problems.

However, pay attention to the possible warp and bending of the PC board.

3-5-3. Hand soldering

Hand soldering typically causes significant temperature change, which may induce excessive thermal stresses inside the Varistors, resulting in the thermal crack, etc.

In order to prevent any defects, the following should be observed.

- The temperature of the soldering tips should be controlled with special care.
- · The direct contact of soldering tips with the Varistor and/or terminal electrodes should be avoided.
- · Dismounted Varistors shall not be reused.

(1) Condition 1 (with preheating)

- (a) Soldering:
 - ϕ 1.0mm or below Thread eutectic solder with soldering flux* in the core.
 - *Rosin-based and non-activated flux is recommended.
- (b) Preheating:

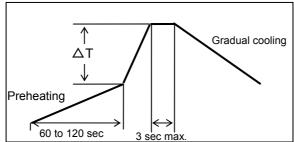
The Varistors shall be preheated so that the "Temperature Gradient" between the devices and the tip of soldering iron is 150°C or below.

- (c) Temperature of Iron tip: 300°C max.
 - (The required amount of solder shall be melted in advance on the soldering tip.)
- (d) Gradual Cooling :

After soldering, the Varistors shall be cooled gradually at room temperature.

CLASSIFICATION SPECIFICATIONS SUBJECT Multilayer Varistor , Chip Type Common Specification (Precautions for Use) No. 151S-EZJ-SCS004E 7 of 8 DATE 1 Apr, 2008

Recommended profile of Hand Soldering [Ex.]



⟨Allowable temperature difference △T⟩		
Size Temp. Tol.		
0402 to 0805	ΔΤ≦ 150 °C	

(2) Condition 2 (without preheating)

Hand soldering can be performed without preheating, by following the conditions below :

- (a) Soldering iron tip shall never directly touch the ceramic and terminal electrodes of the Varistors.
- (b) The lands are sufficiently preheated with a soldering iron tip before sliding the soldering iron tip to the terminal electrodes of the Varistors for soldering.

Conditions of Hand soldering without preheating

Conditions of Fland Soldering Without profiteding		
	Condition	
Chip size	0402 to 0805	
Temperature of iron tip	270 °C max.	
Wattage	20 W max.	
Shape of Iron tip	ϕ 3 mm max.	
Soldering time with a soldering iron	3 sec max.	

3- 6.Post Soldering Cleaning

3-6-1. Cleaning solvent

Soldering flux residue may remain on the PC board if cleaned with an inappropriate solvent. This may deteriorate the electrical characteristics and reliability of the Varistors.

3-6-2. Cleaning conditions

Inappropriate cleaning conditions such as insufficient cleaning or excessive cleaning may impair the electrical characteristics and reliability of the Varistors.

- (1) Insufficient cleaning can lead to:
 - (a) The halogen substance found in the residue of the soldering flux may cause the metal of terminal electrodes to corrode.
 - (b) The halogen substance found in the residue of the soldering flux on the surface of the Varistors may change resistance values.
 - (c) Water-soluble soldering flux may have more remarkable tendencies of (a) and (b) above compared to those of rosin soldering flux.
- (2) Excessive cleaning can lead to:
 - (a) Overuse of ultrasonic cleaning may deteriorate the strength of the terminal electrodes or cause cracking in the solder and/or ceramic bodies of the Varistors due to vibration of the PC boards.

Please follow these conditions for Ultrasonic cleaning:

Ultrasonic wave output : 20 W/L max.
Ultrasonic wave frequency : 40 kHz max.
Ultrasonic wave cleaning time : 5 min. max.

3-6-3. Contamination of Cleaning solvent

Cleaning with contaminated cleaning solvent may cause the same results as insufficient cleaning due to the high density of liberated halogen.

3-7.Inspection Process

When mounted PC boards are inspected with measuring terminal pins, abnormal and excess mechanical stress shall not be applied to the PC board or mounted components, to prevent failure or damage to the devices.

- (1) Mounted PC boards shall be supported by an adequate number of supporting pins with bend settings of 90 mm span 0.5mm max.
- (2) Confirm that the measuring pins have the right tip shape, are equal in height and are set in the correct positions. The following figures are for your reference to avoid bending the PC board.

	Prohibited setting	Recommended setting
Bending of PC board	Check pin Separated, Crack	Check pin Supporting pin

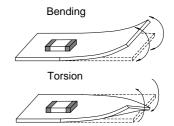
CLASSIFICATION	SPECIFICATIONS	No. 151S-EZJ-SCS004E
SUBJECT	Multilayer Varistor , Chip Type	PAGE 8 of 8
	Common Specification (Precautions for Use)	DATE 1 Apr, 2008

3-8.Protective Coating

When the surface of a PC board on which the Thermistors have been mounted is coated with resin to protect against moisture and dust, it shall be confirmed that the protective coating which is corrosive or chemically active is not used, in order that the reliability of the Thermistors in the actual equipment may not be influenced. Coating materials that expand or shrink also may lead to damage to the Thermistor during the curing process.

3- 9. Dividing/Breaking of PC Boards

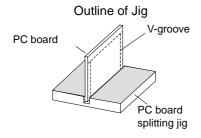
- (1) Abnormal and excessive mechanical stress such as bending or torsion shown below can cause cracking in the Varistors.
- (2) Dividing/Breaking of the PC boards shall be done carefully at moderate speed by using a jig or apparatus to prevent the Varistors on the boards from mechanical damage.

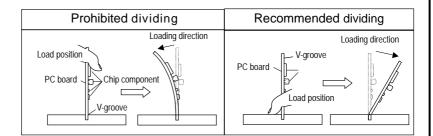


(3) Examples of PCB dividing/breaking jig:

The outline of PC board breaking jig is shown below.

When PC board are broken or divided, loading points should be close to the jig to minimize the extent of the bending. Also, planes with no parts mounted on should be used as plane of loading, which generates a compressive stress on the mounted plane, in order to prevent tensile stress induced by the bending, which may cause crack of the Varistors or other parts mounted on the PC boards.





3- 10.Mechanical Impact

(1) The Varistors shall be free from any excessive mechanical impact.

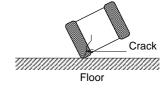
The Varistor body is made of ceramics and may be damaged or cracked if dropped.

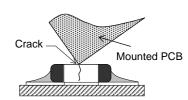
Never use a Varistor which has been dropped; their quality may be impaired and failure rate increased.

(2) When handling PC boards with Varistors mounted on them, do not allow the Varistors to collide with another PC board.

When mounted PC boards are handled or stored in a stacked state, impact

between the corner of a PC board and the Varistor may cause damage or cracking and can deteriorate the withstand voltage and insulation resistance of the Varistor.





4. Other

The various precautions described above are typical. For special mounting conditions, please contact us.

Note	
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CLASSFICATION	SPECIFICATIONS	No. 151S-EZJ-SCV002E	
SUBJECT	Multilayer Varistor, Chip Type	PAGE 1 of 5	
	Taped and Reeled Packaging Specifications	DATE 5 June, 2006	

This specification applies to taped and reeled packing for Multilayer varistors, chip type.

2. Applicable Standards

EIAJ (Electric Industries Association of Japan) Standard EIAJ RC-1009B

JIS (Japanese Industrial Standard) Standard JIS C 0806

3. Packing Specification

3- 1.Structure and Dimensions

Paper taping packaging is carried out according the following diagram

1) Carrier tape : Shown in Fig. 5. 2) Reel : Shown in Fig. 6.

3) Packaging : We shall pack suitably in order prevent damage during transportation or storage.

3- 2. Packing Quantity

		Carrier-Tape		Quantity (pcs./reel)	
Size Thickness			Taping	<i>∮</i> 180mm Reel	
(EIA)	Capacitor(mm)	Material	Pitch	Packaging Code	Quantity
0402	0.50 +/- 0.05	Paper Taping	2 mm	V	10,000
0603	0.8 +/- 0.1	Paper Taping	4 mm	V	4,000
	0.8 +/- 0.2	Paper Taping	4 mm	V	5,000
0805	1.25 +/- 0.20 Embossed Tap.	4 mm	Y	2,000	
			F	3,000	

Explanation of Part Numbers (Example)

EZJZ 1 <u>V</u> 270 G A Packaging Code

3- 3. Marking on the Reel

The following items are described in the side of a reel in English at least.

- 1) Part Number
- 2) Quantity
- 3) Lot Number
- 4) Place of origin

Note ;				
		APPROVAL	CHECK	DESIGN
	Panasonic Electronic Devices Co., Ltd.	Y.Sakaguti	T.Kawamura	Y.Sasaki

CLASSFICATION	SPECIFICATIONS	No. 151S-EZJ-SCV002E
SUBJECT	Multilayer Varistor, Chip Type	PAGE 2 of 5
	Taped and Reeled Packaging Specifications	DATE 5 June, 2006

3- 4. Structure of Taping

1) The direction of winding of taping on the reel shall be in accordance with the following diagram.

Fig. 1 Paper Taping

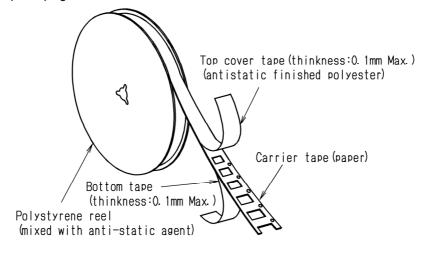
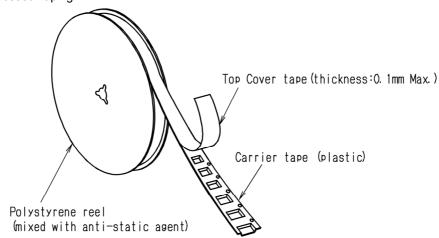
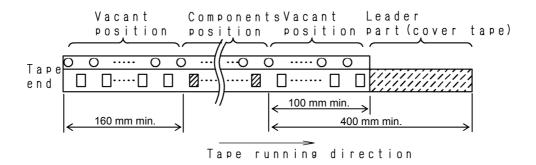


Fig. 2 Embossed Taping



2) The specification of the leader and empty portion shall be in accordance with the following diagram.

Fig. 3 Leader Part and Taped End



CLASSFICATION	SPECIFICATIONS	No. 151S-EZJ-SCV002E
SUBJECT	Multilayer Varistor, Chip Type	PAGE 3 of 5
	Taped and Reeled Packaging Specifications	DATE 5 June, 2006

4. Efficiency

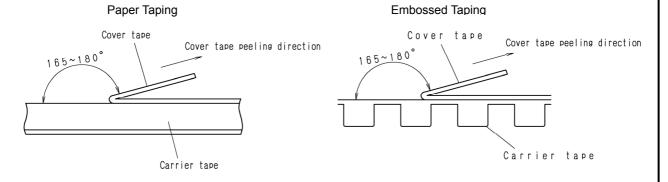
4- 1.Breakage strength of the tape: 10N or more.

4- 2.Peel strength of the cover tape (refer to the Fig. 4).1) Peel angle: 165 to 180 degree from the tape adhesive face.

2) Peel velocity: 300 mm per min.

3) Peel strength: 0.1 to 0.7 N

Fig. 4 Peel strength of the cover tape



4-3.Barrs on tape

There shall be no barrs preventing suction when products are taken out.

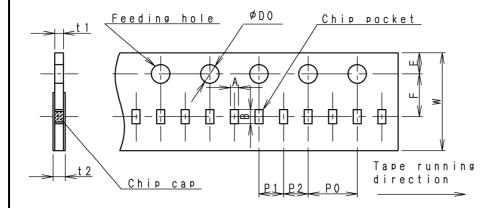
4- 4. Missing of products

The missing of products shall be 0.1 % or less per reel and there shall be no continuous missing of products.

4- 5.Adherence to the tape

Products shall not be stuck to the cover tape or bottom tape.

Fig. 5 Carrier Tape Dimension



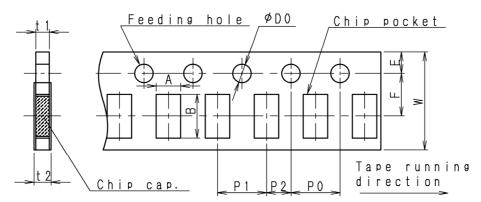
Code	Dimension	
W	8.0 +/- 0.2	
F	3.50 +/- 0.05	
Ш	1.75 +/- 0.10	
P_1	2.00 +/- 0.05	
P_2	2.00 +/- 0.05	
P_0	4.00 +/- 0.05	
D_0	φ 1.5 +0.1/-0	
t_1	0.7 max.	
t ₂	1.0 max.	

Unit: mm

Size Code	0402	
Α	0.62 +/- 0.05	
В	1.12 +/- 0.05	
	Unit : mm	

CLASSFICATION SPECIFICATIONS SUBJECT Multilayer Varistor, Chip Type Taped and Reeled Packaging Specifications No. 151S-EZJ-SCV002E PAGE 4 of 5 DATE 5 June, 2006

(b) 0603,0805 size: 4mm taping pitch for Paper taping.



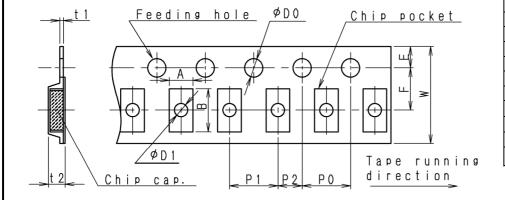
Code	Dimension	
W	8.0 +/- 0.2	
F	3.50 +/- 0.05	
Е	1.75 +/- 0.10	
P ₁	4.0 +/- 0.1	
P ₂	2.00 +/- 0.05	
P ₀	4.0 +/- 0.1	
D_0	φ 1.5 +0.1/-0	
t ₁	1.1 max.	
t ₂ 1.4 max.		

Unit : mm

Size Code	0603	0805
Α	1.0 +/- 0.1	1.65 +/- 0.20
В	1.8 +/- 0.1	2.4 +/- 0.2

Unit: mm

(c) 0805 size: 4mm taping pitch for Embossed taping.



Code	Dimension	
W	8.0 +/- 0.2	
F	3.50 +/- 0.05	
Ш	1.75 +/- 0.10	
P ₁	4.0 +/- 0.1	
P_2	2.00 +/- 0.05	
P ₀	4.0 +/- 0.1	
D_0	φ 1.5 +0.1/-0	
D_1	φ 1.1+/- 0.1	
t_1	0.6 max.	
t ₂	2.5 max.	

Unit : mm

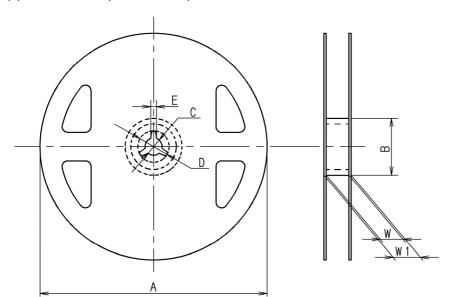
Size Code	0805
Α	1.55 +/- 0.20
В	2.35 +/- 0.20
-	L lucit c mana

Unit: mm

CLASSFICATION	SPECIFICATIONS	No. 151S-EZJ-SCV002E
SUBJECT	Multilayer Varistor, Chip Type	PAGE 5 of 5
	Taped and Reeled Packaging Specifications	DATE 5 June, 2006

Fig. 6 Reel Dimension

(a) Φ180mm Reel (Standard Reel)



Code	Dimension
Α	φ 180 +0/-3.0
В	φ 60.0 +/- 0.5
С	13.0 +/- 0.5
D	21.0 +/- 0.8
Ш	2.0 +/- 0.5
W	9.0 +/- 0.3
W_1	11.4 +/- 0.1

Unit : mm

Note;		