

# DATA SHEET

## **CBT3244**

Octal bus switch with quad output enables

Product data  
Supersedes data of 2001 May 15

2002 May 28

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## CBT3244

## FEATURES

- Standard '244-type pinout
- 5  $\Omega$  switch connection between two ports
- TTL compatible control input levels
- Package options include plastic small outline (D), shrink small outline (DB), QSOP (DS), thin shrink small outline (TSSOP)
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

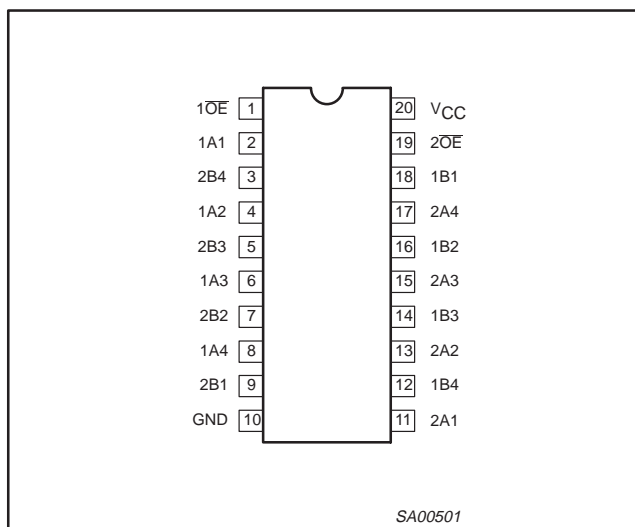
## DESCRIPTION

The CBT3244 provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3244 device is organized as two 4-bit low-impedance switches with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the switch is on and data can flow from port A to port B, or vice versa. When  $\overline{OE}$  is high, the switch is open and high-impedance state exists between the two ports.

The CBT3244 is characterized for operation from  $-40$  to  $85$   $^{\circ}\text{C}$ .

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 19	$1\overline{OE}$ , $2\overline{OE}$	Output enable
2, 4, 6, 8	1A1–1A4	Inputs
11, 13, 15, 17	2A1–2A4	Inputs
18, 16, 14, 12	1B1–1B4	Outputs
9, 7, 5, 3	2B1–2B4	Outputs
10	GND	Ground (0V)
20	$V_{CC}$	Positive supply voltage

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25$ $^{\circ}\text{C}$ ; GND = 0 V	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Yn	$C_L = 50$ pF; $V_{CC} = 5$ V	250	ps
$C_{IO(OFF)}$	Pin capacitance (OFF state)	$V_O = 3$ V or 0V	6	pF
$I_{CC}$	Quiescent supply current	$V_{CC} = 5.5$ V; $I_O = 0$ ; $V_I = V_{CC}$ or GND	1	$\mu\text{A}$

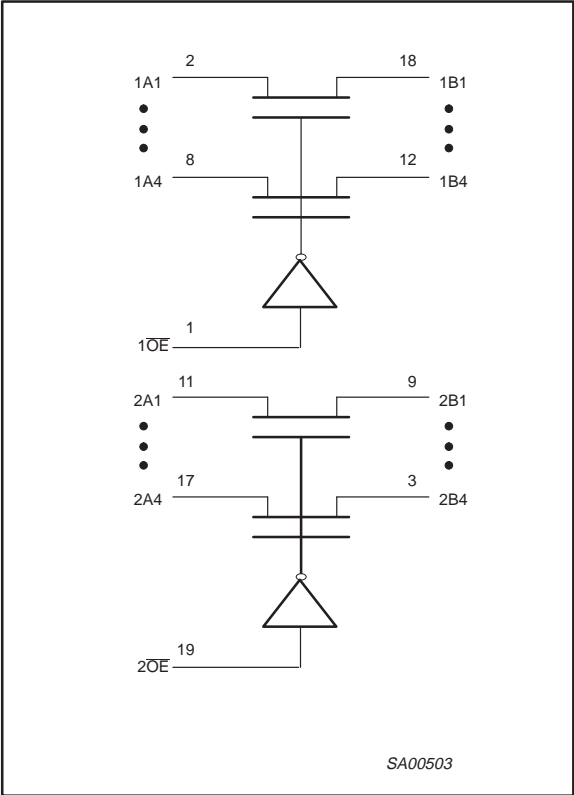
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
20-Pin Plastic TSSOP	$-40$ to $85$ $^{\circ}\text{C}$	CBT3244PW	SOT360-1
20-Pin Plastic SSOP (QSOP)	$-40$ to $85$ $^{\circ}\text{C}$	CBT3244DS	SOT566-1
20-Pin Plastic SSOP	$-40$ to $85$ $^{\circ}\text{C}$	CBT3244DB	SOT339-1
20-Pin Plastic SO	$-40$ to $85$ $^{\circ}\text{C}$	CBT3244D	SOT163-1

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LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
1OE	2OE	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

H = High voltage level  
L = Low voltage level  
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		−0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	−18	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		−1.2 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	−50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	output in Off or High state	−0.5 to +7	V
I <sub>OUT</sub>	DC output current	output in Low state	128	mA
T <sub>stg</sub>	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2.0	—	V
$V_{IL}$	Low-level Input voltage	—	0.8	V
$T_{amb}$	Operating free-air temperature range	−40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T <sub>amb</sub> = −40 to +85 °C			
			Min	Typ <sup>1</sup>	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5 V; I <sub>I</sub> = −18 mA	—	—	−1.2	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	—	—	±5	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5 V; I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	—	1	3	μA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5 V, one input at 3.4 V, other inputs at V <sub>CC</sub> or GND	—	—	3.5	mA
C <sub>I</sub>	Control pins	V <sub>I</sub> = 3 V or 0, $\overline{OE}$ = V <sub>CC</sub>	—	3	—	pF
C <sub>IO(OFF)</sub>	Power-off leakage current	V <sub>O</sub> = 3 V or 0	—	6	—	pF
r <sub>on</sub> <sup>3</sup>	On-resistance	V <sub>CC</sub> = 4.5 V; V <sub>1</sub> = 0 V; I <sub>I</sub> = 64 mA	—	5	7	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>1</sub> = 0 V; I <sub>I</sub> = 30 mA	—	5	7	
		V <sub>CC</sub> = 4.5 V; V <sub>1</sub> = 0 V; I <sub>I</sub> = 15 mA	—	10	15	

## NOTES:

1. All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_{amb} = 25 \text{ }^{\circ}\text{C}$
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.  
On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

## AC CHARACTERISTICS

GND = 0 V;  $t_R$ ;  $C_L = 50 \text{ pF}$ 

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	74CBT3244		UNIT
				T <sub>amb</sub> = −40 to +85 °C V <sub>CC</sub> = +5.0 V ±0.5 V		
				Min	Max	
t <sub>pd</sub>	Propagation delay <sup>1</sup>	A or B	B or A	—	.25	ns
t <sub>en</sub>	Output enable time to High and Low level	OE	A or B	1.0	6.3	ns
t <sub>dis</sub>	Output disable time from High and Low level	OE	A or B	1.0	6.0	ns

## NOTE:

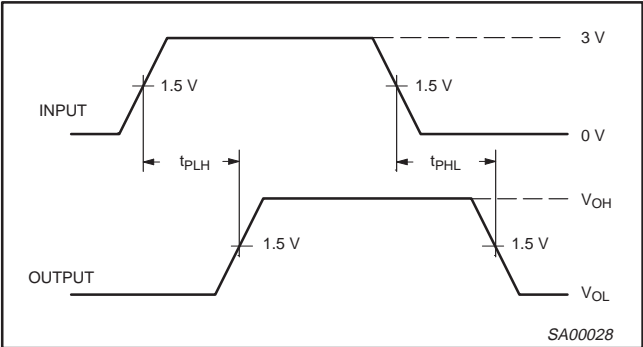
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

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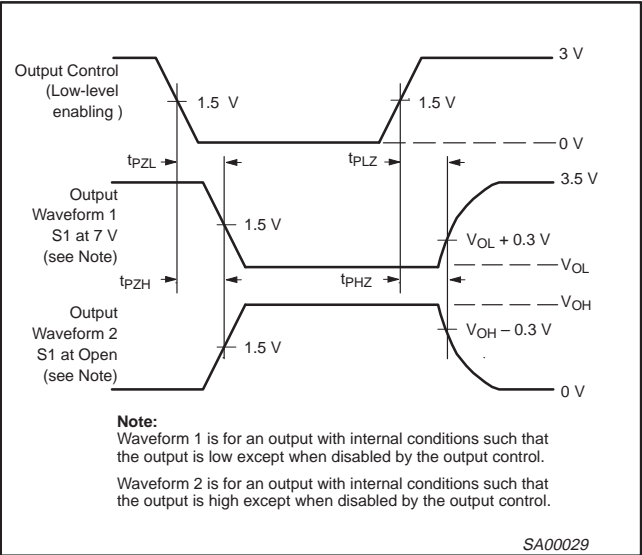
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AC WAVEFORMS

$V_M = 1.5\text{ V}$ ,  $V_{IN} = \text{GND to } 3.0\text{ V}$



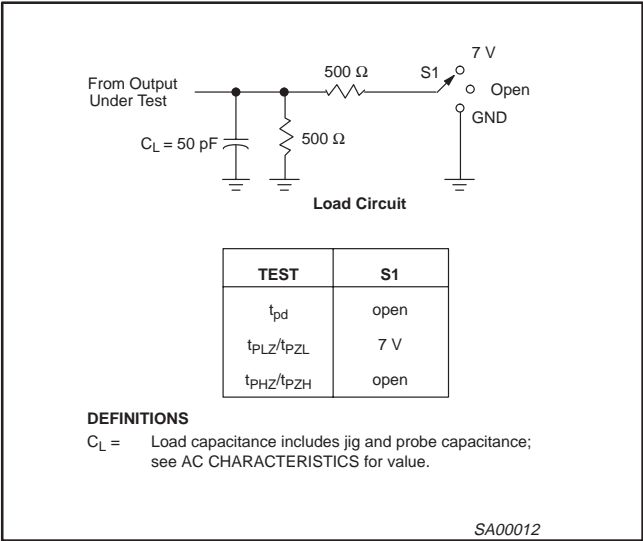
Waveform 1. Input to Output Propagation Delays



**Note:**  
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



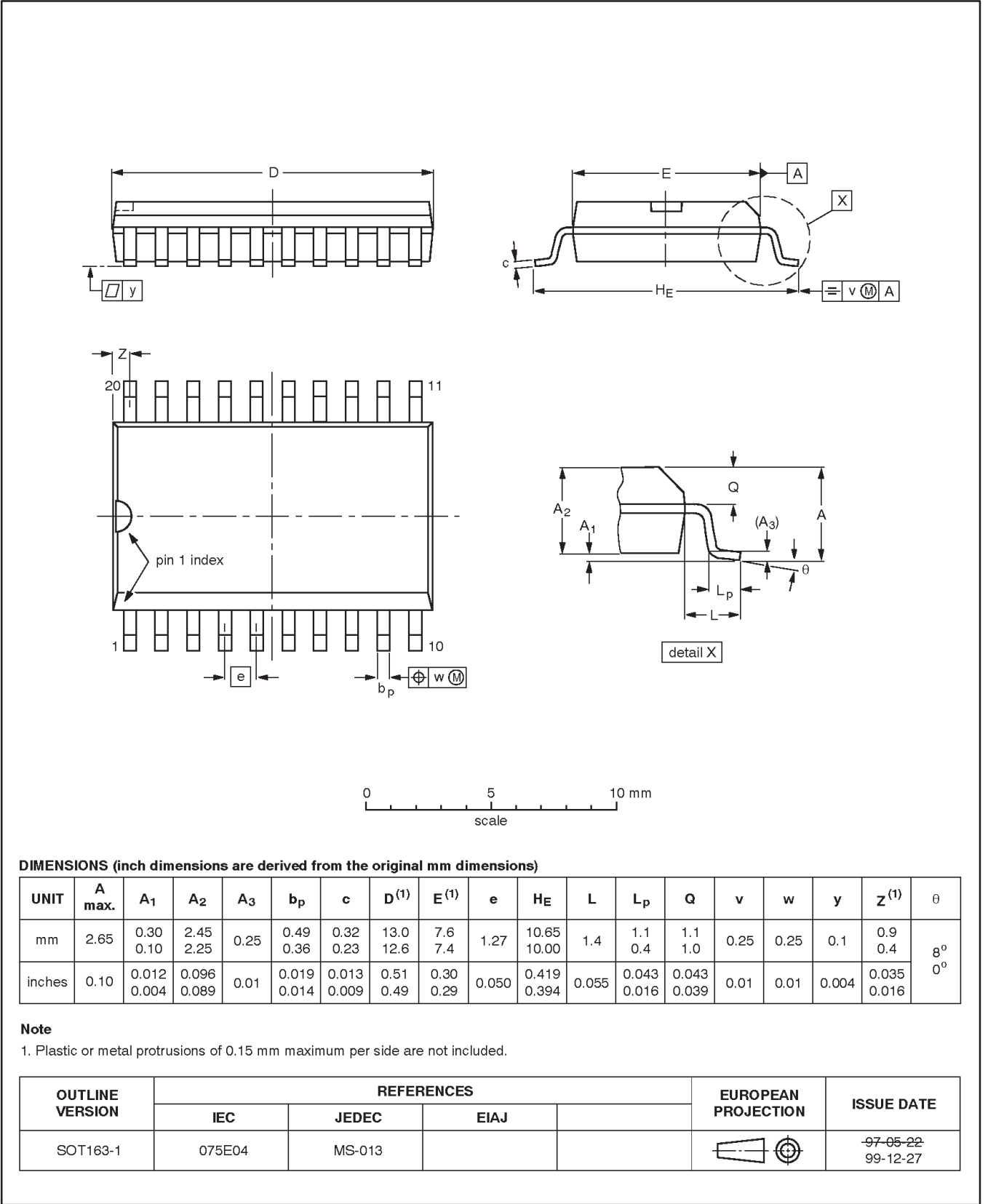
- NOTES:**
1. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  2. The outputs are measured one at a time with one transition per measurement.

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

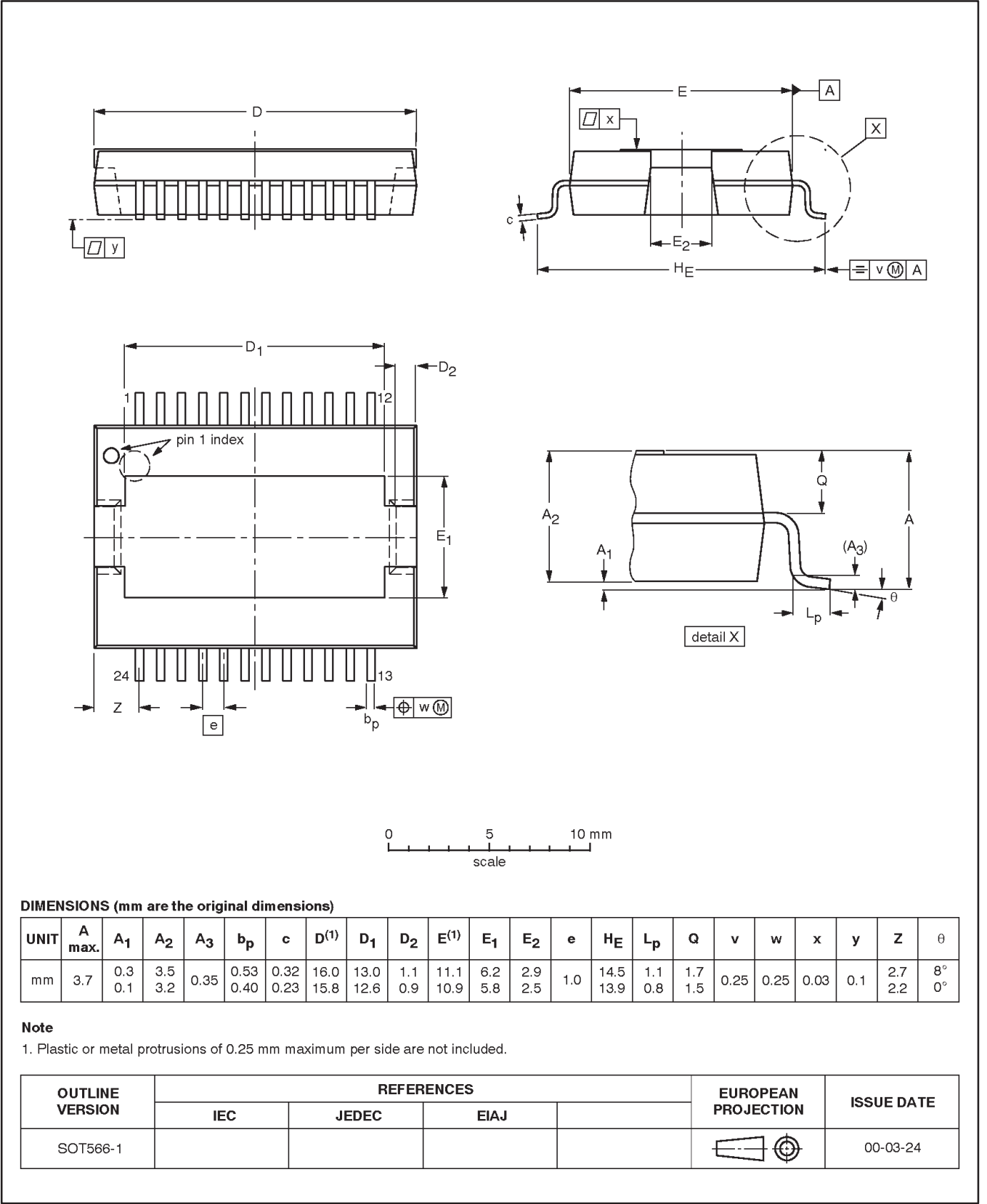


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HSOP24: plastic, heatsink small outline package; 24 leads

SOT566-1

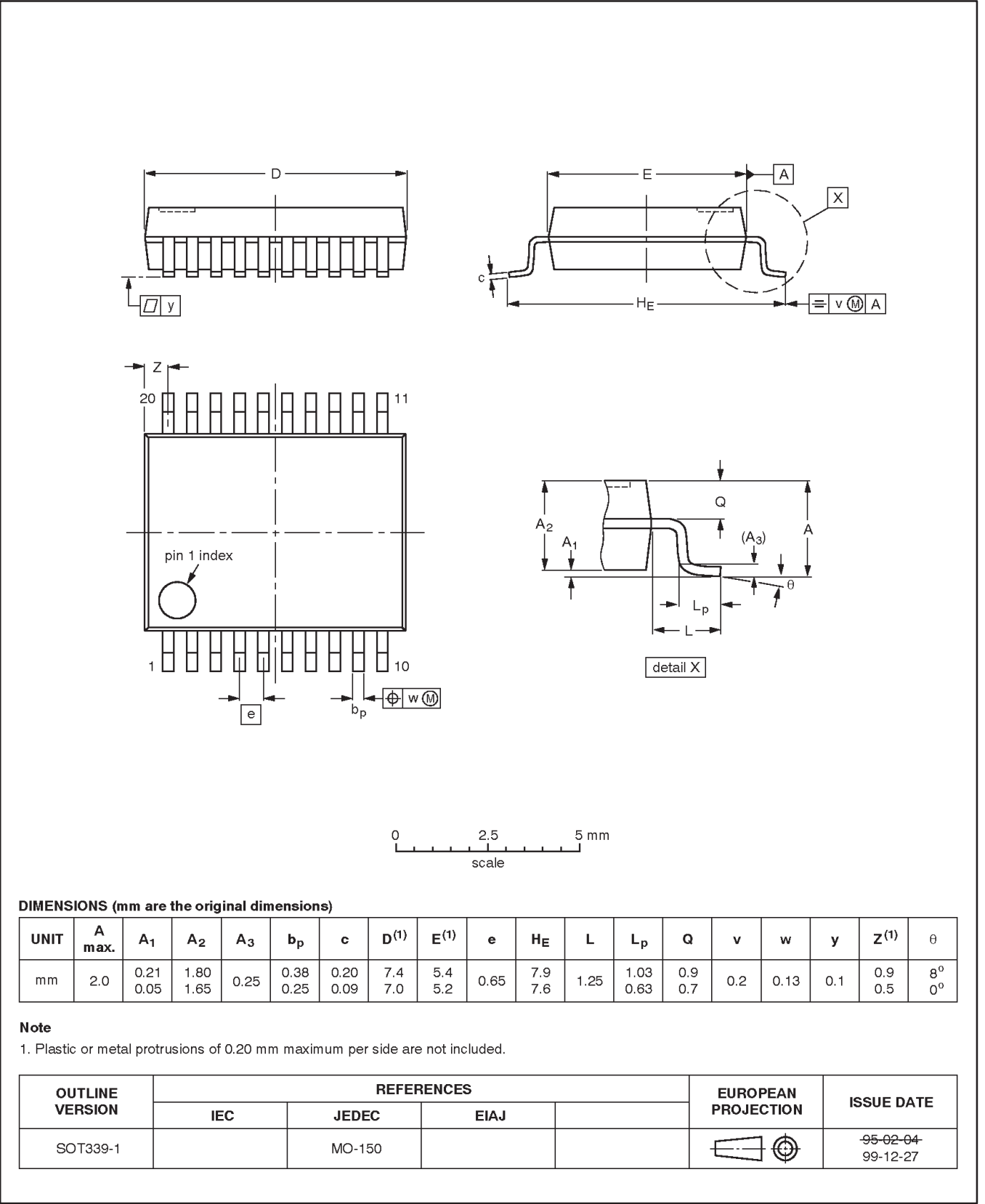


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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



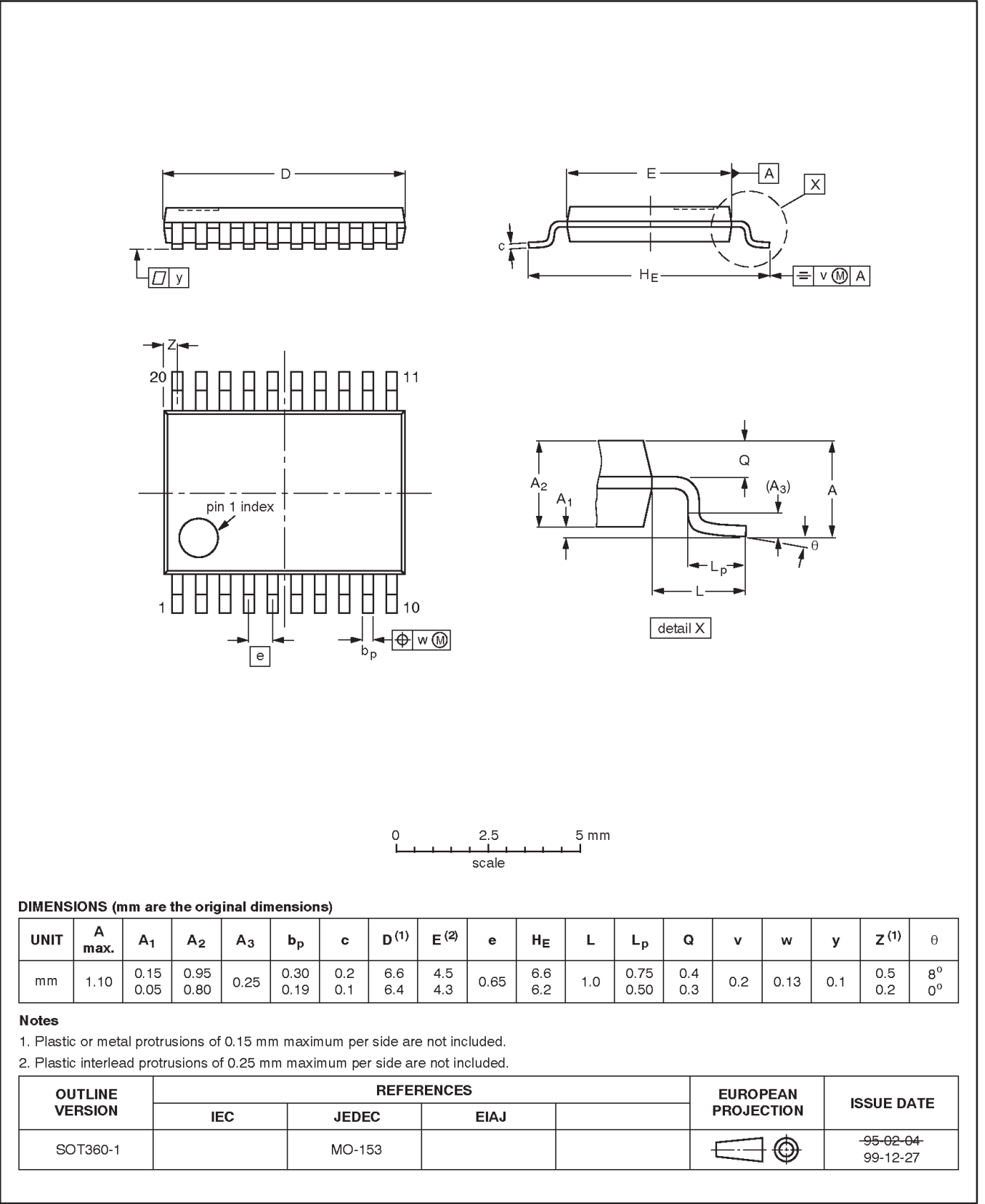


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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



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## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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