



Features

- Lead free device (RoHS compliant*)
- 100 A (2/10 μ s) per Bellcore GR1089 (Intra-Building)
- Protects 2 lines
- ESD protection
- Low capacitance 8 pF

Applications

- T1/E1 line cards
- ISDN U-Interface and S/T Interface
- xDSL
- Ethernet – 10/100 Base T

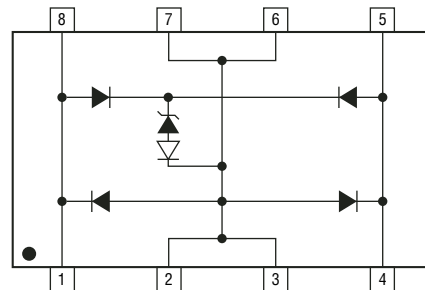
CDNBS08-PLC03-3.3 Steering Diode/TVS Array Combo

General Information

The markets of portable communications, computing and video equipment are challenging the semiconductor industry to develop increasingly smaller electronic components.

Bourns offers Steering Diode/Transient Voltage Suppressor Array combination diodes for surge and ESD protection applications in an 8 Lead Narrow Body SOIC package size format. Bourns Chip Diodes conform to JEDEC standards, are easy to handle on standard pick and place equipment and their flat configuration minimizes roll away.

The Bourns® device will meet IEC 61000-4-2 (ESD), IEC 61000-4-4 (EFT) and IEC 61000-4-5 (Surge) requirements.



Electrical Characteristics (@ $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Min.	Nom.	Max.	Unit
Capacitance @ 0 V 1 MHz ¹	$C_{j(\text{SD})}$		20	25	pF
Capacitance @ 0 V 1 MHz ²	$C_{j(\text{SD})}$		8	12	pF
Working Peak Voltage	V_{WM}			3.0	V
Min Breakdown Voltage @ 1 mA	V_{BR}	3.3			V
Clamping Voltage @ 8/20 μ s @ IPP = 100 A ^{3, 4}	V_F			18	V
Clamping Voltage @ 8/20 μ s @ IP = 50 A, Line - Ground	V_F			11	
Max Leakage Current @ V_{WM}	I_D			2	μ A
ESD Protection: IEC 61000-4-2 Contact Discharge Air Discharge		± 8 ± 15			kV kV
Peak Pulse Power ($t_p = 8/20 \mu\text{s}$) ⁵	P_{PP}			1800	W

Notes:

1. Measured between I/O pins and ground (pin 1 or 2).
2. Measured between I/O pins (pins 1 to 4).
3. See Pulse Wave Form. For an 8/20 μ s waveform, apply positive pulse to pin 1 to 8 to pin 2 or 3 (ground).
4. Measured between pin 1 or 8 to pin 2 or 3; pin 1 or 8 to pin 4 or 5.
5. See Peak Pulse Power vs. Pulse Time.

Thermal Characteristics (@ $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Min.	Nom.	Max.	Unit
Junction Temperature Range	T_J	-55	+25	+150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55	+25	+150	$^\circ\text{C}$

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex.

Specifications are subject to change without notice.

Customers should verify actual device performance in their specific applications.

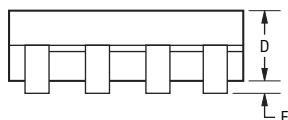
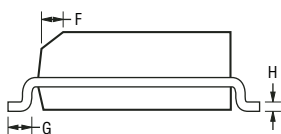
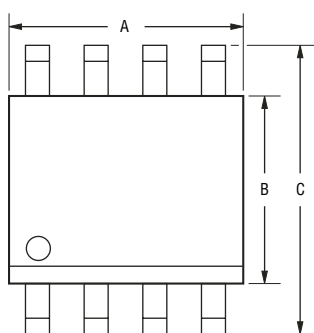
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Mechanical Characteristics

This is a molded JEDEC Narrow Body SO-8 package with lead free 100 % Sn plating on the lead frame. It weighs approximately 15 mg and has a flammability rating of UL 94V-0.

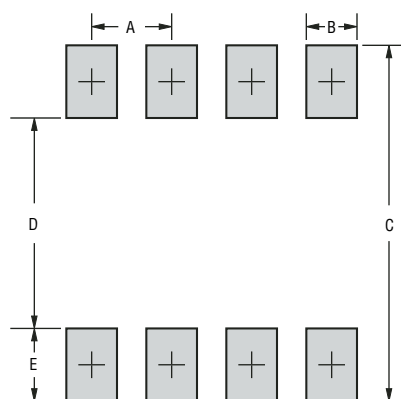
Product Dimensions



DIMENSIONS = $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$

Dimensions	
A	$\frac{4.80 - 5.00}{(0.189 - 0.196)}$
B	$\frac{3.80 - 4.00}{(0.150 - 0.157)}$
C	$\frac{5.80 - 6.20}{(0.229 - 0.244)}$
D	$\frac{1.35 - 1.75}{(0.054 - 0.068)}$
E	$\frac{0.10 - 0.25}{(0.004 - 0.008)}$
F	$\frac{0.25 - 0.50}{(0.010 - 0.019)}$
G	$\frac{0.40 - 1.250}{(0.016 - 0.049)}$
H	$\frac{0.18 - 0.25}{(0.007 - 0.009)}$

Recommended Footprint



Dimensions	
A	$\frac{1.143 - 1.397}{(0.045 - 0.055)}$
B	$\frac{0.635 - 0.889}{(0.025 - 0.035)}$
C	$\frac{6.223}{(0.245)} \text{ Min.}$
D	$\frac{3.937 - 4.191}{(0.155 - 0.165)}$
E	$\frac{1.016 - 1.27}{(0.040 - 0.050)}$

How To Order

CD NBS08 - PLC03 - 3.3

Common Code _____
 CD = Chip Diode
 Package _____
 NBS08 = Narrow Body SOIC8 Package
 Model _____
 PLC03 = Model Number
 Minimum Breakdown Voltage _____
 3.3 = 3.3 V_{BR} (Volts)

Typical Part Marking

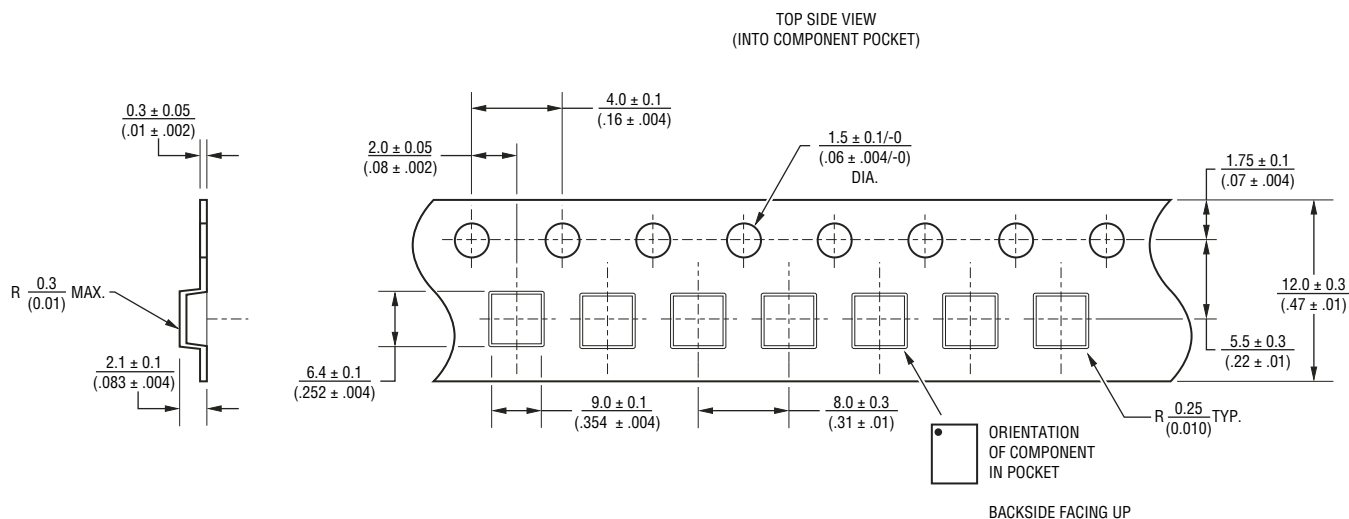
CDNBS08-PLC03-3.3 **PBC**

CDNBS08-PLC03-3.3 Steering Diode/TVS Array Combo

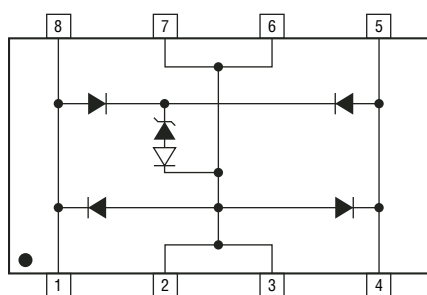
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Packaging

The surface mount product is packaged in a 12 mm x 8 mm Tape and Reel format per EIA-481 standard.



Block Diagram



Device Pinout

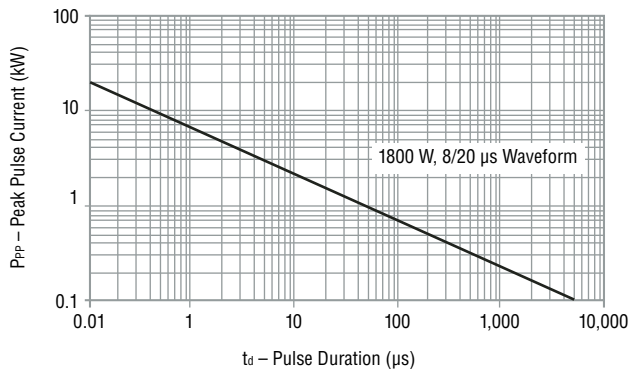
Pin	Function
1	I/O 1
2	GND
3	GND
4	I/O 2
5	I/O 2
6	GND
7	GND
8	I/O 1

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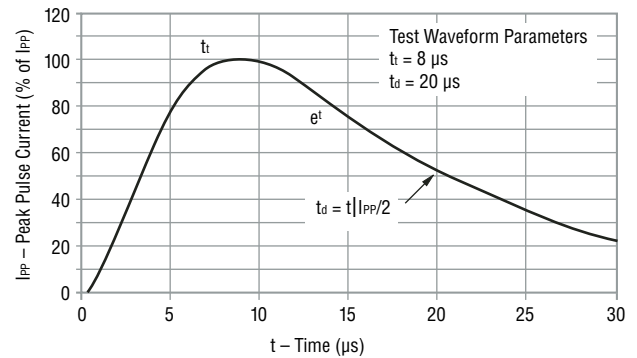
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Performance Graphs

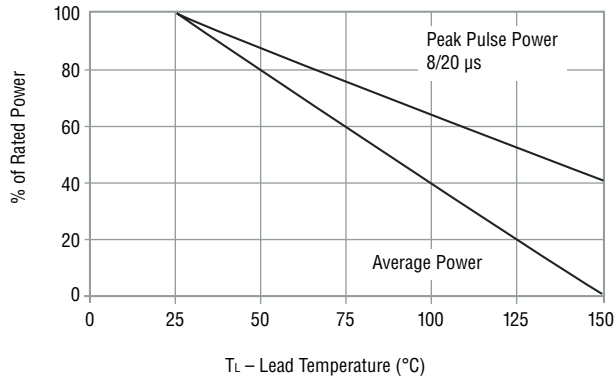
Peak Pulse Power vs Pulse Time



Pulse Wave Form



Power Derating Curve



Reliable Electronic Solutions

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