HD74CDCV857

2.5-V Phase-lock Loop Clock Driver

REJ03D0135–0700Z
(Previous ADE-205-335E (Z))
Preliminary
Rev.7.00
Oct.09.2003

Description

The HD74CDCV857 is a high-performance, low-skew, low-jitter, phase locked loop clock driver. It is specifically designed for use with DDR (Double Data Rate) synchronous DRAMs.

Features

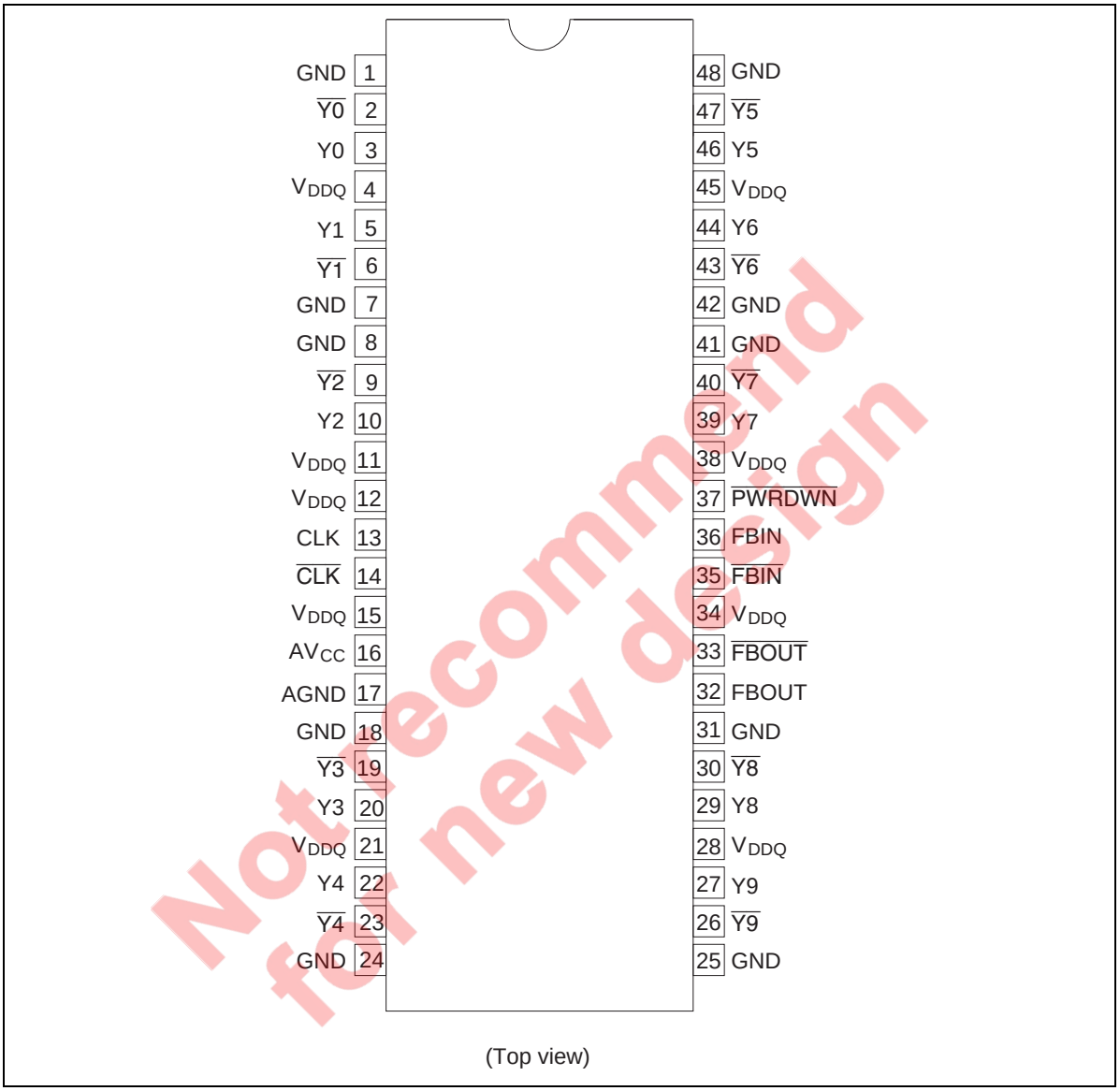
- DDR266 / PC2100-Compliant
- Supports 60 MHz to 170 MHz operation range
- Distributes one differential clock input pair to ten differential clock outputs pairs
- Supports spread spectrum clock requirements meeting the PC100 SDRAM registered DIMM specification
- External feedback pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the outputs to the clock input
- Supports 2.5V analog supply voltage (AV_{CC}), and 2.5 V V_{DDQ}
- No external RC network required
- Sleep mode detection
- 48pin TSSOP (Thin Shrink Small Outline Package)

Function Table

Inputs				:	Outputs				:	
AV_{CC}	$\overline{\text{PWRDWN}}$	CLK	$\overline{\text{CLK}}$	:	Y	$\overline{\text{Y}}$	FBOUT	$\overline{\text{FBOUT}}$	:	PLL
GND	H	L	H	:	L	H	L	H	:	Bypassed / off [*1]
GND	H	H	L	:	H	L	H	L	:	Bypassed / off [*1]
X	L	L	H	:	Z	Z	Z	Z	:	off
X	L	H	L	:	Z	Z	Z	Z	:	off
2.5 V	H	L	H	:	H	L	H	L	:	on
2.5 V	H	H	L	:	H	L	H	L	:	on
2.5 V	X	0 MHz	0 MHz	:	Z	Z	Z	Z	:	off

H : High level
L : Low level
X : Don't care
Z : High impedance
Note: 1. Bypasse mode is used for RENESAS test mode.

Pin Arrangement

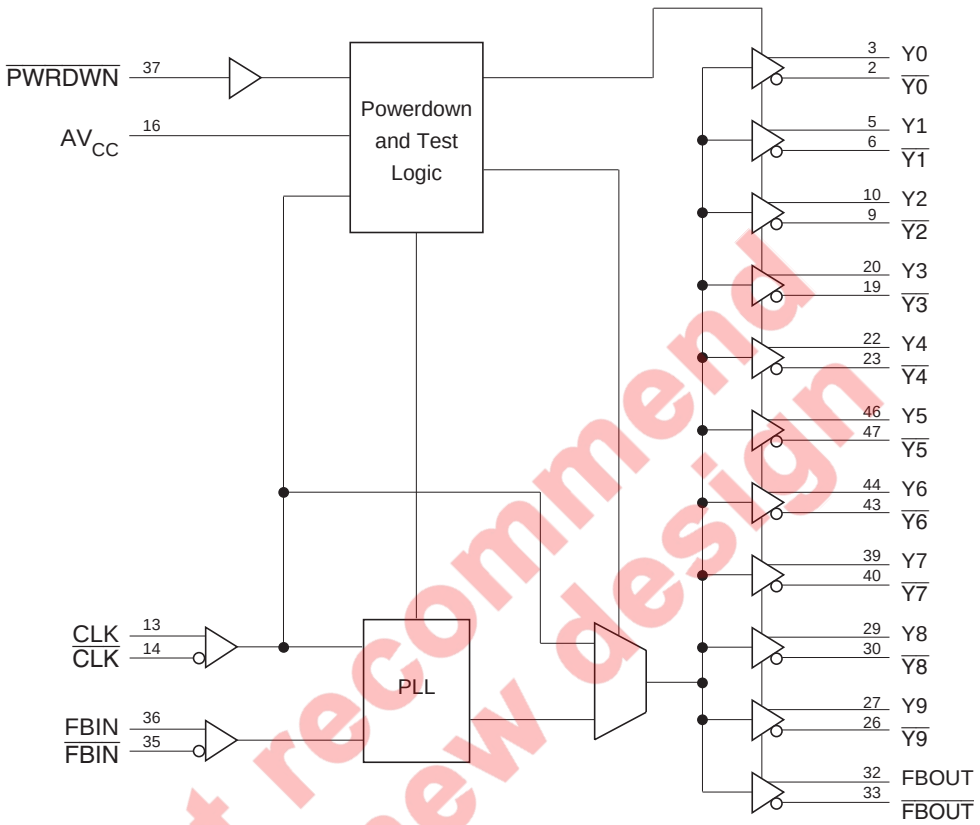


(Top view)

Pin Function

Pin name	No.	Type	Description
AGND	17	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
AV_{CC}	16	Power	Analog power supply. AV_{CC} provides the power reference for the analog circuitry. In addition, AV_{CC} can be used to bypass the PLL for test purposes. When AV_{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. This bypass mode is used for RENESAS test.
CLK, $\overline{CLK}$	13, 14	I Differential input	Clock input. CLK provides the clock signal to be distributed by the HD74CDCV857 clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
$\overline{FBIN}$, FBIN	35, 36	I Differential input	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
FBOUT, $\overline{FBOUT}$	32, 33	O Differential output	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
$\overline{PWRDWN}$	37	I	Output bank enable. $\overline{PWRDWN}$ is the output enable for all outputs. When $\overline{PWRDWN}$ is low, VCO will stop and all outputs are disabled to a high impedance state. When $\overline{PWRDWN}$ will be returned high, PLL will re-synchroniz to CLK frequency and all outputs are enabled.
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	Ground	Ground
V_{DDQ}	4, 11, 12, 15, 21, 28, 34, 38, 45	Power	Power supply
Y	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	O Differential output	Clock outputs. These outputs provide low-skew copies of CLK.
$\overline{Y}$	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	O Differential output	Clock outputs. These outputs provide low-skew copies of $\overline{CLK}$.

Logic Diagram



Note: All inputs and outputs are associated with V_{DDQ} = 2.5 V.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{DDQ}, A_{CC}	–0.5 to 3.6	V	
Input voltage	V_I	–0.5 to V_{DDQ}+0.5	V	
Output voltage [*1]	V_O	–0.5 to V_{DDQ} +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	–50	mA	$V_O < 0$
Continuous output current	I_O	±50	mA	V_O = 0 to V_{DDQ}
Supply current through each V_{DDQ} or GND	I_{VDDQ} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air)		0.7	W	
Storage temperature	T_{stg}	–65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	AV_{CC}	2.3	2.5	2.7	V	
Output supply voltage	V_{DDQ}	2.3	2.5	2.7	V	
DC input signal voltage [*1]		–0.3	—	V_{DDQ}+0.3	V	All pins
High level input voltage	V_{IHG}	1.7	—	V_{DDQ}+0.3	V	$\overline{\text{PWRDWN}}$ input pin
Low level input voltage	V_{ILG}	–0.3	—	0.7	V	$\overline{\text{PWRDWN}}$ input pin
Differential input signal voltage	V_{ID}	0.36	—	V_{DDQ}+0.6	V	
Differential cross point voltage [*2]	V_{IX} V_{OX} [*3]	0.5×V_{DDQ} –0.20	—	0.5×V_{DDQ} +0.20	V	
Output current	I_{OH}	—	—	–12	mA	
	I_{OL}	—	—	12		
Input slew rate	SR	1	—	4	V/ns	20% – 80%
Operating temperature	T_a	0	—	70	°C	

Notes: Inputs pins must be prevent from floating.
Feedback inputs (FBIN, $\overline{\text{FBIN}}$) may float when the device is in low power mode.

1. DC input signal voltage specifies the allowable dc execution of differential input.
2. Differential cross point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing. (See figure1)
3. Guaranteed by design, not 100% tested in production.

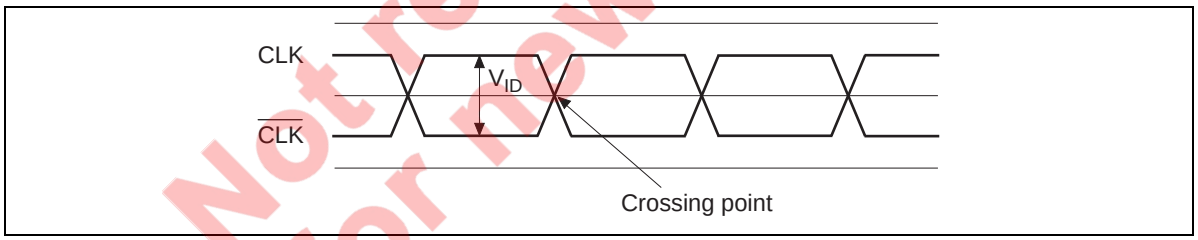


Figure 1 Differential input levels

Electrical Characteristics

Item		Symbol	Min	Typ [*1]	Max	Unit	Test Conditions
Input clamp voltage	CLK, $\overline{CLK}$ FBIN, $\overline{FBIN}$, G	V_{IK}	—	—	–1.2	V	I_I = –18 mA, V_{DDQ} = 2.3 V
Output voltage		V_{OH}	V_{DDQ}–0.2	—	—	V	I_{OH} = –100 µA, V_{DDQ} = 2.3 to 2.7 V
			1.7	—	—		I_{OH} = –12 mA, V_{DDQ} = 2.3 V
		V_{OL}	—	—	0.2		I_{OL} = 100 µA, V_{DDQ} = 2.3 to 2.7 V
			—	—	0.6		I_{OL} = 12 mA, V_{DDQ} = 2.3 V
Input current		I_I	—	—	±10	µA	V_I = 0 V to 2.7 V, V_{DDQ} = 2.7 V
Input capacitance		C_I	2.5	—	3.5	pF	CLK and $\overline{CLK}$, FBIN and $\overline{FBIN}$
Delta input capacitance		C_{DI}	–0.25	—	0.25	pF	CLK and $\overline{CLK}$, FBIN and $\overline{FBIN}$
Supply current		DI_{CC}	—	250	300	mA	f = 170 MHz, V_{DDQ} = AV_{CC} = 2.7 V, All Yx, $\overline{Yx}$ pin = open
		AI_{CC}	—	9	12		
Supply current in power down mode		I_{CCpd}	—	—	100	µA	

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Switching Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Period jitter	t_{PER}	–75	—	75	ps	See figure 6, 9	7, 8
Half period jitter	t_{HPER}	–100	—	100	ps	See figure 7, 9	8, 10
Cycle to cycle jitter	t_{CC}	–75	—	75	ps	See figure 5, 9	10
Static phase offset	t_{SPE}	–75	—	75	ps	See figure 3, 9	4, 5, 9, 10
Output clock skew	t_{sk}	—	—	100	ps	See figure 4, 9	
Operating clock frequency	$f_{CLK(O)}$	60	—	200	MHz	See figure 9	1, 2
Application clock frequency	$f_{CLK(A)}$	95	133	170	MHz	See figure 9	1, 3
Slew rate	t_{SL}	1.0	—	2.0	V/ns	See figure 9	20% – 80%
PLL stabilization time	t_{STAB}	—	—	0.1	ms	See figure 9	6, 10

Notes:
1. The PLL must be able to handle spread spectrum induced skew (the specification for this frequency modulation can be found in the latest Intel PC100 Registered DIMM specification)
2. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters.
3. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
4 Assumes equal wire length and loading on the clock output and feedback path.
5. Static phase offset does not include jitter.
6. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up.
7. Period jitter defines the largest variation in clock period, around anominal clock period.
8. Period jitter and half period jitter are independent from each other.
9. Conditions at V_{DDQ} = 2.5 V, Ta = 25°C.
10. Guaranteed by design, not 100% tested in production.

Differential clock outputs are directly terminated by a 120 Ω resistor. Figure 2 is typical usage conditions of outputs load.

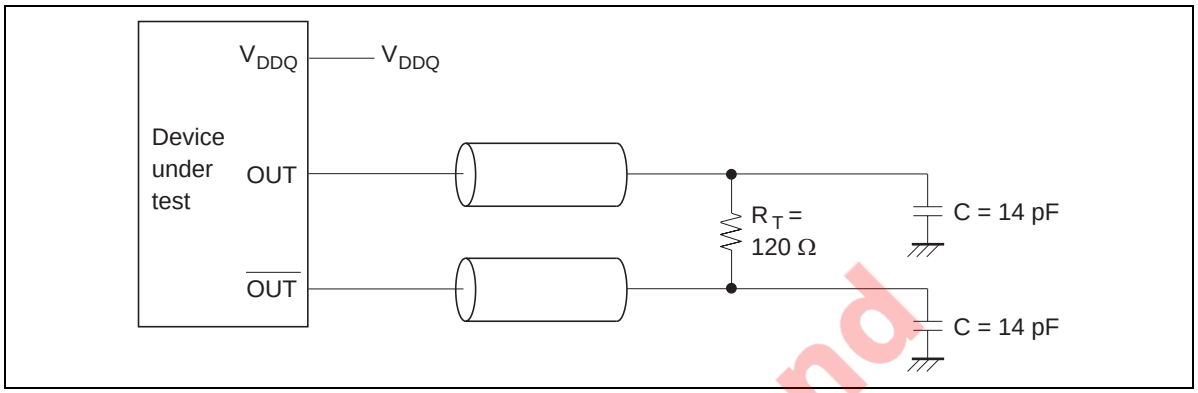


Figure 2 Differential signal using direct termination resistor

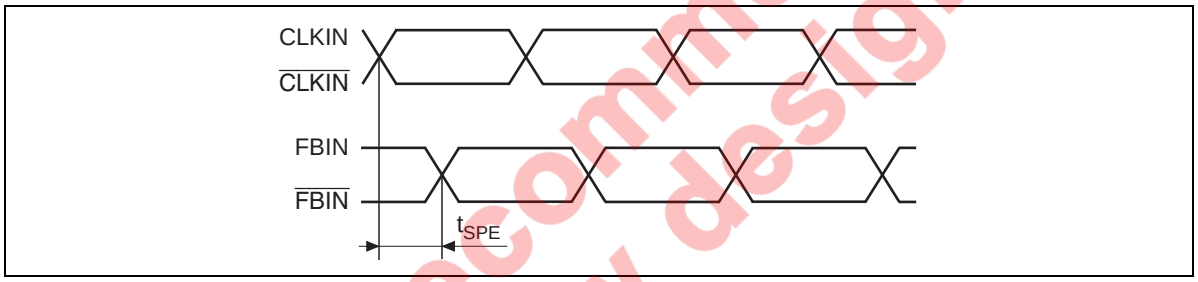


Figure 3 Static phase offset

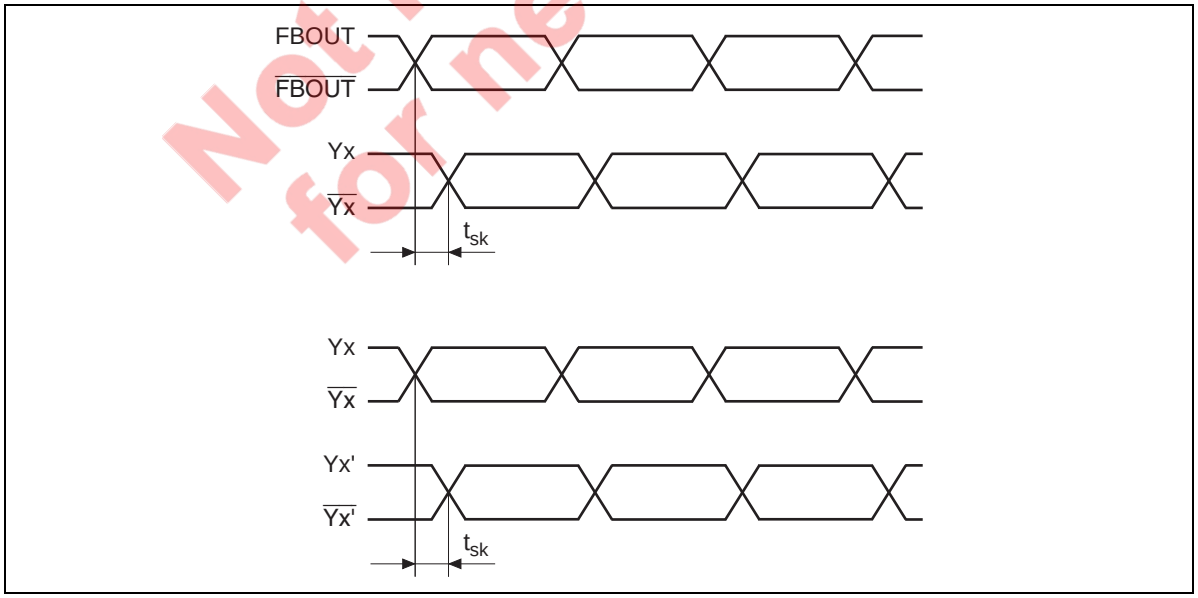


Figure 4 Output skew

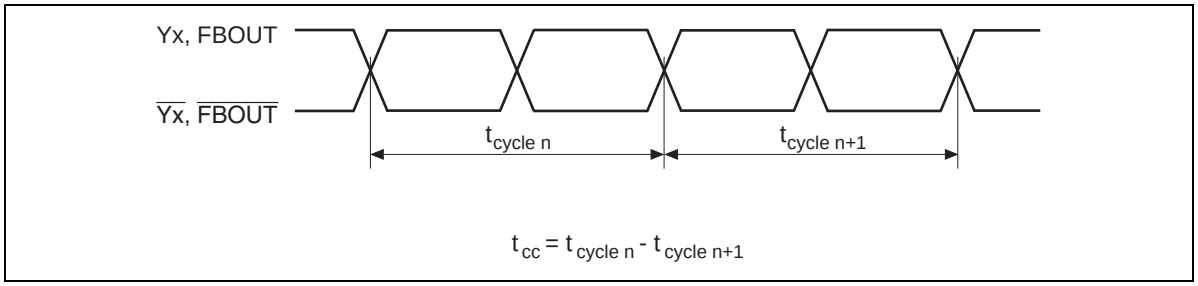


Figure 5 Cycle to cycle jitter

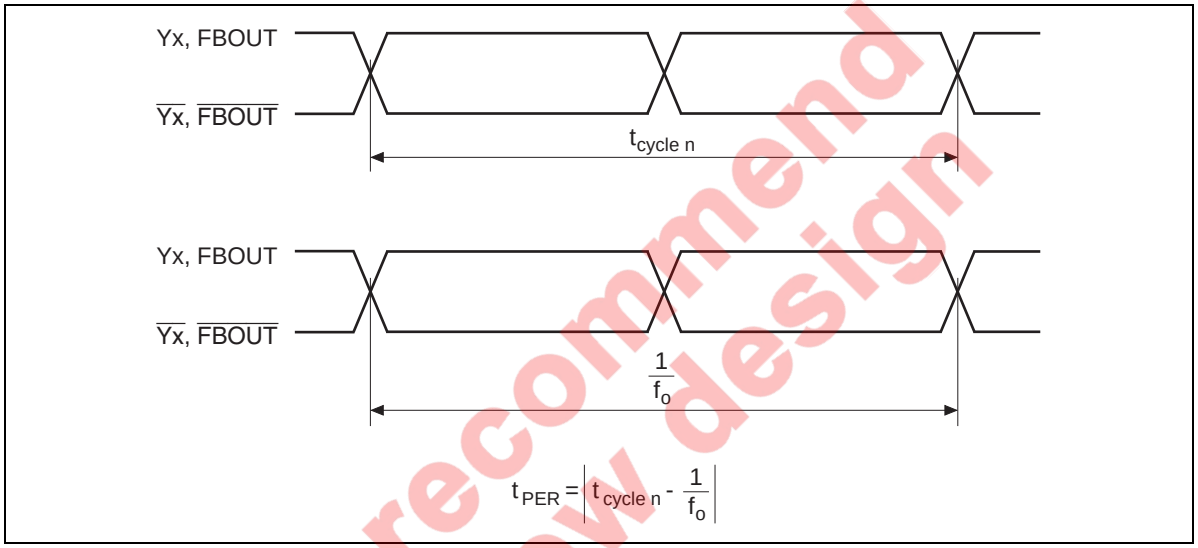


Figure 6 Period jitter

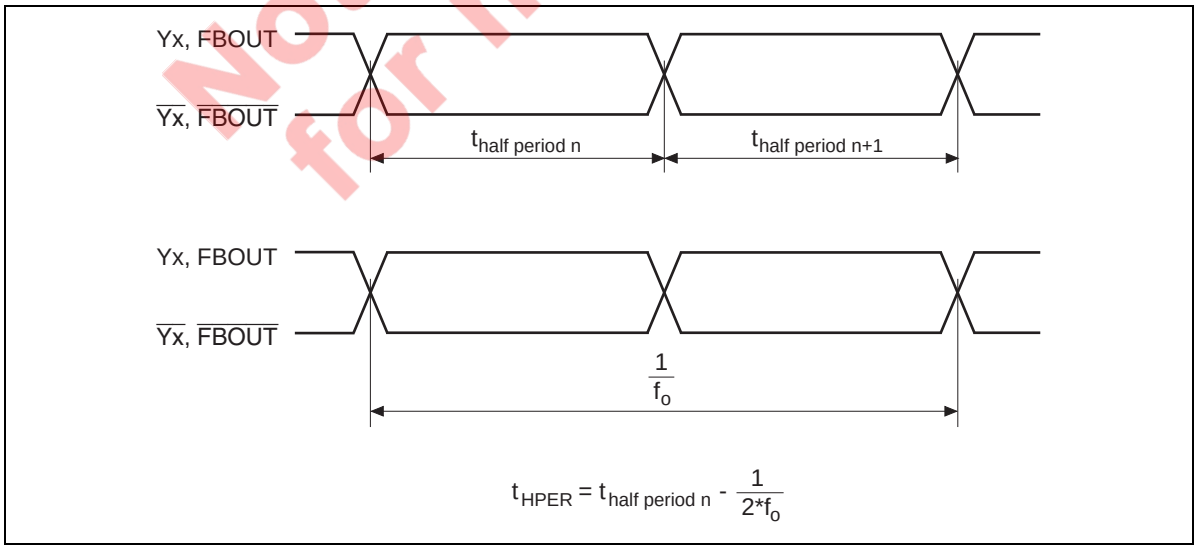


Figure 7 Half period jitter

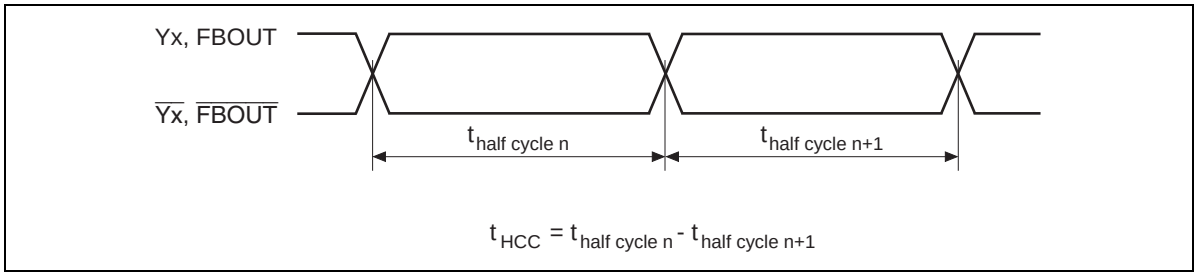


Figure 8 Half cycle to cycle jitter

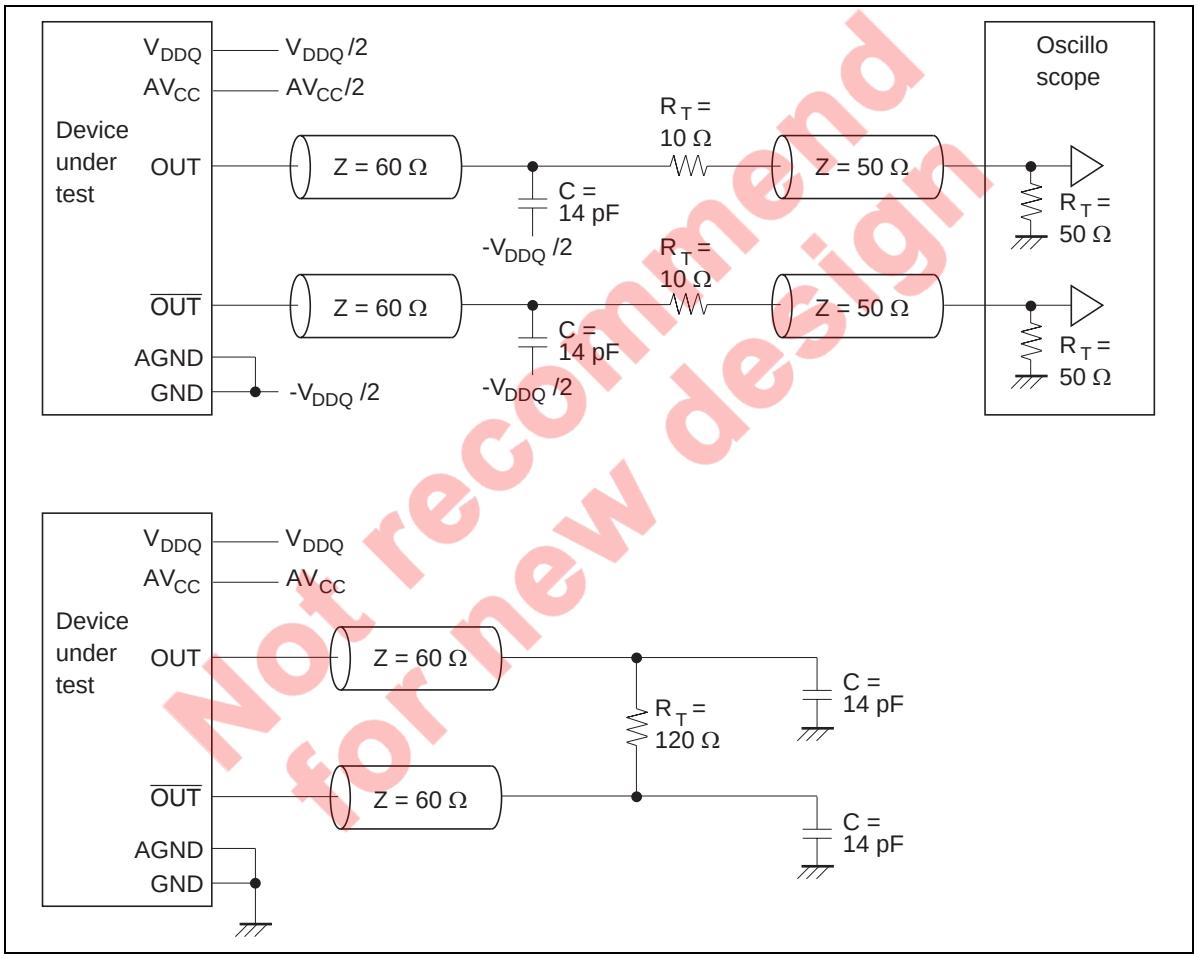
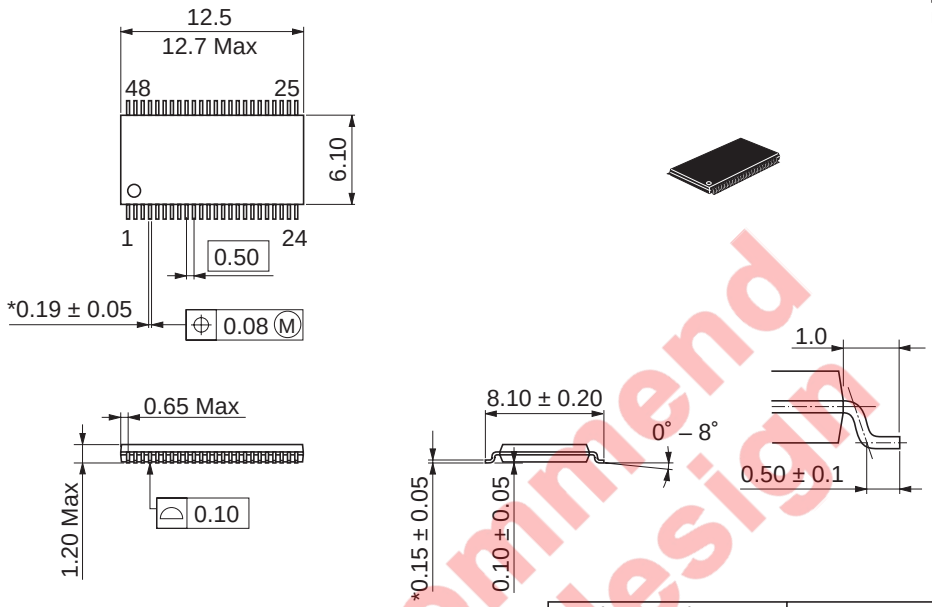


Figure 9 Output load test circuit

Package Dimensions

As of January, 2002

Unit: mm



*Pd plating

Package Code	TTP–48DBV
JEDEC	—
JEITA	—
Mass (reference value)	0.20 g

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