Memory interfaces

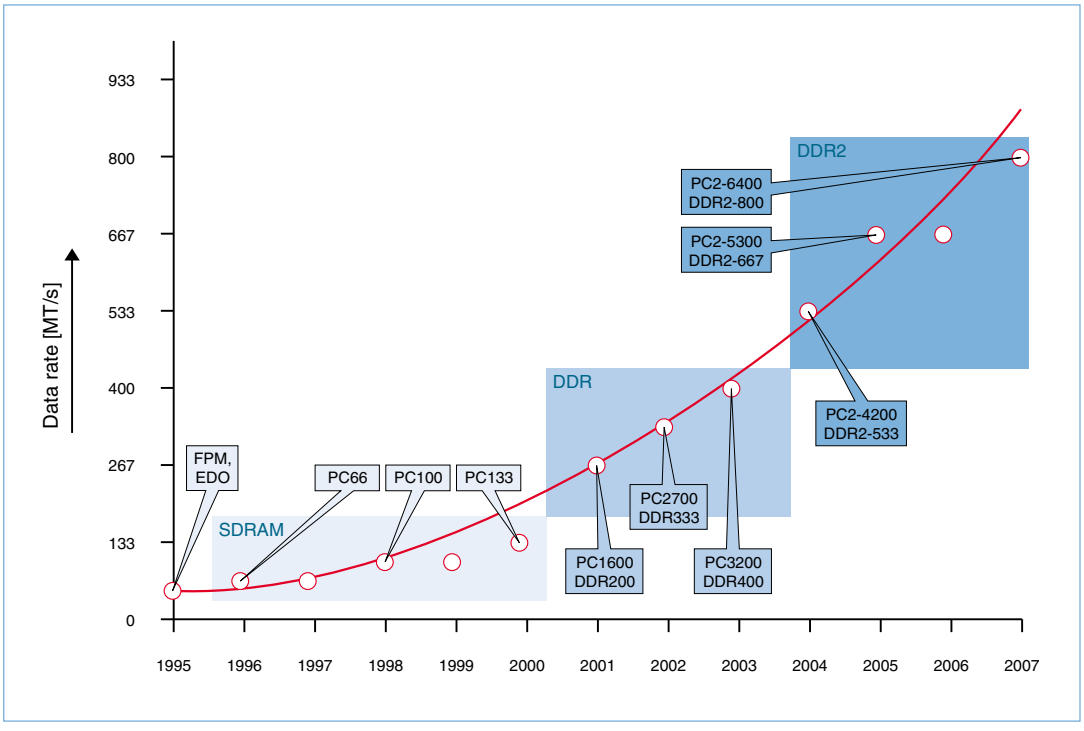
Support logic for memory modules
and other memory subsystems

NXP
founded by Philips

Portfolio overview

PC100 to PC133	• AVC, ALVC, AVCM, and ALVCH series registered drivers • PCK2509 and PCK2510 series PLL clock buffers
DDR200 to DDR266	• SSTV and SSTL series registered drivers • PCKV series PLL clock buffers
DDR333 to DDR400	• SSTVF and SSTVN series registered drivers • PCKVF857 series PLL clock buffers
DDR2-400 to DDR2-533	• SSTU and SSTUH series registered drivers • PCKU877 and PCKU878 PLL clock buffers
DDR2-667 to DDR2-800	• SSTUA and SSTUB series registered drivers • PCKU877 and PCK878 PLLs, and PCKUA clock buffers
Bus switches	• CBTV and CBTU series bus switches, plus DDR and DDR2 bus switches
Specialty memory solutions	• HSTL memory-address latches • Clock and address drivers for NGDIMM • Custom solutions for DDR, DDR2, memory-bus switching

Evolution of memory technology



Enabling bandwidth

The past decade has seen dramatic changes in memory technology. Moving from SDRAM to DDR and DDR2, new process technologies and improvements in design efficiency have led to dramatic increases in capacity and speed.

As a result, memory-intensive systems like servers, workstations, and equipment for networking, telecom, and industrial applications have been able to offer increasing levels of bandwidth.

Memory-support logic can be used to enhance bandwidth by addressing timing issues like jitter, propagation delay/skew and signal buffering/drive. Using the right registers and PLLs can improve timing further, and in some cases – as with DDR1-400 – can even extend a memory technology beyond its original speed target.

NXP, an established supplier of memory interfaces, offers a comprehensive portfolio of memory-support logic that includes registered command and address drivers, PLL clock buffers, and CBTV bus switches for PC100/133 SDRAM, DDR, and DDR2. Available in standard and custom formats, these cost-effective solutions deliver industry-leading speed in a wide range of package options.

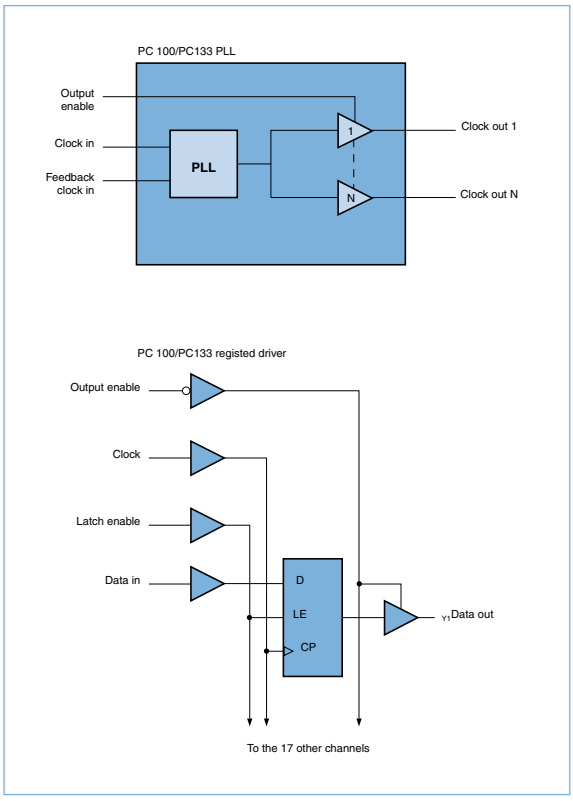
Memory applications

- Registered Dual In-Line Memory Modules (DIMMs)
- Memory subsystems using SDRAM, DDR, DDR2 technology
- Motherboard memory bus switching, buffering, and timing

End-user applications

- Servers
- Graphics and workstations
- Networking equipment
- Telecommunications equipment
- Industrial equipment

NXP memory-interface solutions



PC100 – PC133

This mature memory-module format, based on 3.3-V technology, uses PLLs and registers with single-ended LVTTL (Low Voltage Transistor – Transistor Logic) signaling at clock rates of 100 or 133 MHz. Through the use of SDR (single data rate) clocking, which clocks the data on only one clock edge, the corresponding data rates are 100 and 133 MT/s (megatransfers per second). The PLL is selected according to the memory topology used. Non-parity modules require nine outputs (eight DRAM loads plus one feedback output), parity modules require ten outputs (nine DRAM loads plus one feedback output). All registers have 3-state capability and, to support specific application loading conditions, are equipped with built-in series-termination resistors and Dynamic Controlled Outputs.

- 3.3-V typical supply voltage
- LVTTL signaling
- Single Data Rate (SDR)
- 100- to 133-MT/s data rates
- 100- to 133-MHz clock rates

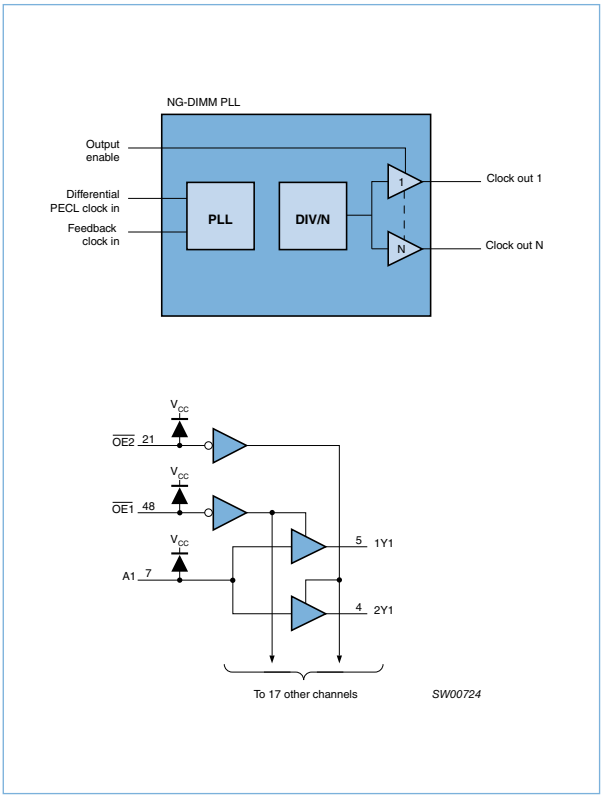
PCK2509SA	50- to 150-MHz 1:9 PLL clock driver
PCK2509SL	50- to 150-MHz 1:9 PLL clock driver with low-power mode
PCK2510SA	50- to 150-MHz 1:10 PLL clock driver
PCK2510SL	50- to 150-MHz 1:10 PLL clock driver with low-power mode
74ALVC16334A	16-bit registered driver with inverted register enable (3-state)
74ALVC162334A	16-bit registered driver with inverted register enable and 30-Ω termination resistors (3-state)
74ALVC16834A	18-bit registered driver with inverted register enable (3-state)
74ALVC162834A	18-bit registered driver with inverted register enable and 30-Ω termination resistors (3-state)
74ALVC16835A	18-bit registered driver (3-state)
74ALVC162835A	18-bit registered driver with 30-Ω termination resistors (3-state)
74ALVC16836A	20-bit registered driver (3-state)
74ALVC162836A	20-bit registered driver with 30-Ω termination resistors (3-state)
74AVCM162834	18-bit registered driver with inverted register enable and 15-Ω termination resistors (3-state)
74AVCM162835	18-bit registered driver with 15-Ω termination resistors (3-state)
74AVCM162836	20-bit registered driver with inverted register enable and 15-Ω termination resistors (3-state)
74AVC16334A	16-bit registered driver with inverted register enable and Dynamic Controlled Outputs (3-state)
74AVC16834A	18-bit registered driver with inverted register enable and Dynamic Controlled Outputs (3-state)
74AVC16835A	18-bit registered driver with Dynamic Controlled Outputs (3-state)
74AVC16836A	20-bit registered driver with inverted register enable and Dynamic Controlled Outputs (3-state)

NG-DIMM

NG-DIMM (Next-generation DIMM) is a proprietary memory-module technology used in servers and workstations.
Like the PC100 and PC133 memory modules, it is based on SDR clocking and a 3.3-V supply voltage. Unlike the PC100 and PC133, however, it accepts a differential PECL clock from the memory controller and then translates and distributes it to the DRAMs using CMOS signaling. The address bus is buffered but not registered, and the address/command buffers are available with or without built-in termination resistors for the data output drivers.

- 3.3-V typical supply voltage
- PECL input clock signaling, LVCMOS data signaling
- Single Data Rate (SDR)
- 100- to 133-MT/s data rates
- 100- to 133-MHz clock rates

PCK953	20- to 125-MHz PECL input / 9 CMOS output 3.3-V PLL clock driver
74ALVCHS16830	18- to 36-bit address driver with bus hold (3-state)
74ALVCHS162830	18- to 36-bit address driver with bus hold (3-state) and 26-Ω termination resistor

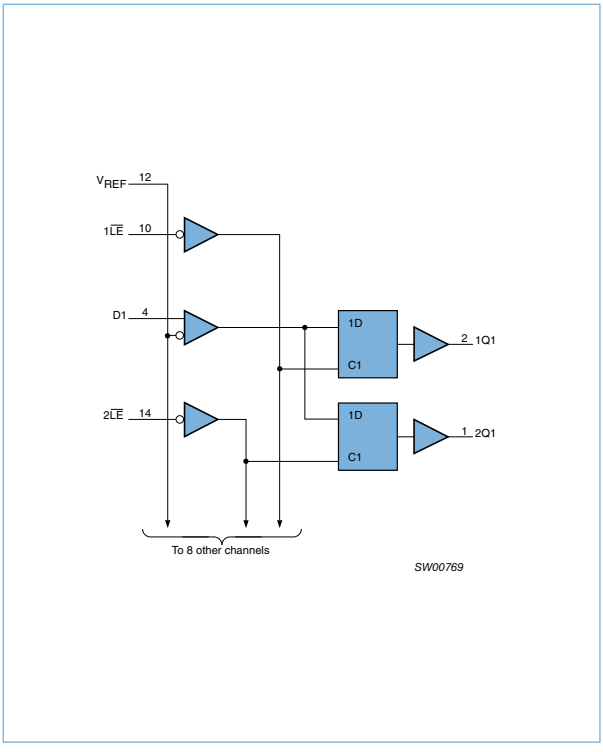


HSTL

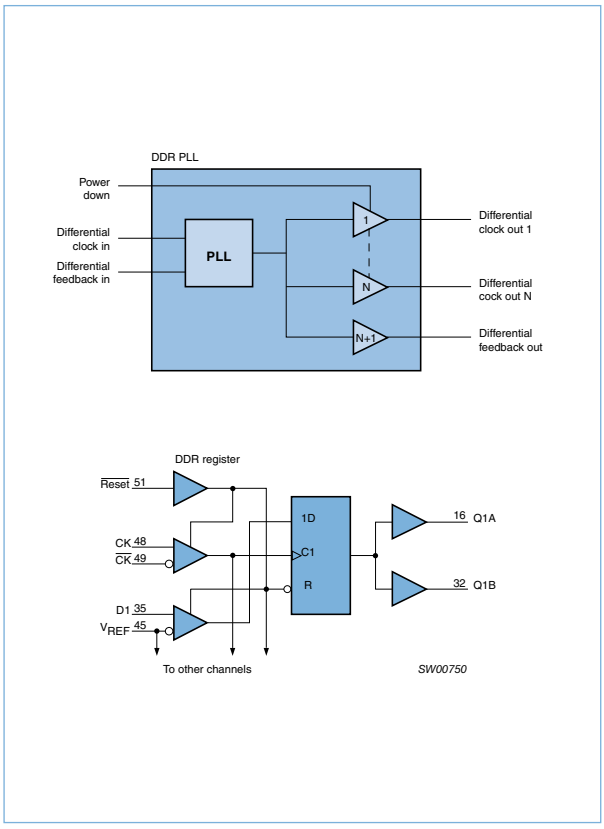
HSTL (High-speed Transceiver Logic) is a common standard based on 1.5-V signaling, typically used to interface between high-speed (100 MHz or higher), high-pin-count CMOS logic devices. NXP provides a set of translators that interface between LVTTL/LVCMOS and HSTL signaling using a 3.3-V typical supply voltage. Both translators comply with HSTL Class III drive type, which uses asymmetrically terminated loads (lines are terminated into a resistor to V_{DD}), and have two buffers per input for a 1:2 fanout. The typical application is latching and redriving an HSTL address bus for two banks of memory.

- 3.3-V typical supply voltage
- HSTL inputs, LVTTL outputs
- Suitable for driving address bus to two banks of memory
- 100- to 133-MHz clock rates

HSTL16918	9- to 18-bit HSTL-to-LVTTL memory address latch
HSTL16919	9- to 18-bit HSTL-to-LVTTL memory address latch with 12-kΩ pull-up resistor



NXP memory-interface solutions



DDR 200 - 266

DDR (Double Data Rate) memory, the most common memory standard shipping today, uses a clocking technique whereby two data bits are transferred per clock cycle, or once every clock edge, to significantly improve speed. Registers and PLLs are used in the Registered DIMMs commonly used in servers and other high-capacity systems, which require high signal integrity independent of the load (that is, the number of DIMMs occupying a slot on a memory bus). DDR memory uses SSTL-2 (stub-series terminated logic, 2.5 V) signaling, with pseudo-differential signaling for the address bus (a reference voltage provides a precise threshold), and, to minimize timing uncertainty, fully differential signaling for the clock signals. The higher speed of DDR memory makes signal integrity, low PLL jitter, and fast register propagation delay times increasingly critical. NXP DDR registers and PLLs are designed with special attention to these essential parameters, so different device speeds incrementally meet the tighter timing specifications associated with each DIMM speed grade – in this case, 200 MT/s at a 100-MHz clock, and 266 MT/s at a 133-MHz clock. Typical application of these devices is on DDR DIMMs, but the PCK2057 integrates an I^2C port for output-enable control and is typically used on the motherboard.

- 2.5-V typical supply voltage
- SSTL_2 (Stub Series Terminated Logic, 2.5-V) signaling
- Double Data Rate (DDR)
- 200- to 266-MT/s data rates
- 100- to 133-MHz clock rates

PCKV857	70- to 190-MHz differential 1:10 clock driver
PCKV857A	100- to 250-MHz differential 1:10 clock driver
PCK2057	70- to 190-MHz differential 1:10 clock driver with I^2C control
SSTV16857	14-bit SSTL_2 registered driver with differential clock inputs
SSTV16859	13-bit 1:2 SSTL_2 registered driver with differential clock inputs for stacked DDR DIMMs

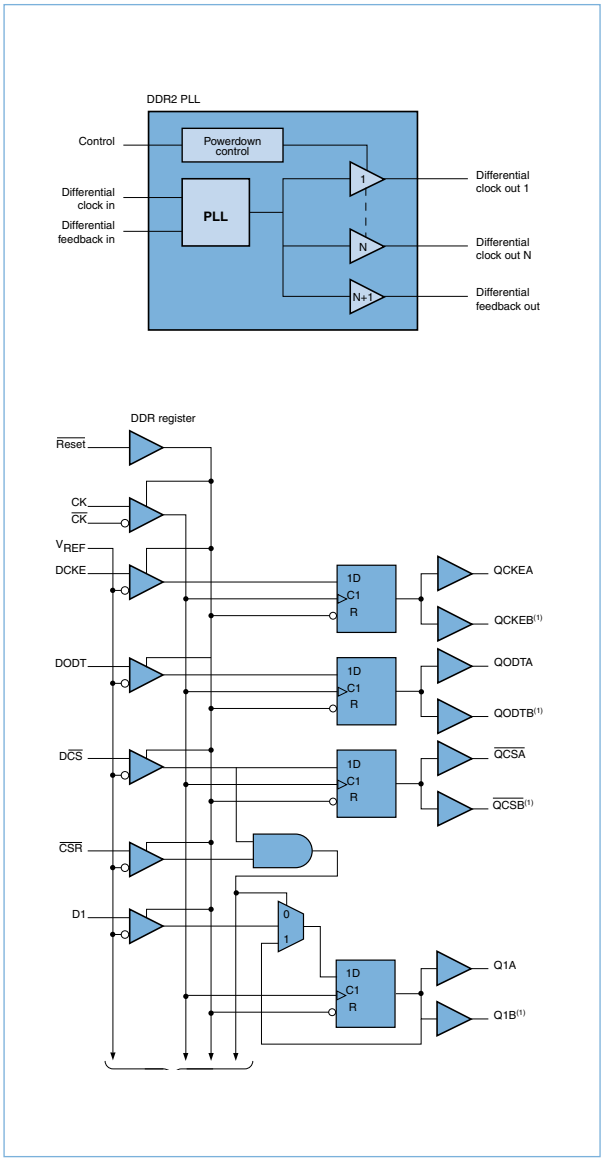
DDR 333 – 400

The higher speed grades of DDR 333-400 (333 and 400 MT/s, using 167 and 200 MHz clock rates) mean tighter timing specifications – especially register propagation delay, PLL jitter, and skew – to support the shorter system clock cycle. In the case of DDR400, the supply voltage to the memory module, and hence to the PLL and register, is increased from the typical 2.5 V ±200 mV to 2.6 V ±100 mV for higher performance.
As with all DDR speed grades, registers are available in a 1:1 configuration for the most common planar DIMM technologies and, for stacked DRAM applications, which have a higher load on the address bus, in 1:2 configurations.

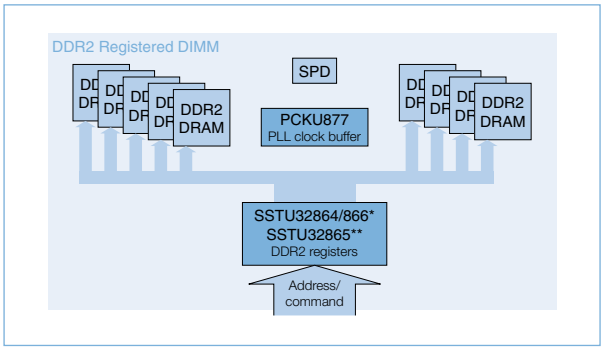
- 2.5-V typical supply voltage (2.6-V supply voltage for DDR-400)
- SSTL_2 signaling
- Double Data Rate (DDR)
- 333- to 400-MT/s data rates
- 167- to 200-MHz clock rates

PCKVF857	60- to 225-MHz differential 1:10 PLL clock driver for DDR200 – DDR400 RDIMMs
SSTVF16857	14-bit 1:1 SSTL_2 registered driver with differential clock inputs for DDR200 – DDR400 RDIMMs
SSTVF16859	13-bit 1:2 SSTL_2 registered driver with differential clock inputs for stacked DDR200 – DDR400 DIMMs
SSTVN16859	13-bit 1:2 SSTL_2 registered driver with differential clock inputs for stacked DDR200 – DDR400 DIMMs

NXP memory-interface solutions



NXP DDR2 PLL and register solution



DDR2 400 – 533

Delivering steady advances in memory density and offering speeds from 400 MT/s to 800 MT/s, DDR2 is the prevailing standard for new memory subsystems. DDR2 registers and PLLs use pseudo-differential SSTL_18 signaling for the address bus (series stub terminated logic, 1.8 V), and differential signaling for the clock, to minimize level-induced skew and jitter. To take advantage of higher DRAM densities while maintaining good signal integrity under heavier loading, NXP offers a normal drive output (SSTU) and a high-drive output (SSTUH) for each register configuration. Graphics workstations and other systems that power-down the memory subsystem benefit from PLLs with faster lock times, which allow for faster sleep recovery.

- 1.8-V typical supply voltage
- SSTL_18 signaling
- Double Data Rate (DDR)
- 400- to 533-MT/s data rates
- 200- to 267-MHz clock rates
- SSTU registers with normal output drive for most common RDIMM applications
- SSTUH registers with high output drive for densely populated or s tacked RDIMM applications
- Output drivers designed for high speed, low overshoot and undershoot, high signal integrity

SSTU32864	1.8-V 25-bit 1:1 or 14-bit 1:2 configurable registered buffer for DDR2 RDIMM applications
SSTU32865	1.8-V 28-bit 1:2 registered buffer with parity for DDR2 RDIMM applications
SSTU32866	1.8-V 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity for DDR2 RDIMM applications
SSTUH32864	1.8-V 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with high output drive for DDR2 RDIMM applications
SSTUH32865	1.8-V 28-bit 1:2 registered buffer with parity and high output drive for DDR2 RDIMM applications
SSTUH32866	1.8-V 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity and high output drive for DDR2 RDIMM applications
PCKU877	1.8-V 1:10 differential zero-delay PLL clock buffer for DDR2 400-533 RDIMM applications
PCKU878	1.8-V 1:10 differential zero-delay PLL clock buffer with fast lock time for DDR2 400-533 RDIMM applications

DDR2 667

The 667 MT/s speed node of DDR2 uses a wider variety of register types with more tightly specified propagation delay times and higher typical operating frequency. As a result, DDR2 667 applications need PLLs with tighter jitter, skew, and offset specifications to meet timing budgets at higher clock rates. The 'A' in SSTUA and PCKUA reflects JEDEC register nomenclature indicating the 667 MT/s specification set. In the case of the 865 and 868 functions, an additional character in the type name (S or D) indicates a single- or dual-die implementation. All NXP registers are single-die implementations, for maximum reliability, lower cost, and uncompromised signal quality.

- 1.8-V typical supply voltage
- SSTL_18 signaling
- Double Data Rate (DDR)
- 400- to 667-MT/s data rates
- 200- to 333-MHz clock rates
- Configurable drive strength for normal or densely populated and stacked RDIMM applications
- 'S' in 32S865 or 32S868 denotes single-die IC implementation. All NXP registers employ single-die implementation for maximum reliability and signal quality
- Output drivers designed for high speed, low overshoot and undershoot, high signal integrity

SSTUA32864	1.8-V 25-bit 1:1 or 14-bit 1:2 configurable registered buffer for DDR2 667 RDIMM applications
SSTUA32S865	1.8-V 28-bit 1:2 registered buffer with parity for DDR2 667 RDIMM applications
SSTUA32866	1.8-V 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity for DDR2 667 RDIMM applications
SSTUA32S868	1.8-V 28-bit 1:2 registered buffer with parity for DDR2 667 RDIMM applications
PCKUA877	1.8-V 1:10 differential zero-delay PLL clock buffer for DDR 667-800 RDIMM applications
PCKUA878	1.8-V 1:10 differential zero-delay PLL clock buffer with fast lock time for DDR2 667-800 RDIMM applications

NXP memory-interface solutions

DDR2 800

The 800 MT/s speed node of DDR2 – designated by JEDEC standard nomenclature with a 'B' in the PLL and register part number – features registers with the lowest absolute propagation delay and the smallest variability in propagation delays to enable 400-MHz clock rates. All devices are single-die implementations.

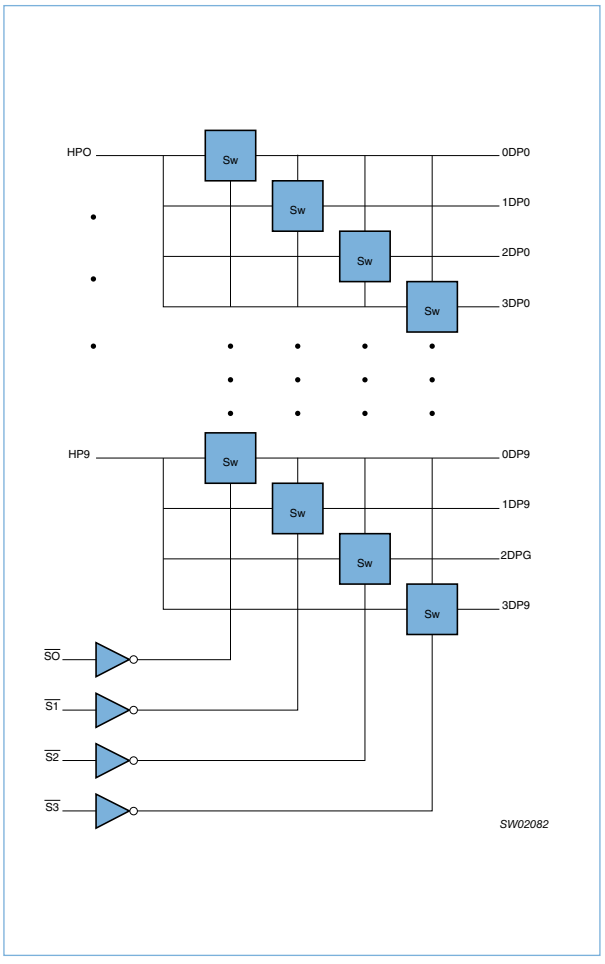
- 1.8-V typical supply voltage
- SSTL_18 signaling
- Double Data Rate (DDR)
- 400- to 800-MT/s data rates
- 200- to 400-MHz clock rates
- Configurable drive strength for normal or densely populated and stacked RDIMM applications
- Two additional chip-select inputs for convenient enabling/disabling on densely populated DIMMs
- All NXP registers use a single-die implementation for maximum reliability and signal quality
- Output drivers designed for high speed, low overshoot and undershoot, high signal integrity

SSTUB32864	1.8-V 25-bit 1:1 or 14-bit 1:2 configurable registered buffer for DDR2 800 RDIMM applications
SSTUB32865	1.8-V 28-bit 1:2 registered buffer with programmable drive strength for DDR2 800 RDIMM applications
SSTUB32866	1.8-V 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity for DDR2 800 RDIMM applications
SSTUB32868	1.8-V 28-bit 1:2 buffer with parity and programmable drive strength for DDR2 800 RDIMM applications
SSTUM32868	1.8-V 28-bit 1:2 registered buffer with parity and permanent high-output drive strength for DDR2 800 RDIMM applications
PCKUA877	1.8-V 1:10 differential zero-delay PLL clock buffer for DDR 667-800 RDIMM applications
PCKUA878	1.8-V 1:10 differential zero-delay PLL clock buffer with fast lock time for DDR2 667-800 RDIMM applications

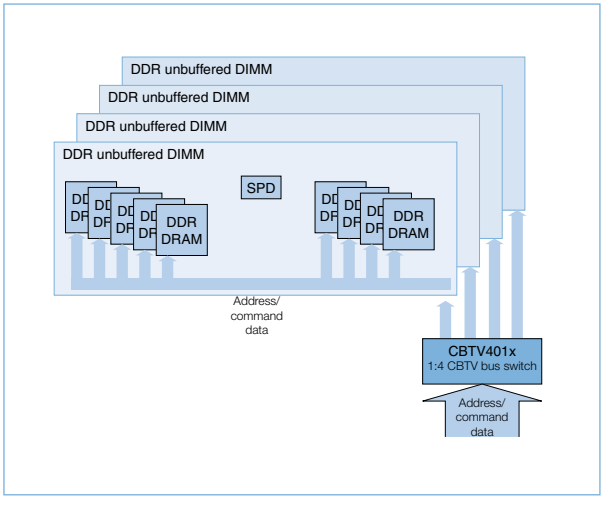
DDR Bus Switches

CBTV bus switches are typically used to expand total memory capacity in a system by providing a switchable, low-impedance path to multiple memory banks while providing high bus isolation to the remaining banks. The 1:2 switches provide a path to two memory banks, the 1:4 switches to four memory banks. CBTV devices implement non-directional MOS switches, designed with an optimum amount of on-resistance, for close impedance matching of the signal path between the memory controller (host port HP) and the DRAM (DIMM port or DP). Simple pin control determines which of the DIMM ports is "on", automatically isolating the remaining DIMM ports. In the off position, the switches provide isolation and pull-down of the unused DIMM port nodes to define idle conditions to a stable low-power state. Low on-capacitance, near-zero propagation delays, and 2.5-V supply voltage operation make CBT switches suitable for use with SSTL_2 signaling in DDR systems up to 400 MT/s.

- 2.5-V typical supply voltage
- Typically used with SSTL_2 signaling
- Low on-resistance with series impedance matching resistor optimized for signal integrity
- Low on-capacitance and fast propagation delays enable data rates of up to 400 Mbps
- 4-DIMM (1:4) and 2-DIMM (1:2), 10-channel or 20-channel configurations



NXP DDR memory bus switch in a typical configuration



CBTU4411	1.8V 11-bit 1:4 DDR2 DRAM multiplexer/bus switch with 12-Ω on-resistance
CBTV4010	2.5-V 10-bit 1:4 DDR SDRAM multiplexer/bus switch with 20-Ω on-resistance
CBTV4011	2.5-V 10-bit 1:4 DDR SDRAM multiplexer/bus switch with 10-Ω on-resistance
CBTV4012	2.5-V 10-bit 1:4 DDR SDRAM multiplexer/bus switch with 10-Ω on-resistance and 400-Ω pull-down
CBTV4020	2.5-V 20-bit 1:2 DDR SDRAM multiplexer/bus switch with 20-Ω on-resistance

PLL clock buffers

Part number	Supply voltage (V)	Output frequency range (MHz)	Input (type)	Outputs (number x type)	Jitter pk-pk (ps)	Output skew (ps)	Phase offset (ps)	Programmability	Operating temperature (°C)	Other features	Packages	Primary application
PCK2509SA	3.3	50 to 150	LVTTL	9 x LVTTL	80	200	125	Pin select	0 to +70	bank output enable, feedback always enabled, bypass	TSSOP-24	PC100/PC133 zero-delay SDRAM clock distribution (JEDEC compliant DIMMs)
PCK2509SL	3.3	50 to 150	LVTTL	9 x LVTTL	80	200	125	Pin select	0 to +70	bank output enable, bypass, low-power mode	TSSOP-24	PC100/PC133 zero-delay SDRAM clock distribution
PCK2510SA	3.3	50 to 150	LVTTL	10 x LVTTL	80	200	125	Pin select	0 to +70	output enable, feedback always enabled, bypass	TSSOP-24	PC100/PC133 zero-delay SDRAM clock distribution (JEDEC compliant DIMMs)
PCK2510SL	3.3	50 to 150	LVTTL	10 x LVTTL	80	200	125	Pin select	0 to +70	output enable, bypass, low-power mode	TSSOP-24	PC100/PC133 zero-delay SDRAM clock distribution
PCK2057	2.5	70 to 190	SSTL-2	11 x SSTL-2	75	75	270	I2C	0 to +70	individual output disable, bypass	TSSOP-48	DDR zero-delay clock distribution
PCK857	2.5; 3.3	66 to 167	SSTL-2	11 x SSTL-2	100	100	150	-	0 to +85	output enable	TSSOP-48	DDR zero-delay clock distribution, DIMMs
PCK953	3.3	50 to 125	Differential PECL	9 x LVCMOS	55	100	60	Pin select	0 to +70	output disable, bypass, 1:18 effective fan-out	LQFP-32	High-performance clock tree design, NG-DIMMs
PCK2059B	2.5	100 to 185	SSTL-2	13 x SSTL-2	75	75	75	I2C	0 to +70	individual output disable, bypass	TFBGA-72	DDR200 - DDR333 zero-delay clock distribution, DIMMs
PCK2159B	2.5	100 to 225	SSTL-2	13 x SSTL-2	75	75	75	I2C	0 to +70	individual output disable, bypass	TFBGA-72	DDR200 - DDR400 zero-delay clock distribution, DIMMs
PCKV857	2.5	60 to 190	SSTL-2	11 x SSTL-2	100	100	150	-	0 to +70	power-down; input frequency detection	TSSOP-48, TVSOP-48, VFBGA-56	DDR200 - DDR266 zero-delay clock distribution, DIMMs
PCKV857A	2.5	100 to 250	SSTL-2	11 x SSTL-2	75	75	50	-	0 to +70	power-down; input frequency detection	TSSOP-48, TVSOP-48, VFBGA-56	DDR200 - DDR333 zero-delay clock distribution, DIMMs
PCKVF2057	2.5	60 to 225	SSTL-2	11 x SSTL-2	35	75	50	I2C	0 to +70	individual output disable, bypass	TSSOP-48	DDR200 - DDR400 zero-delay clock distribution
PCKVF857	2.5	60 to 225	SSTL-2	11 x SSTL-2	35	75	50	Pin select	0 to +70	power-down; input frequency detection	TSSOP-48, TVSOP-48, VFBGA-56	DDR200 - DDR400 zero-delay clock distribution, DIMMs
PCKU877	1.8	125 to 270	Differential clock	11 x differential	40	40	50	Pin select	0 to +70	power-down; selective disable, bypass	VFBGA-52, HVQFN-40	DDR2 400 - 533 zero delay clock distribution, DIMMs
PCKU878	1.8	125 to 270	Differential clock	11 x differential	40	40	50	Pin select	0 to +70	power-down; selective disable, bypass, fast lock time	VFBGA-52, HVQFN-40	DDR2 400 - 533 zero delay clock distribution, DIMMs

Parametric selection tables

Bus switches – DDR

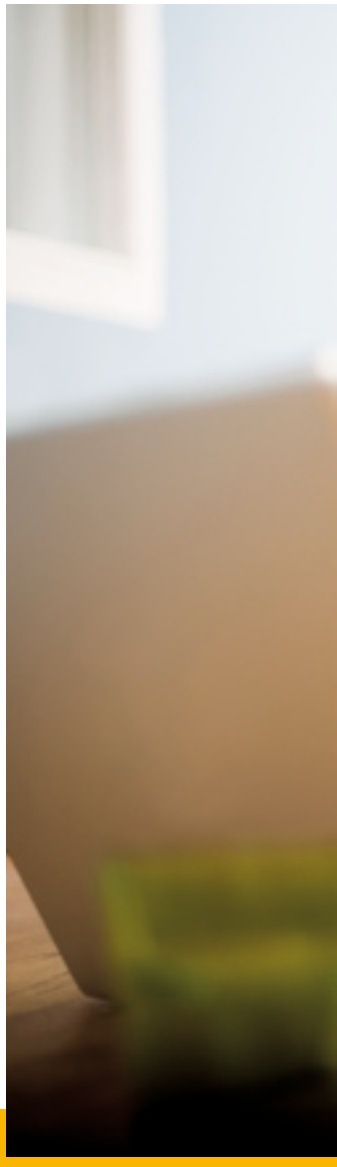
Part number	Supply voltage (V)	Data throughput rate (Mb/s)	Inputs	Outputs	Propagation delay (ps)	On-resistance (Ω)	Operating temperature (°C)	Other features	Packages	Primary application
CBTU4411	1.8	800	11	44	50	12	0 to +85	400-Ω pull-down resistors; differential strobe	TFBGA-72	DDR2 bus switches
CBTV4010	2.5	400	10	40	140	20	0 to +85	100-Ω pull-down resistors	TFBGA-64	DDR bus switch
CBTV4011	2.5	400	10	40	100	10	0 to +85	100-Ω pull-down resistors	TFBGA-64	DDR bus switch
CBTV4012	2.5	400	10	40	100	10	0 to +85	400-Ω pull-down resistors	TFBGA-64	DDR bus switch
CBTV4020	2.5	400	20	40	140	20	0 to +85	100-Ω pull-down resistors	TFBGA-72	DDR bus switch

Registers – SDRAM technology

Part number	Supply voltage (V)	Fmax (MHz)	Inputs	Outputs	Propagation delay A-Y (ns)	Termination resistor (Ω)	Output driver type	Operating temperature (°C)	Other features	Packages	Primary application
74ALVC16334A	1.2 to 3.6	350	16	16	2.3	-	3-state	-40 to +85	inverted register enable	TSSOP-48	PC100 DIMM address/control distribution
74ALVC162334A	1.2 to 3.6	240	16	16	2.9	30	3-state	-40 to +85	inverted register enable	TSSOP-48	PC100 DIMM address/control distribution
74ALVC16834A	1.2 to 3.6	350	18	18	2.3	-	3-state	-40 to +85	inverted register enable	TSSOP-56	PC100 DIMM address/control distribution
74ALVC162834A	1.2 to 3.6	240	18	18	2.9	30	3-state	-40 to +85	inverted register enable	TSSOP-56	PC100 DIMM address/control distribution
74ALVC16835A	1.2 to 3.6	350	18	18	2.3	-	3-state	-40 to +85	-	TSSOP-56	PC100 DIMM address/control distribution
74ALVC162835A	1.2 to 3.6	240	18	18	2.9	30	3-state	-40 to +85	-	TSSOP-56	PC100 DIMM address/control distribution
74ALVC16836A	1.2 to 3.6	350	20	20	2.3	-	3-state	-40 to +85	inverted register enable	TSSOP-56	PC100 DIMM address/control distribution
74ALVC162836A	1.2 to 3.6	240	20	20	2.9	30	3-state	-40 to +85	inverted register enable	TSSOP-56	PC100 DIMM address/control distribution
74AVCM162834	1.2 to 3.6	500	18	18	2	15	3-state	-40 to +85	inverted register enable	TSSOP-56	PC133 DIMM address/control distribution
74AVCM162835	1.2 to 3.6	500	18	18	2	15	3-state	-40 to +85	-	TSSOP-56	PC133 DIMM address/control distribution
74AVCM162836	1.2 to 3.6	500	20	20	2	15	3-state	-40 to +85	inverted register enable	TSSOP-56	PC133 DIMM address/control distribution
74AVC16334A	1.2 to 3.6	500	16	16	1.7	-	Dynamic Controlled Outputs, 3-state	-40 to +85	inverted register enable	TSSOP-48	PC133 DIMM address/control distribution
74AVC16834A	1.2 to 3.6	500	18	18	1.7	-	Dynamic Controlled Outputs, 3-state	-40 to +85	inverted register enable	TSSOP-56, TVSOP-56	PC133 DIMM address/control distribution
74AVC16835A	1.2 to 3.6	500	18	18	1.7	-	Dynamic Controlled Outputs, 3-state	-40 to +85	-	TSSOP-56, TVSOP-56	PC133 DIMM address/control distribution
74AVC16836A	1.2 to 3.6	500	20	20	1.7	-	Dynamic Controlled Outputs, 3-state	-40 to +85	inverted register enable	TSSOP-56, TVSOP-56	PC133 DIMM address/control distribution
74ALVCHS16830	2.3 to 3.6	500	18	36	2	-	3-state	-40 to +85	bus hold on inputs	TVSOP-80	NG-DIMM registered drivers
74ALVCHS162830	2.3 to 3.6	500	18	36	2	26	3-state	-40 to +85	bus hold on inputs	TVSOP-80	NG-DIMM registered drivers
74ALVCH16832	2.3 to 3.6	150	7	28	2.5	-	3-state	-40 to +85	bus hold on inputs; select register/buffer mode	TSSOP-64	registered memory driver
74ALVCHT16835	2.3 to 3.6	150	18	18	2.3	-	3-state	-40 to +85	bus hold on inputs	TVSOP-56	registered memory driver

Registers – DDR and DDR2 technology

Part number	Supply voltage (V)	Fmax (MHz)	Inputs (number x type)	Outputs (number x type)	Propagation delay CLK-Q (ns)	Set-up time DATA-CLK (ns)	Hold time CLK-DATA (ns)	Operating temperature (°C)	Other features	Packages	Primary application
SSTL16857	2.5; 3.3	200	14 x SSTL-2	14 x SSTL-2	1.8	0.8	0.5	0 to +70	master reset	TSSOP-48	DDR SDRAM register
SSTL16877	2.5	200	14 x SSTL-2	14 x SSTL-2	2.4	0.2	1.2	0 to +70	master reset	TSSOP-48	DDR SDRAM register
SSTV16857	2.5	200	14 x SSTL-2	14 x SSTL-2	2.4	0.2	0.75	0 to +70	master reset	TSSOP-48, TVSOP-48. VFBGA-56	DDR SDRAM register
SSTV16857A	2.5	200	14 x SSTL-2	14 x SSTL-2	2.4	0.2	0.75	0 to +70	master reset	TSSOP-48, TVSOP-48. VFBGA-56	DDR SDRAM register
SSTV16859	2.5	200	13 x SSTL-2	26 x SSTL-2	2.4	0.75	0.75	0 to +70	master reset	TSSOP-64, LFBGA-96, HVQFN-56	DDR stacked SDRAM register
SSTVF16857	2.5	210	14 x SSTL-2	14 x SSTL-2	2.6	0.2	0.75	0 to +70	reset	TSSOP-48, TVSOP-48. VFBGA-56	DDR SDRAM register
SSTVF16859	2.5	210	13 x SSTL-2	26 x SSTL-2	2.5	0.65	0.65	0 to +70	master reset	TSSOP-64, LFBGA-96, HVQFN-56	DDR stacked SDRAM register
SSTVN16859	2.5	210	13 x SSTL-2	26 x SSTL-2	2.5	0.65	0.65	0 to +70	master reset	HVQFN-56	DDR stacked SDRAM register
SSTU32864	1.8	450	14 or 25 x SSTL_18	28 or 25 x SSTL_18	1.8	0.5	0.5	0 to +70	basic DDR2 register	LFBGA-96	DDR2 400 - 533 Registered DIMMs
SSTU32865	1.8	450	28 x SSTL_18	56 x SSTL_18	1.8	0.5	0.5	0 to +70	parity function	TFBGA-160	DDR2 400 - 533 2 rank x4 Registered DIMMs
SSTU32866	1.8	450	14 or 25 x SSTL_18	28 or 25 x SSTL_18	1.8	0.5	0.5	0 to +70	parity function	LFBGA-96	DDR2 400 - 533 Registered DIMMs
SSTUH32864	1.8	450	14 or 25 x SSTL_18	28 or 25 x SSTL_18	1.8	0.5	0.5	0 to +70	high output drive	LFBGA-96	DDR2 400 - 533 Registered DIMMs, stacked or dual density
SSTUH32865	1.8	450	28 x SSTL_18	56 x SSTL_18	1.8	0.5	0.5	0 to +70	parity function, high output drive	TFBGA-160	DDR2 400 - 533 2 rank x4 Registered DIMMs, stacked or dual density
SSTUH32866	1.8	450	14 or 25 x SSTL_18	28 or 25 x SSTL_18	1.8	0.5	0.5	0 to +70	parity function, high output drive	LFBGA-96	DDR2 400 - 533 Registered DIMMs, stacked or dual density
SSTUA32864	1.8	450	14 or 25 x SSTL_18	28 or 25 x SSTL_18	1.8	0.5	0.5	0 to +70	high output drive	LFBGA-96	DDR2 400 - 667 Registered DIMMs, stacked or dual density
SSTUA32S865	1.8	450	28 x SSTL_18	56 x SSTL_18	1.8	0.5	0.5	0 to +70	parity function, high output drive	TFBGA-160	DDR2 400 - 667 2 rank x4 Registered DIMMs, stacked or dual density
SSTUA32866	1.8	450	14 or 25 x SSTL_18	28 or 25 x SSTL_18	1.8	0.5	0.5	0 to +70	parity function, high output drive	LFBGA-96	DDR2 400 - 667 Registered DIMMs, stacked or dual density
SSTUA32S868	1.8	450	28 x SSTL_18	56 x SSTL_18	1.8	0.5	0.5	0 to +70	parity function, high output drive, configurable pinout	TFBGA-176	DDR2 400 - 667 2 rank x4 Registered DIMMs, stacked or dual density



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Date of release: November 2006
Document order number: 9397 750 15761
Printed in the Netherlands

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PHILIPS