



16K-Bit CMOS PARALLEL EEPROM

FEATURES

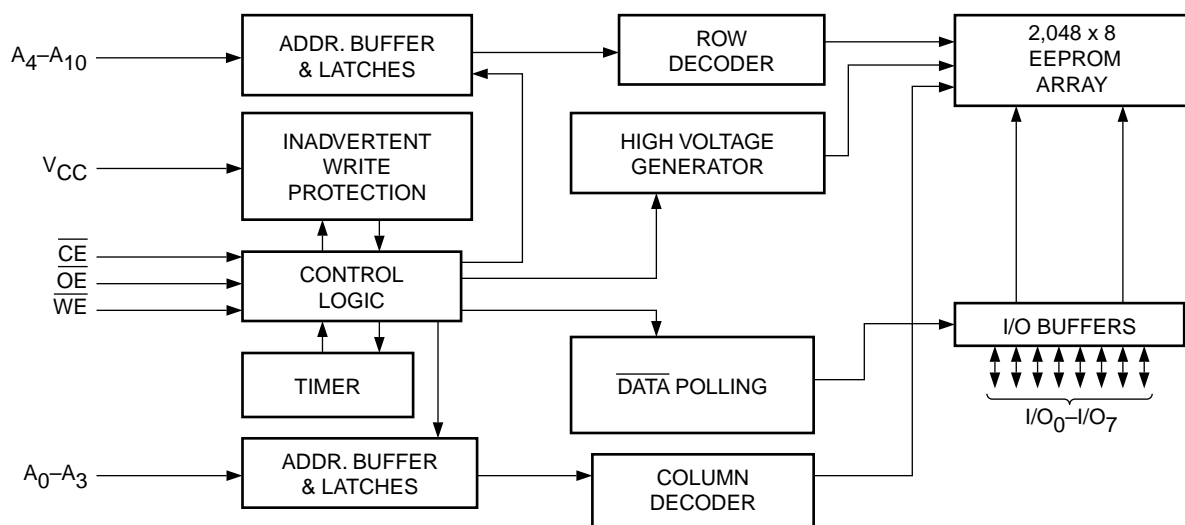
- Fast read access times: 90 ns, 120 ns, 200 ns
- Low power CMOS cissipation:
 - Active: 25 mA Max.
 - Standby: 100 μ A Max.
- Simple write operation:
 - On-chip address and data latches
 - Self-timed write cycle with auto-clear
- Fast write cycle time: 10ms max
- End of write detection: $\overline{\text{DATA}}$ polling
- Hardware write protection
- CMOS and TTL compatible I/O
- 10,000 or 100,000 Program/erase cycles
- 10 or 100 year data retention
- Commercial, industrial and automotive temperature ranges

DESCRIPTION

The CAT28C16A is a fast, low power, 5V-only CMOS Parallel EEPROM organized as 2K x 8-bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and V_{CC} power up/down write protection eliminate additional timing and protection hardware. $\overline{\text{DATA}}$ Polling signals the start and end of the self-timed write cycle. Additionally, the CAT28C16A features hardware write protection.

The CAT28C16A is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 10,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 24-pin DIP and SOIC or 32-pin PLCC packages.

BLOCK DIAGRAM

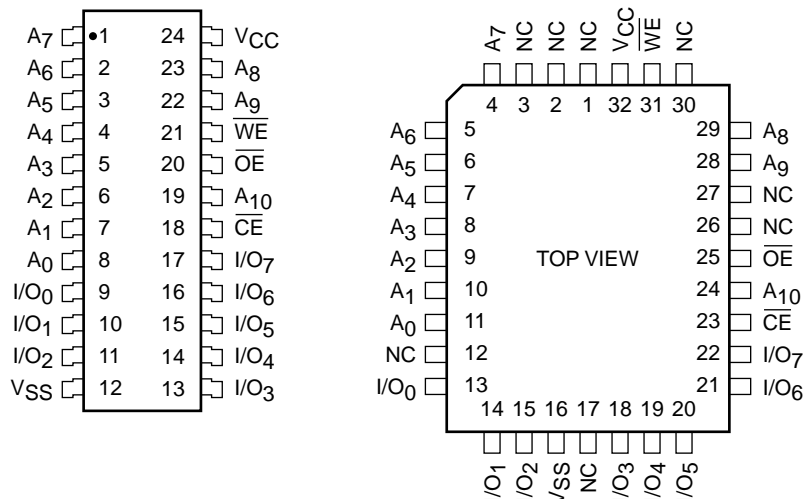


PIN CONFIGURATION

DIP Package (P, L)

SOIC Package (J, K, W, X)

PLCC Package (N, G)



PIN FUNCTIONS

Pin Name	Function
A ₀ –A ₁₀	Address Inputs
I/O ₀ –I/O ₇	Data Inputs/Outputs
CE	Chip Enable
OE	Output Enable
WE	Write Enable
V _{CC}	5V Supply
V _{SS}	Ground
NC	No Connect

MODE SELECTION

Mode	CE	WE	OE	I/O	Power
Read	L	H	L	D _{OUT}	ACTIVE
Byte Write (WE Controlled)	L		H	D _{IN}	ACTIVE
Byte Write (CE Controlled)		L	H	D _{IN}	ACTIVE
Standby, and Write Inhibit	H	X	X	High-Z	STANDBY
Read and Write Inhibit	X	H	H	High-Z	ACTIVE

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
C _{I/O} ⁽¹⁾	Input/Output Capacitance	10	pF	V _{I/O} = 0V
C _{IN} ⁽¹⁾	Input Capacitance	6	pF	V _{IN} = 0V

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground ⁽²⁾	–2.0V to +V _{CC} + 2.0V
V _{CC} with Respect to Ground	–2.0V to +7.0V
Package Power Dissipation Capability (T _a = 25°C)	1.0W
Lead Soldering Temperature (10 secs)	300°C
Output Short Circuit Current ⁽³⁾	100 mA

***COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
N _{END} ^(1, 7)	Endurance	100,000		Cycles/Byte
T _{DR} ^(1, 7)	Data Retention	100		Years
V _{ZAP} ⁽¹⁾	ESD Susceptibility	2000		Volts
I _{LTH} ⁽¹⁾⁽⁴⁾	Latch-Up	100		mA

D.C. OPERATING CHARACTERISTICS

V_{CC} = 5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
I _{CC}	V _{CC} Current (Operating, TTL)			35	mA	$\overline{CE} = \overline{OE} = V_{IL}$, f = 1/t _{RC} min, All I/O's Open
I _{CCC} ⁽⁵⁾	V _{CC} Current (Operating, CMOS)			25	mA	$\overline{CE} = \overline{OE} = V_{ILC}$, f = 1/t _{RC} min, All I/O's Open
I _{SB}	V _{CC} Current (Standby, TTL)			1	mA	$\overline{CE} = V_{IH}$, All I/O's Open
I _{SBC} ⁽⁶⁾	V _{CC} Current (Standby, CMOS)			100	μA	$\overline{CE} = V_{IHC}$, All I/O's Open
I _{LI}	Input Leakage Current	–10		10	μA	V _{IN} = GND to V _{CC}
I _{LO}	Output Leakage Current	–10		10	μA	V _{OUT} = GND to V _{CC} , $\overline{CE} = V_{IH}$
V _{IH} ⁽⁶⁾	High Level Input Voltage	2		V _{CC} + 0.3	V	
V _{IL} ⁽⁵⁾	Low Level Input Voltage	–0.3		0.8	V	
V _{OH}	High Level Output Voltage	2.4			V	I _{OH} = –400μA
V _{OL}	Low Level Output Voltage			0.4	V	I _{OL} = 2.1mA
V _{WI}	Write Inhibit Voltage	3.0			V	

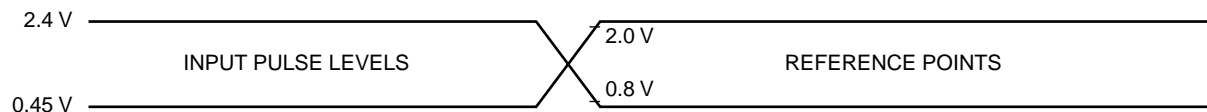
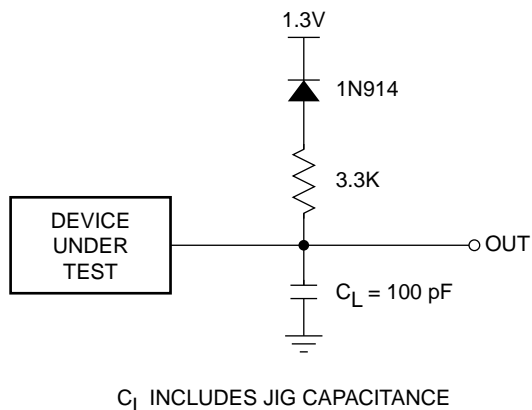
Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20 ns.
- (3) Output shorted for no more than one second. No more than one output shorted at a time.
- (4) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.
- (5) V_{ILC} = –0.3V to +0.3V.
- (6) V_{IHC} = V_{CC} – 0.3V to V_{CC} + 0.3V.
- (7) For the CAT28C16A-20, the minimum endurance is 10,000 cycles and the minimum data retention is 10 years.

A.C. CHARACTERISTICS, Read Cycle

$V_{CC} = 5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	28C16A-90		28C16A-12		28C16A-20		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	90		120		200		ns
t_{CE}	\overline{CE} Access Time		90		120		200	ns
t_{AA}	Address Access Time		90		120		200	ns
t_{OE}	\overline{OE} Access Time		50		60		80	ns
$t_{LZ}^{(1)}$	\overline{CE} Low to Active Output	0		0		0		ns
$t_{OLZ}^{(1)}$	\overline{OE} Low to Active Output	0		0		0		ns
$t_{HZ}^{(1)(2)}$	\overline{CE} High to High-Z Output		50		50		55	ns
$t_{OHZ}^{(1)(2)}$	\overline{OE} High to High-Z Output		50		50		55	ns
$t_{OH}^{(1)}$	Output Hold from Address Change	0		0		0		ns

Figure 1. A.C. Testing Input/Output Waveform(3)**Figure 2. A.C. Testing Load Circuit (example)**

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.
- (3) Input rise and fall times (10% and 90%) < 10 ns.

A.C. CHARACTERISTICS, Write Cycle

$V_{CC} = 5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	28C16A-90		28C16A-12		28C16A-20		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time		5		5		10	ms
t_{AS}	Address Setup Time	0		0		10		ns
t_{AH}	Address Hold Time	100		100		100		ns
t_{CS}	\overline{CE} Setup Time	0		0		0		ns
t_{CH}	\overline{CE} Hold Time	0		0		0		ns
$t_{CW}^{(2)}$	\overline{CE} Pulse Time	110		110		150		ns
t_{OES}	\overline{OE} Setup Time	0		0		15		ns
t_{OEH}	\overline{OE} Hold Time	0		0		15		ns
$t_{WP}^{(2)}$	\overline{WE} Pulse Width	110		110		150		ns
t_{DS}	Data Setup Time	60		60		50		ns
t_{DH}	Data Hold Time	0		0		10		ns
t_{DL}	Data Latch Time	5	10	5	10	50		ns
$t_{INIT}^{(1)}$	Write Inhibit Period After Power-up	.05	100	.05	100	5	20	ms

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

(2) A write pulse of less than 20ns duration will not initiate a write cycle.

DEVICE OPERATION

Read

Data stored in the CAT28C16A is transferred to the data bus when \overline{WE} is held high, and both \overline{OE} and \overline{CE} are held

low. The data bus is set to a high impedance state when either \overline{CE} or \overline{OE} goes high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

Figure 3. Read Cycle

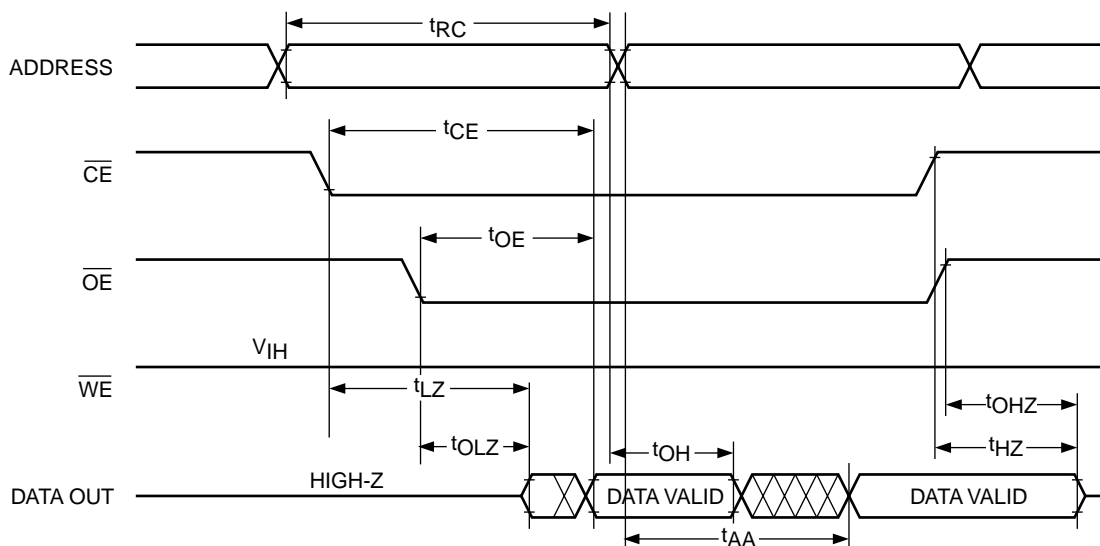
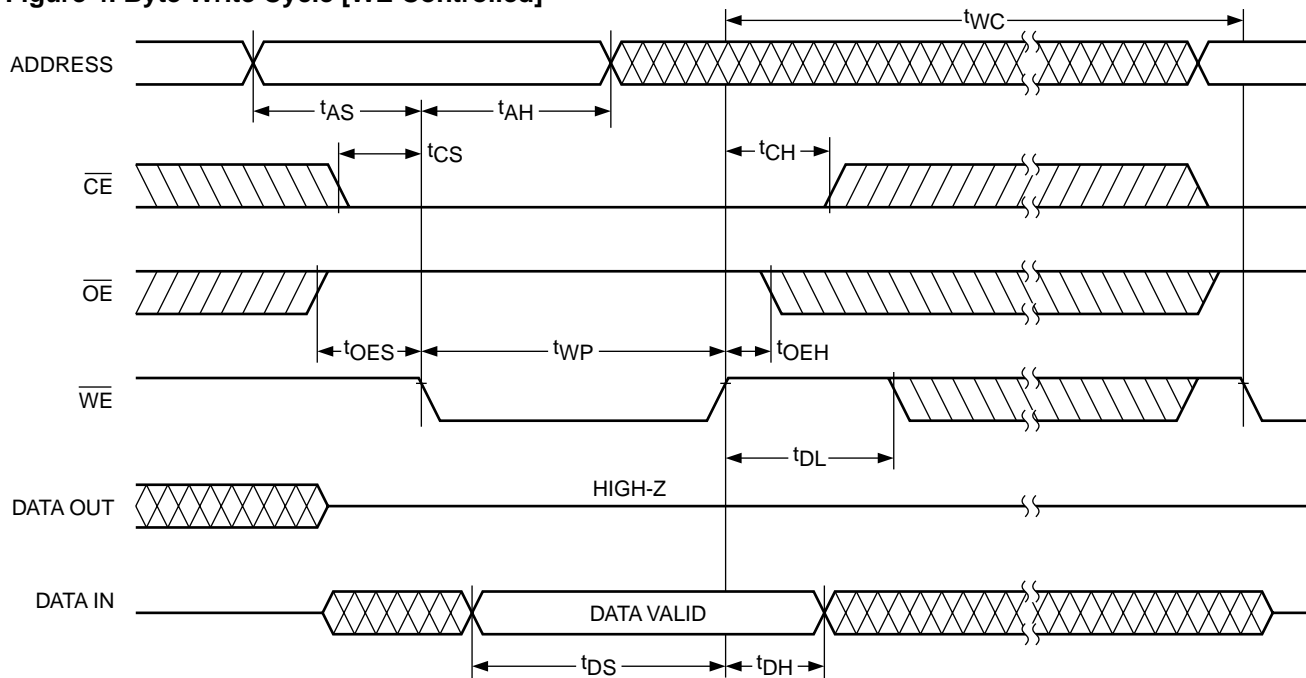


Figure 4. Byte Write Cycle [\overline{WE} Controlled]



Byte Write

A write cycle is executed when both $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are low, and $\overline{\text{OE}}$ is high. Write cycles can be initiated using either $\overline{\text{WE}}$ or $\overline{\text{CE}}$, with the address input being latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10 ms.

DATA Polling

$\overline{\text{DATA}}$ polling is provided to indicate the completion of a byte write cycle. Once a byte write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O₇ (I/O₀–I/O₆ are indeterminate) until the programming cycle is complete. Upon completion of the self-timed byte write cycle, all I/O's will output true data during a read cycle.

Figure 5. Byte Write Cycle [$\overline{\text{CE}}$ Controlled]

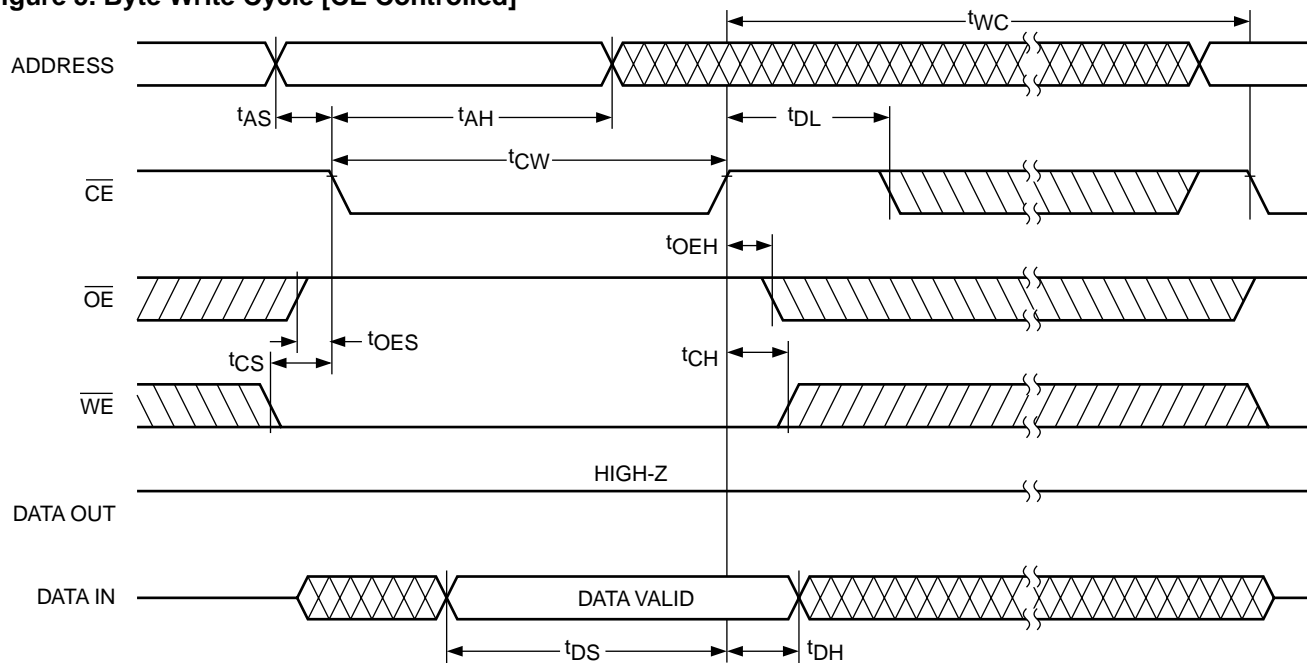
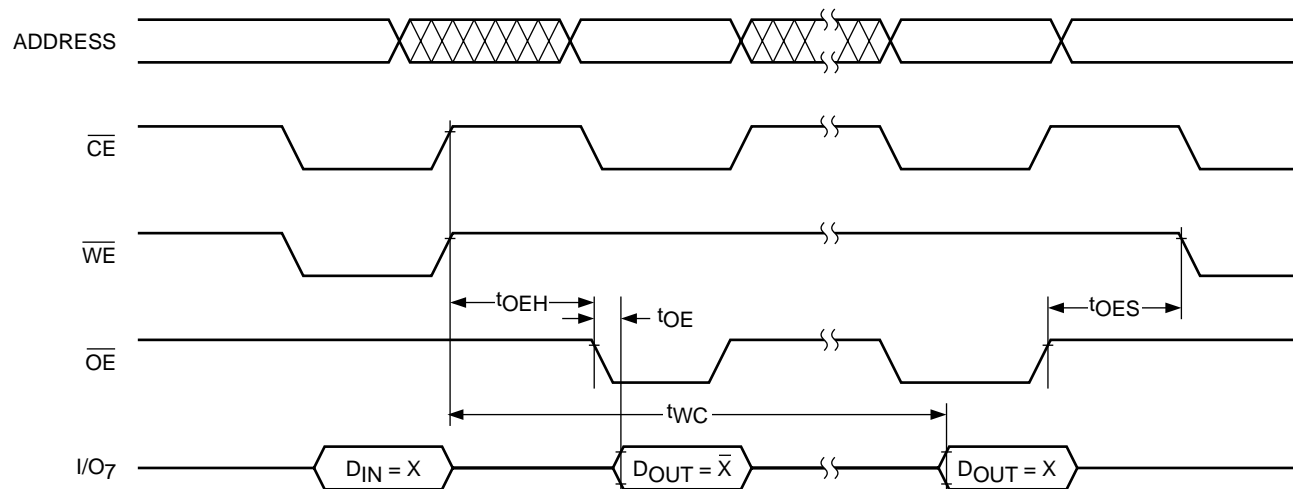


Figure 6. DATA Polling



HARDWARE DATA PROTECTION

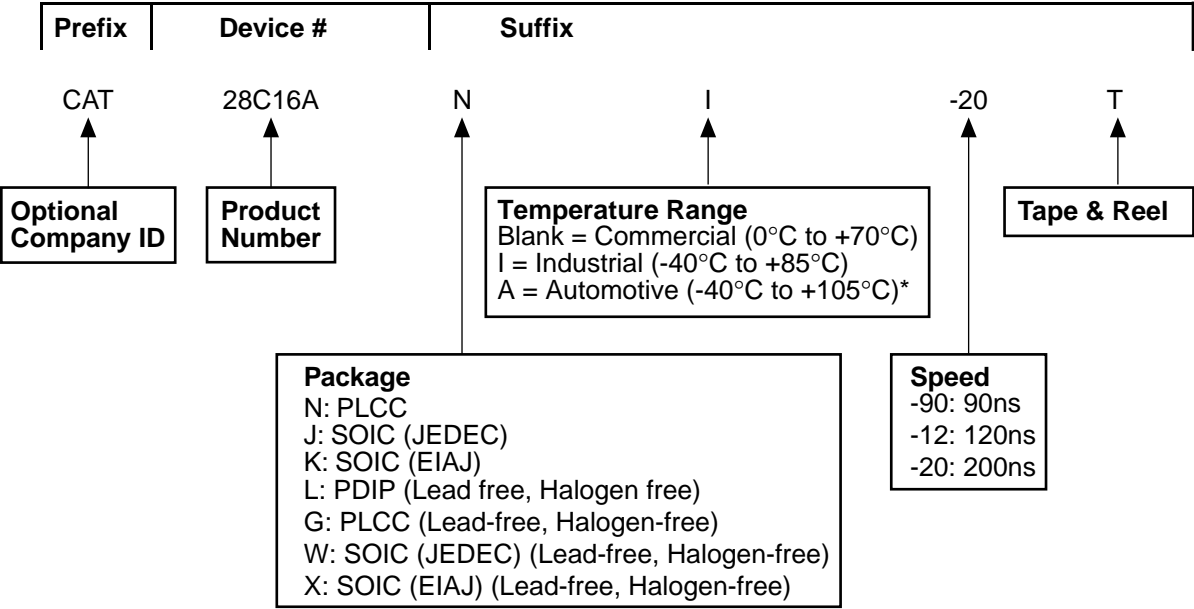
The following is a list of hardware data protection features that are incorporated into the CAT28C16A.

- (1) V_{CC} sense provides for write protection when V_{CC} falls below 3.0V min.
- (2) A power on delay mechanism, t_{INIT} (see AC charac-

teristics), provides a 5 to 20 ms delay before a write sequence, after V_{CC} has reached 3.0V min.

- (3) Write inhibit is activated by holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high.
- (4) Noise pulses of less than 20 ns on the \overline{WE} or \overline{CE} inputs will not result in a write cycle.

ORDERING INFORMATION




* -40°C to +125°C is available upon request

Notes:
(1) The device used in the above example is a CAT28C16ANI-20T (PLCC, Industrial temperature, 200 ns Access Time, Tape & Reel).

REVISION HISTORY

Date	Revision	Description
30-Mar-04	A	Added Green packages in all areas
19-Apr-04	B	Delete data sheet designation Update Block Diagram Update Ordering Information Update Revision History Update Rev Number
21-Sep-04	C	Update Features Update AC Characteristics tables Update Ordering Information
22-Sep-04	D	Minor changes
24-Nov-08	E	Update Ordering Information - Adding L-PDIP package Change logo and fine print to ON Semiconductor

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