

Linear codec IC for digital cellular telephones

BU8730KV

The BU8730KV is a linear codec IC developed for use with digital cellular telephones. It contains a 14-bit precision linear codec and various other analog input / output features.

Also, there is a built-in DAI and many tone signal functions making this IC perfect for use with GSM cellular telephones.

●Applications

Digital cellular telephones

●Features

- 1) +3V single power supply ($V_{DD} = 2.7V$ to $3.3V$).
- 2) Low current consumption of 8.2mA (typ.) when fully operating and 20 μA (max.) when powered down ($V_{DD} = 3V$).
- 3) Built-in 14-bit precision linear codec.
- 4) Transmission filter for the codec unit conforms to ITU-T recommendation G.714.
- 5) DTMF signal, GSM triple tone, and scale tone signal generator functions are built into the tone signal generator block.
- 6) Signal generator and output level adjustment circuits are built in with the sounder output functions.
- 7) Built-in PLL circuit for system clock generation.
- 8) Analog input / output functions:
 - Built-in mic amplifier with gain switching capabilities.
 - Data signal I / O circuit allows for connection to external devices.
 - Receiver output, ringer output, and EXT output are soft mute compatible.
- 9) Internal DAI (digital audio interface) with GSM11.10 support.
- 10) Internal DSP interface circuit supports multiple DSP formats.
- 11) VQFP 48-pin package.

●Absolute maximum ratings ($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Digital power supply voltage	DV_{DD}	$-0.3 \sim +4.5$	V
Analog power supply voltage	RXV_{DD}	$-0.3 \sim +4.5$	V
	TXV_{DD}	$-0.3 \sim +4.5$	V
Digital input voltage	V_{DIN}	$DV_{SS} - 0.3 \sim DV_{DD} + 0.3$	V
Analog input voltage	V_{AIN}	$RXGND - 0.3 \sim RXV_{DD} + 0.3$	V
		$TXGND - 0.3 \sim TXV_{DD} + 0.3$	V
Input current	I_{IN}	$-10 \sim +10$	mA
Power dissipation	P_d	400*1	mW
Operating temperature	T_{stg}	$-50 \sim +125$	$^\circ C$
Storage temperature	T_{opr}	$-30 \sim +85$	$^\circ C$

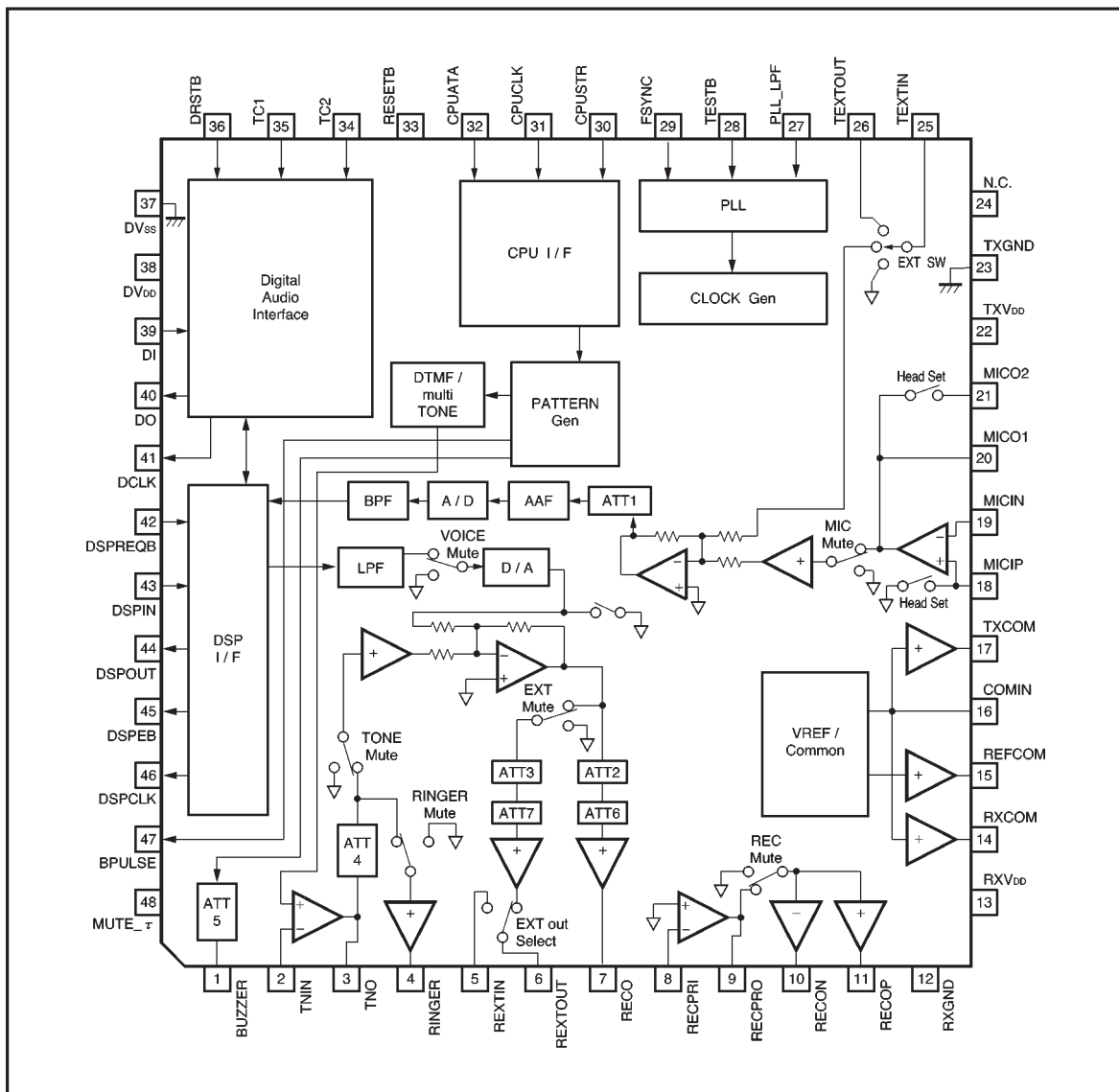
*1 Reduced by 4.0mW for each increase in T_a of $1^\circ C$ over $25^\circ C$.

● Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital power supply voltage	DV _{DD}	2.7	—	3.3	V
Analog power supply voltage	RXV _{DD}	2.7	—	3.3	V
	TXV _{DD}	2.7	—	3.3	V
PLL sync signal frequency	FSY	—	8	—	kHz

○ Not designed for radiation resistance.

● Block diagram



● Pin descriptions

Pin No.	Pin name	I / O	Function
1	BUZZER	O	Rectangular wave output for each tone pattern
2	TNIN	I	Tone output gain control amplifier inverse input
3	TNO	O	Tone output gain control amplifier output
4	RINGER	O	Tone waveform output
5	REXTIN	I	Reception external signal input
6	REXTOUT	O	Reception external signal output
7	RECO	O	Reception signal output
8	RECPRI	I	Receiver gain control amplifier inverse input
9	RECPRO	O	Receiver gain control amplifier output
10	RECON	O	Receiver amplifier inverse output
11	RECOP	O	Receiver amplifier non-inverse output
12	RXGND	—	Analog ground for reception
13	RXVDD	—	Analog power supply for reception
14	RXCOM	O	Analog reference voltage output for reception
15	REFCOM	O	Reference voltage output for internal reference
16	COMIN	O	Analog reference voltage output
17	TXCOM	O	Analog reference voltage output for transmission
18	MICIP	I	Mic amplifier non-inverse input
19	MICIN	I	Mic amplifier inverse input
20	MICO1	O	Mic amplifier output 1
21	MICO2	O	Mic amplifier output 2
22	TXVDD	—	Analog power supply for transmission
23	TXGND	—	Analog ground for transmission
24	N.C.	—	—
25	TEXTIN	I	Transmission external input
26	TEXTOUT	O	Transmission external output
27	PLLFP	I / O	Input / output connection for PLL filter
28	TESTB	I	Test input (→DVDD)
29	FSYNC	I	PLL reference 8kHz clock input
30	CPUSTR	I	CPU I / F strobe input
31	CPUCLK	I	CPU I / F shift clock input
32	CPUDATA	I	CPU I / F address data input
33	RESETB	I	System reset input (L: reset)
34	TC2	I	DAI test input
35	TC1	I	DAI test input
36	DRSTB	I	DAI reset input
37	DVSS	—	Digital ground
38	DVDD	—	Digital power supply
39	DI	I	Digital serial data input

Pin No.	Pin name	I / O	Function
40	DO	O	DAI serial data output
41	DCLK	O	DAI shift clock output
42	DSPREQB	I	DSP serial data request input
43	DSPIN	I	DSP serial data input
44	DSPOUT	O	DSP serial data output
45	DSPEB	O	DSP serial data enable output
46	DSPCLK	O	DSP serial data clock output
47	BPULSE	O	Tone pattern intermittent output
48	MUTE_τ	I	Connector for capacitor for soft mute setting

- Electrical characteristics (unless otherwise noted, Ta = 25°C, DV_{DD} = RXV_{DD} = TXV_{DD} = 3.0V, FSYNC = 8kHz, gain of each attenuator = 0dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
〈DC characteristics〉							
Current consumption*1	I _{DD}	—	8.2	—	mA	All power on	FSYNC=8kHz
	I _{DD1}	—	0.1	20	μA	Complete power down	FSYNC pin fixed
Digital input high level voltage	I _{DD2}	0.8DV _{DD}	—	—	V	—	
Digital input low level voltage	I _{DD3}	—	—	0.2DV _{DD}	V	—	
Digital input high level current	I _{IH}	—	—	10	μA	V _{IH} =DV _{DD}	
Digital input low level current	I _{IL}	—10	—	—	μA	V _{IL} =0V	
Digital output high level voltage	V _{OH}	DV _{DD} —0.5	—	—	V	I _{OH} =—1mA	
Digital output low level voltage	V _{OL}	—	—	0.5	V	I _{OL} =1mA	

*1 The power supply voltage (DV_{DD}, RXV_{DD}, and TXV_{DD}) is 3V. There is no load on the digital and analog output pins.
 Digital input pins other than the FSYNC pin are connected to DV_{DD} or DV_{SS}.
 Analog input pins are connected to TXCOM or RXCOM with the proper resistance.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions		
〈Transmission characteristics〉								
Signal to total power distortion ratio (A→D) TEXTIN→DSPOUT	S _{DT}	24	—	—	dB	1020Hz reference	—45dBm0	C-Wgt
		29	—	—			—40dBm0	
		35	—	—			0, —30dBm0	
Signal to total power distortion ratio (D→A) DSPIN→RECO	S _{DR}	24	—	—	dB	1020Hz reference	—45dBm0	C-Wgt
		29	—	—			—40dBm0	
		35	—	—			0, —30dBm0	
Transmission level characteristics (A→D) TEXTIN→DSPOUT	G _{TX}	—0.9	—	0.9	dB	1020Hz reference	—55dBm0	Reference level =—10dBm0
		—0.6	—	0.6			—50dBm0	
		—0.3	—	0.3			0, —40dBm0	
Transmission level characteristics (D→A) DSPIN→RECO	G _{TR}	—0.9	—	0.9	dB	1020Hz reference	—55dBm0	Reference level =—10dBm0
		—0.6	—	0.6			—50dBm0	
		—0.3	—	0.3			0, —40dBm0	
Transmission output level	V _{OTX}	—	0.395	—	V _{rms}	1020Hz, 0dBm0 input reference	MICO1 →DSPOUT	Set the MIC1 level to 0dB
		—	0.125	—	V _{rms}		TEXTIN →DSPOUT	Set the TESTIN level to 0dB
Reception output level	V _{ORX}	—	0.346	—	V _{rms}	1020Hz, 0dBm0 input reference	DSPIN →REXTOUT	—
		—	0.346	—	V _{rms}		DSPIN →RECOP RECOM	When RECO→ RECPRO—6dB
Transmission loss frequency characteristics (A→D) TEXTIN→DSPOUT	G _{RX}	24	—	—	dB	1020Hz, 0dBm0 input reference	0.06kHz	—
		0	—	2.5			0.2kHz	
		—0.3	—	0.3			0.3~3.0kHz	
		—0.3	—	0.9			3.4kHz	
		0	—	—			3.6kHz	
		6.5	—	—			3.78kHz	
Transmission loss frequency characteristics (D→A) DSPIN→RECO	G _{RR}	—0.3	—	0.3	dB	1020Hz, 0dBm0 input reference	0.0~3.0kHz	—
		—0.3	—	0.9			3.4kHz	
		0	—	—			3.6kHz	
		6.5	—	—			3.78kHz	

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions		
〈Tone generator〉									
Tone output level	HTONE	V _{TNH}	−10.4	−8.9	−7.4	dBm	Set at 2kHz	→RINGER	C-Wgt 0dBm=0.775V _{rms}
			−10.9	−8.9	−6.9	dBm		→REXTOUT	
	HTONE ATONE	V _{TNL}	−12.6	−11.1	−9.6	dBm		→RINGER	
Tone loss		G _{LOSS}	15	18	21	dB	HTONE set at 2kHz	→RINGER	TGLOS=1
Tone distortion		S _{DTN}	—	—	−29	dB	HTONE set at 2kHz	→RINGER	C-Wgt
〈Attenuator〉									
Gain error	ATT1	ΔATT1	—	—	±0.6	dB	1020Hz input	→DSPOUT	—
	ATT2	ΔATT2	—	—	±2	dB		→RECO	
	ATT3	ΔATT3	—	—				→REXTOUT	
	ATT4	ΔATT4	—	—	±0.8	dB	Set at 2kHz	→RINGER	—
	ATT5	ΔATT5	—	—	±0.1	V	—	→BUZZER	—
	ATT6	ΔATT6	—	—	±0.8	dB	1020Hz input	→RECO	—
	ATT7	ΔATT7	—	—				→REXTOUT	
〈PLL block〉									
PLL lead-in time		T _{PL}	—	5	100	msec	—		

● Digital AC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
〈Serial data interface / timing〉					
DSPCLK frequency	f _{SCK}	—	256	—	kHz
DSPREQB input setup time	t _{SUR}	3.0	—	—	μs
DSPREQB input hold time	t _{HTR}	3.0	—	—	μs
DSPIN input setup time	t _{SUS}	100	—	—	ns
DSPIN input hold time	t _{HTS}	100	—	—	ns
DSPEB low pulse width	t _{WEN}	5.0	—	—	μs
DSPREQB scan internal clock frequency	t _{REX}	—	8	—	kHz
〈Register write timing〉					
CPUCLK frequency	f _{CLK}	—	—	3	MHz
CPUDATA input setup time	t _{SUDA}	100	—	—	ns
CPUDATA input hold time	t _{HTDA}	100	—	—	ns
Input setup time (CPUCLK high vs. CPUSTR high)	t _{SUD}	333	—	—	ns
Input hold time (CPUCLK high vs. CPUSTR low)	t _{HTD}	1000	—	—	ns
CPUSTR strobe pulse width	f _{PWD}	667	—	—	ns
〈DAI timing〉					
DCLK frequency	f _{DCLK}	—	104	—	kHz
DCLK low pulse width	t _{WDCL}	3.8	4.8	5.8	μs
DCLK high pulse width	t _{WDCH}	3.8	4.8	5.8	μs
DRSTB low pulse width	t _{WDR}	4	—	—	ms
DI input setup time	t _{SUDI}	100	—	—	ns
DI input hold time	t _{HIDI}	100	—	—	ns

●Measurement circuit

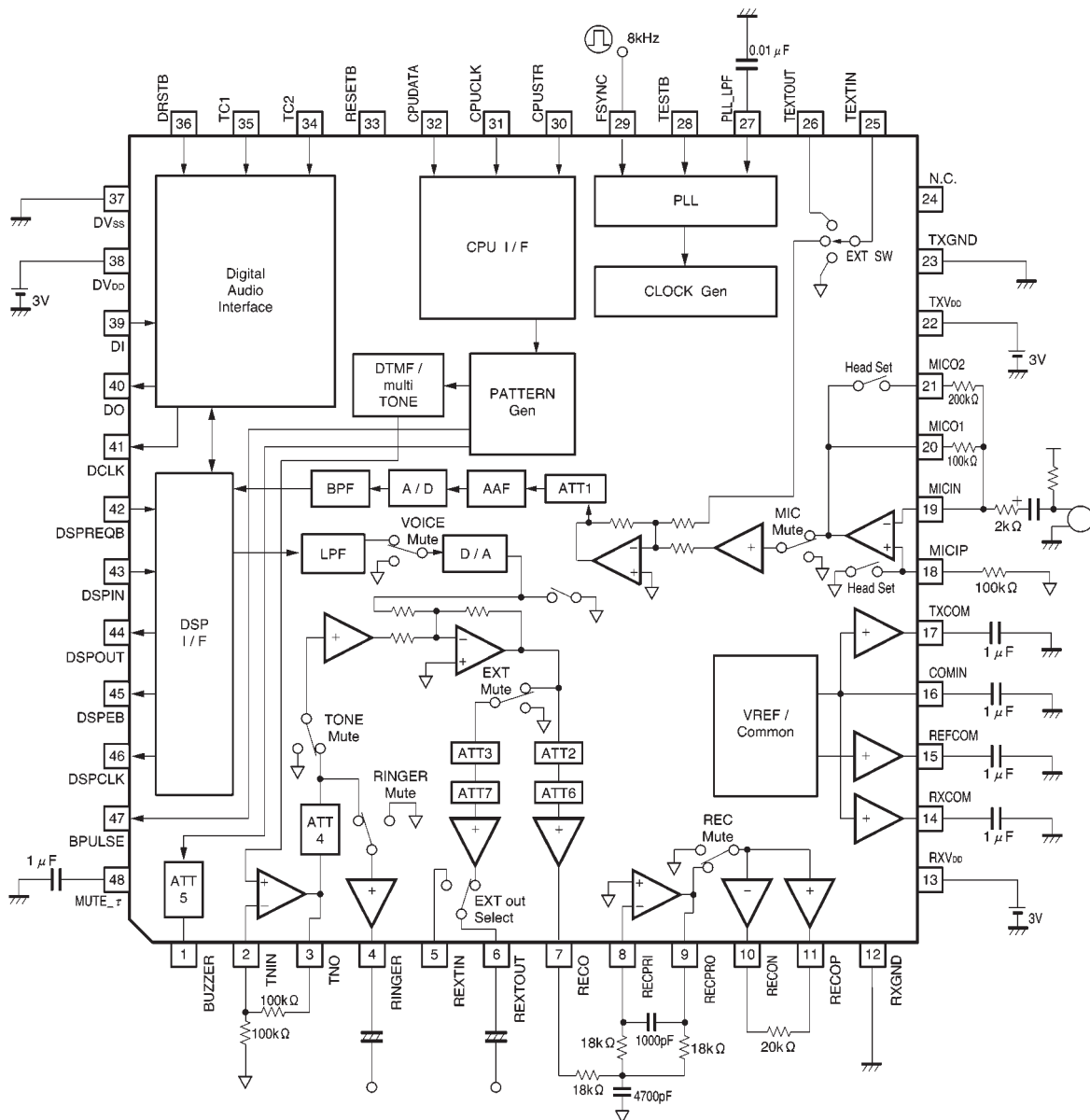


Fig.1

● Application example

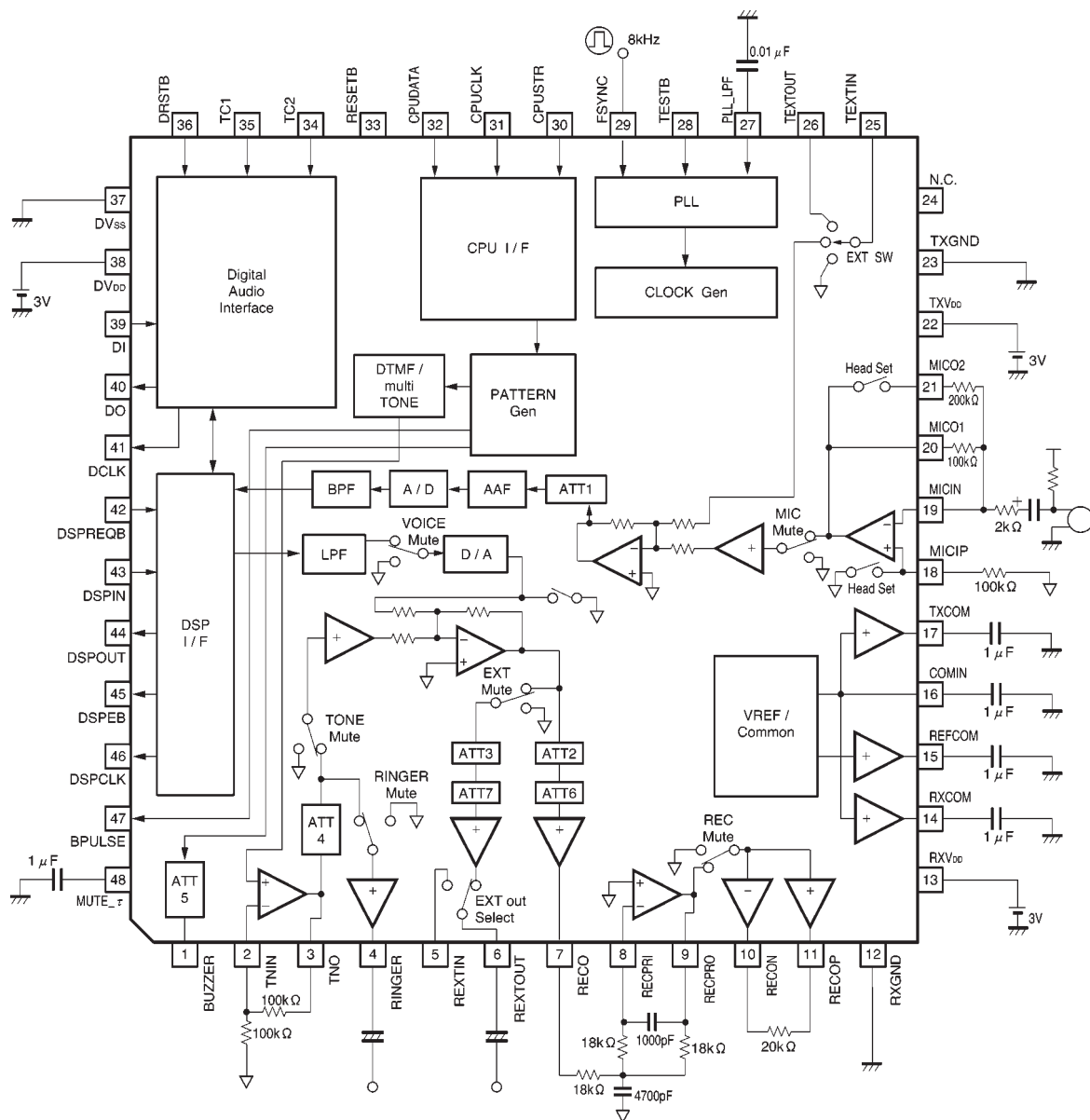
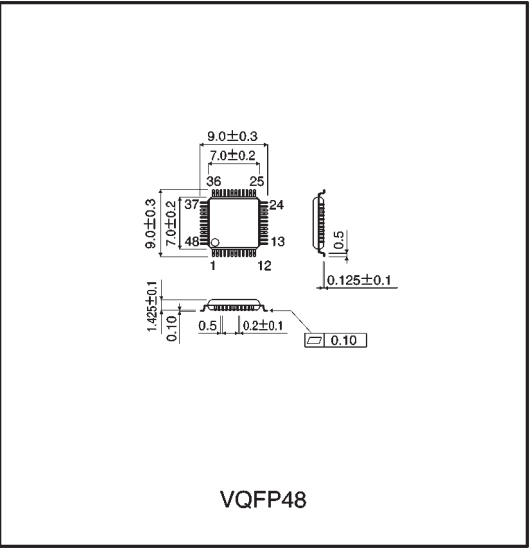


Fig.2

●External dimensions (Units: mm)



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