TECHNICAL NOTE





Voltage Detector IC Series

Low Voltage Free Delay Time Setting CMOS Voltage Detector IC Series BU42 G/F/FVE, BU43 G/F/FVE Series





General Description

ROHM CMOS reset IC series with adjustable output delay is a high-accuracy low current consumption reset IC series with a built-in delay circuit. The lineup was established with two output types (Nch open drain and CMOS output) and detection voltages range from 0.9V to 4.8V in increments of 0.1V, so that the series may be selected according to the application at hand.

Features

- 1) Detection voltage from 0.9V to 4.8V in 0.1V increments
- 2) Highly accurate detection voltage: ±1.0%
- 3) Ultra-low current consumption
- 4) Nch open drain output (BU42□□G/F/FVE)and CMOS output (BU43□□G/F/FVE)

5) Small surface package : SSOP5(BU42 \square G, BU43 \square G)

: SOP4(BU42□□F, BU43□□F)

: VSOF5(BU42□□FVE, BU43□□FVE)

Applications

All electronics devices that use microcontrollers and logic circuits.

Selection Guide



Number	Specification	Details		
1	Output Circuit Type	2 : Open drain output 3 : CMOS output		
2	Detection voltage	Example) VDET: Represented as 0.1V steps in the range from 0.9V to 4.8V (Displayed as 0.9 in the case of 0.9V)		
3	Package	G : SSOP5 (SMP5C2) F : SOP4 FVE : VSOF5 (EMP5)		

●Lineup

Making	Detection voltage	Part Number									
ZR	4.8V	BU4248	ΥV	2.8V	BU4228	1H	4.8V	BU4348	OM	2.8V	BU4328
ZQ	4.7V	BU4247	YU	2.7V	BU4227	1G	4.7V	BU4347	0L	2.7V	BU4327
ZP	4.6V	BU4246	YT	2.6V	BU4226	1F	4.6V	BU4346	0K	2.6V	BU4326
ZN	4.5V	BU4245	YS	2.5V	BU4225	1E	4.5V	BU4345	0J	2.5V	BU4325
ZM	4.4V	BU4244	YR	2.4V	BU4224	1D	4.4V	BU4344	0H	2.4V	BU4324
ZL	4.3V	BU4243	YQ	2.3V	BU4223	1C	4.3V	BU4343	0G	2.3V	BU4323
ZK	4.2V	BU4242	YP	2.2V	BU4222	1B	4.2V	BU4342	0F	2.2V	BU4322
ZJ	4.1V	BU4241	YN	2.1V	BU4221	1A	4.1V	BU4341	0E	2.1V	BU4321
ZH	4.0V	BU4240	YM	2.0V	BU4220	0Z	4.0V	BU4340	0D	2.0V	BU4320
ZG	3.9V	BU4239	YL	1.9V	BU4219	0Y	3.9V	BU4339	0C	1.9V	BU4319
ZF	3.8V	BU4238	YK	1.8V	BU4218	0X	3.8V	BU4338	0B	1.8V	BU4318
ZE	3.7V	BU4237	YJ	1.7V	BU4217	0W	3.7V	BU4337	0A	1.7V	BU4317
ZD	3.6V	BU4236	ΥH	1.6V	BU4216	0V	3.6V	BU4336	ZZ	1.6V	BU4316
ZC	3.5V	BU4235	YG	1.5V	BU4215	0U	3.5V	BU4335	ZY	1.5V	BU4315
ZB	3.4V	BU4234	YF	1.4V	BU4214	0T	3.4V	BU4334	ZX	1.4V	BU4314
ZA	3.3V	BU4233	YE	1.3V	BU4213	0S	3.3V	BU4333	ZW	1.3V	BU4313
YZ	3.2V	BU4232	YD	1.2V	BU4212	0R	3.2V	BU4332	ZV	1.2V	BU4312
YY	3.1V	BU4231	YC	1.1V	BU4211	0Q	3.1V	BU4331	ZU	1.1V	BU4311
YX	3.0V	BU4230	YB	1.0V	BU4210	0P	3.0V	BU4330	ZT	1.0V	BU4310
YW	2.9V	BU4229	YA	0.9V	BU4209	0N	2.9V	BU4329	ZS	0.9V	BU4309

2007 Oct.

●ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

Parameter		Symbol	Limits	Unit	
Power Supply Voltage		VDD-GND	-0.3 to +7	V	
Output Voltage	Nch Open Drain Output	Vout	GND-0.3 to +7	V	
	CMOS Output	V001	GND-0.3 to VDD+0.3		
Power Dissipation	SSOP5 *1		540		
	SOP4 *2 *4	Pd	400	mW	
	VSOF5 *3		210		
Operating Temperature		Topr	-40 to +125	°C	
Ambient Stora	ge Temperature	Tstg	-55 to +125	°C	

- *1 When used at temperatures higher than Ta=25°C,the power is reduced by 5.4mW per 1°C above 25°C
- *2 When used at temperatures higher than Ta=25°C, the power is reduced by 4.0mW per 1°C above 25°C
- *3 When used at temperatures higher than Ta=25°C,the power is reduced by 2.1mW per 1°C above 25°C
- *4 When a ROHM standard circuit board (70mm×70mm×1.6mm, glass epoxy board) is mounted.

●ELECTRICAL CHARACTERISTICS (Unless specified otherwise, Ta=-25°C to +125°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Detection Voltage	VDET	VDET(T) × 0.99	VDET (T)	VDET(T) × 1.01	V	VDD=H→L,RL=470kΩ *1
Detection Voltage Temperature Coefficient	VDET/ΔT	-	±30	-	ppm/ °C	Ta=-40°C to +125°C (Designed Guarantee)
Hysteresis Voltage	ΔVDET	VDET × 0.03	VDET×0.05	VDET×0.07	V	VDET≥1.1V,RL=470kΩ,VDD=L→H→L
Circuit Current when ON	IDD1	-	0.40	1.75	μА	VDD=VDET-0.2V,VDET=4.3 to 4.8V
Circuit Current when OFF	IDD2	-	0.55	2.28	μА	VDD=VDET+2.0V,VDET=4.3 to 4.8V
Operating Voltage Range	VOPL	0.7	-	-	V	VOL≤0.4V,RL=470kΩ,Ta=25 to 125°C
"L" Output Current (Nch)	IOL	3.6	6.5	-	mA	VDS=0.5V,VDD=2.4V,VDET=2.7 to 4.8V
"H" Output Current (Pch)	IOH	2.0	4.0	-	mA	VDS=0.5V,VDD=6.0V,VDET=4.0 to 4.8V
CT pin Threshold Voltage	VCTH	VDD × 0.40	VDD × 0.50	VDD × 0.60	V	VDD=VDET×1.1,RL=470kΩ,VDET=2.6 to 4.8V *1
Output Delay Resistance	RCT	9	10	11	MΩ	VDD=VDET × 1.1,VCT=0.5V (Designed Guarantee)*1
CT pin Output Current	ICT	200	400	-	μА	VCT=0.5V,VDD=1.5V,VDET=1.7 to 4.8V

^{*1} Guarantee on Ta=25°C

Note) RL is unnecessary for CMOS output.

Note) Regarding the operating limit voltage

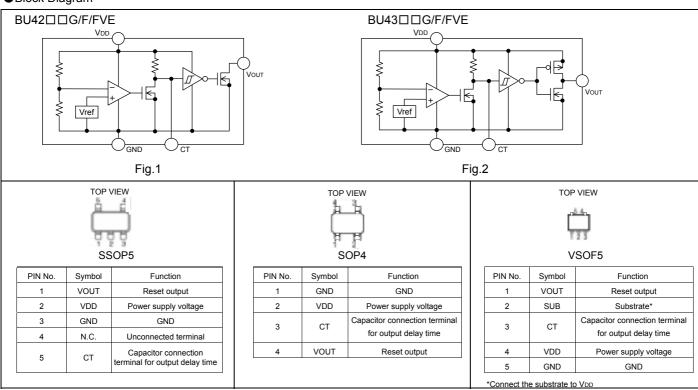
The VouT output is unsettled when VDD is less than this voltage. It will be Open, High or Low.

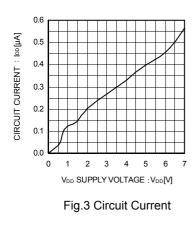
Note) Hysteresis Voltage = (Reset Release Voltage) – (Reset Detection Voltage) [V]

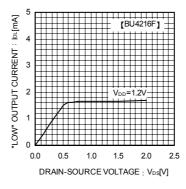
VDET (T): Set Value of Detection voltage (0.9V to 4.8V, 0.1Vstep)

Designed Guarantee. (Outgoing inspection is not done an all products.)

Block Diagram







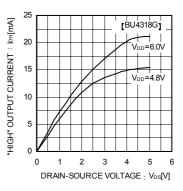
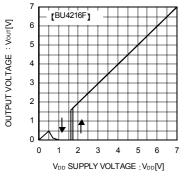
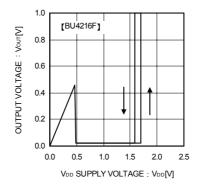


Fig.4 "LOW" Output Current

Fig.5 "High" Output Current





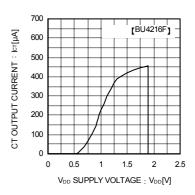
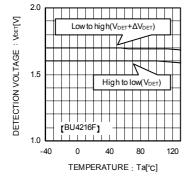
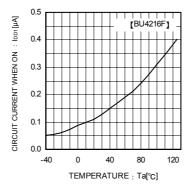


Fig.6 I/O Characteristics

Fig.7 Operating Limit Voltage

Fig.8 Ct Terminal Current





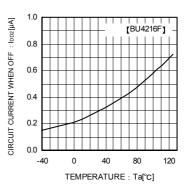
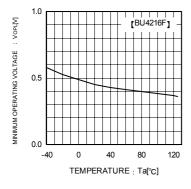
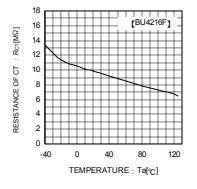


Fig.9 Detecting Voltage Release Voltage

Fig.10 Circuit Current when ON

Fig.11 Circuit Current when OFF





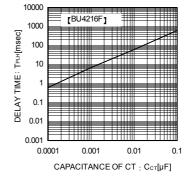


Fig.12 Operating Limit Voltage

Fig.13 Ct Terminal Circuit Resistance

Fig.14 Delay Time (TPLH) and CT Terminal External Capacitance

Setting of Detector Delay Time

This detector IC can be set delay time at the rise of VDD by the capacitor connected to CT terminal.

• Delay time at the rise of VDD TPLH:Time until when Vout rise to 1/2 of VDD after VDD rise up and beyond the release voltage (VDET+ΔVDET)

TPLH=-CCT
$$\times$$
 RCT \times In $\left(\begin{array}{c} VDD-VCTH \\ \hline VDD \end{array}\right)$

CCT: CT pin Externally Attached Capacitance

RCT : CT pin Internal Impedance VCTH : CT pin Threshold Voltage

Ln: Natural Logarithm

Reference Data

Examples of Output Failing Value (TPHL)

Part Number	TPHL [μs]				
BU4245G	275.7				
BU4345G	359.3				

^{*}This data is for reference only.

This figure will vary with the application, so please confirm actual operation conditions before use.

Explanation of Operation

For both the open drain type (Fig.15) and the CMOS output type (Fig.16), the detection and release voltages are used as threshold voltages. When the voltage applied to the Vdd pins reaches the applicable threshold voltage, the Vout terminal voltage switches from either "High" to "Low" or from "Low" to "High". BU42 \square G/F/FVE and BU43 \square G/F/FVE have delay time function which set TPLH (Output "Low" \rightarrow "High") using an external capacitor (Cct). Because the BU42 \square G/F/FVE series uses an open drain output type, it is possible to connect a pull-up resistor to VDD or another power supply [The output "High" voltage (Vout) in this case becomes VDD or the voltage of the other power supply].

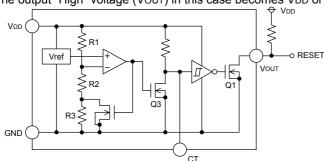


Fig.15 (BU42□□type internal block diagram)

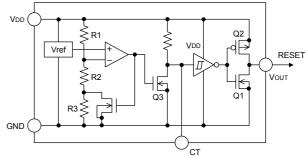


Fig.16 (BU43 ☐ type internal block diagram)

Timing Waveforms

Example: The following shows the relationship between the input voltage VDD, the CT Terminal Voltage VCT and the output voltage VOUT when the input power supply voltage VDD is made to sweep up and sweep down (The circuits are those in Figures 15 and 16).

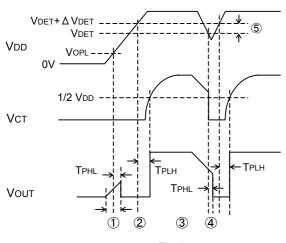


Fig.17

- ① When the power supply is turned on, the output is unsettled from after over the operating limit voltage (VOPL) until TPHL. There fore it is possible that the reset signal is not outputted when the rise time of VDD is faster than TPHL.
- ② When VDD is greater than VOPL but less than the reset release voltage (VDET + VDET), the CT terminal (VCT) and output (VOUT) voltages will switch to L.
- ③ If VDD exceeds the reset release voltage (VDET + VDET), then VOUT switches from L to H (with a delay of TPLH for setting the CT terminal).
- 4 If VDD drops below the detection voltage (VDET) when the power supply is powered down or when there is a power supply fluctuation, VOUT switches to L (with a delay of TPHL).
- The potential difference between the detection voltage and the release voltage is known as the hysteresis width (VDET). The system is designed such that the output does not flip-flop with power supply fluctuations within this hysteresis width, preventing malfunctions due to noise.

Circuit Applications

1) Examples of a common power supply detection reset circuit

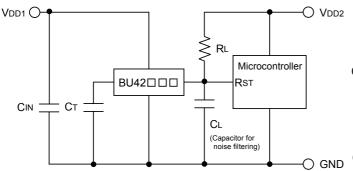
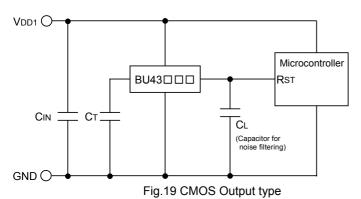


Fig.18 Open collector Output type



Application examples of BU42 \(\subseteq \text{G/F/FVE} \) series (Open Drain output type) and BU43 \(\subseteq \text{G/F/FVE} \) series (CMOS output type) are shown below.

CASE1:The power supply of the microcontroller (Vdd2) differs from the power supply of the reset detection (Vdd1).

Use the Open Drain Output Type (BU42□□G/FVE) attached a load resistance (RL) between the output and Vdd2. (As shown Figure 18)

CASE2:The power supply of the microcontroller (Vdd1) is same as the power supply of the reset detection (Vdd1).

Use CMOS output type (BU43 G/FVE) or Open Drain Output Type (BU42 G/FVE) attached a load resistance (RL) between the output and Vdd1.

(As shown Figure 19)

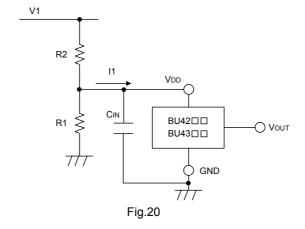
When a capacitance CL for noise filtering is connected to the Vout pin (the reset signal input terminal of the microcontroller), please take into account the waveform of the rise and fall of the output voltage (Vout).

2) Examples of the power supply with resistor dividers

In applications where the power supply input terminal (VDD) of an IC with resistor dividers, it is possible that a through-current will momentarily flow into the circuit when the output logic switches, resulting in malfunctions (such as output oscillatory state).

(Through-current is a current that momentarily flows from the power supply (VDD) to ground (GND) when the output level switches from "High" to "Low" or vice versa.)

Consider the use of BD52□□when the power supply input it with resistor dividers.



Operation Notes

1 . Absolute maximum range

Absolute Maximum Ratings are those values beyond which the life of a device may be destroyed. We cannot be defined the failure mode, such as short mode or open mode. Therefore a physical security countermeasure, like fuse, is to be given when a specific mode to be beyond absolute maximum ratings is considered.

2. GND potential

GND terminal should be a lowest voltage potential every state.

Please make sure all pins that are over ground even if include transient feature.

3 . Electrical Characteristics

Be sure to check the electrical characteristics, that are one the tentative specification will be changed by temperature, supply voltage, and external circuit.

4 . Bypass Capacitor for Noise Rejection

Please put into the to reject noise between VDD pin and GND with 1uF over and between VOUT pin and GND with 1000pF. If extremely big capacitor is used, transient response might be late. Please confirm sufficiently for the point.

5 . Short Circuit between Terminal and Soldering

Don't short-circuit between Output pin and VDD pin, Output pin and GND pin, or VDD pin and GND pin. When soldering the IC on circuit board please is unusually cautious about the orientation and the position of the IC. When the orientation is mistaken the IC may be destroyed.

6 . Electromagnetic Field

Mal-function may happen when the device is used in the strong electromagnetic field.

- 7. The VDD line inpedance might cause oscillation because of the detection current.
- 8 . A VDD -GND capacitor (as close connection as possible) should be used in high VDD line impedance condition.
- 9. Lower than the mininum input voltage makes the VouT high impedance, and it must be VDD in pull up (VDD) condition.
- 10. Case of needless Delay time, recommended to insert more 470kΩ resister between VDD and CT.
- 11. Recommended value of RL Resistar is over $50k\Omega$ (VDET=1.5 to 4.8V), over $100k\Omega$ (VDET=0.9 to 1.4V).
- 12. This IC has extremely high impedance terminals. Small leak current due to the uncleanness of PCB surface might cause unexpected operations. Application values in these conditions should be selected carefully. If 10MΩ leakage is assumed between the CT terminal and the GND terminal, 1MΩ connection between the CT terminal and the VDD terminal would be recommended. Also, if the leakage is assumed between the VOUT terminal and the GND terminal, the pull up resistor should be less than 1/10 of the assumed leak resistance.

The value of RCT depends on the external resistor that is connected to CT terminal, so please consider the delay time that is decided by $\tau \times RCT \times CCT$ changes.

13. Delay time (tPLH)

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tPLH = \tau \times RCT \times CCT (sec)

\tau: time constant

RCT: 10M (typ.) (built-in resistor)

CCT: capacitor connected CT pin.
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Recommended value of CcT capacitor is over 100pF.

The reference value

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 \begin{array}{c} (\tau \times RcT) \times 10^6 \\ \\ V_{DET} = 0.9 \text{ to } 2.5V \\ Ta = 25^{\circ}C \\ Ta = -25 \text{ to } 125^{\circ}C \\ (\text{min.} = 5.1 \times 10^6 & \text{typ.} = 6.0 \times 10^6 & \text{max} = 6.9 \times 10^6) \\ V_{DET} = 2.6 \text{ to } 4.8V \\ Ta = 25^{\circ}C \\ (\text{min.} = 5.9 \times 10^6 & \text{typ.} = 6.9 \times 10^6 & \text{max} = 7.9 \times 10^6) \\ \end{array}
```

Ta = -25 to 125°C (min. =
$$3.8 \times 10^6$$
 typ.= 6.9×10^6 max = 10.0×10^6)

14. External parameters

The recommended parameter range for CT is 100pF to 0.1μ F. For RL, the recommended range is $50k\Omega$ to $1M\Omega$. There are many factors (board layout, etc) that can affect characteristics. Please verify and confirm using practical applications.

15. CT pin discharge

Due to the capabilities of the CT pin discharge transistor, the CT pin may not completely discharge when a short input pulse is applied, and in this case the delay time may not be controlled. Please verify the actual operation.

16. Power on reset operation

Please note that the power on reset output varies with the Vcc rise up time. Please verify the actual operation.

17. Precautions for board inspection

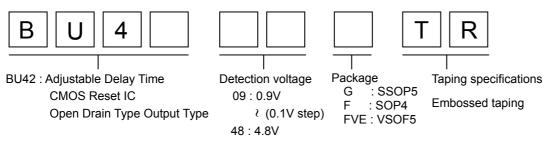
Connecting low-impedance capacitors to run inspections with the board may produce stress on the IC.

Therefore, be certain to use proper discharge procedure before each process of the test operation.

To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handing, transfer and storage operations. Before attempting to connect components to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing any component connected to the test setup.

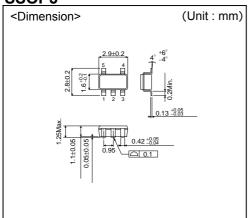
18. When the power supply, is turned on because of incertain cases, momentary Rash-current flow into the IC at the logic unsettled, the couple capacitance, GND pattern of width and leading line must be considered.

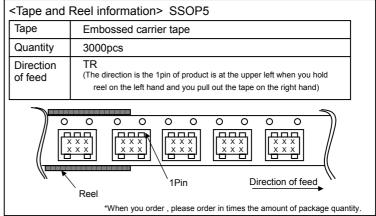
Part Number Selection



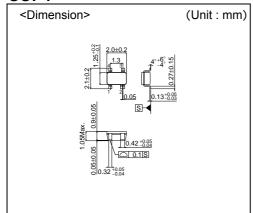
BU43 : Adjustable Delay Time CMOS Reset IC CMOS Output Type

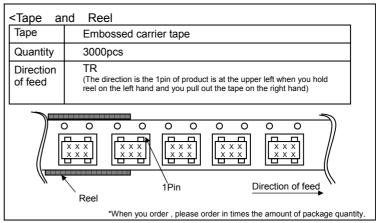
SSOP5



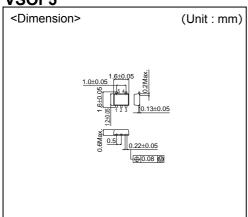


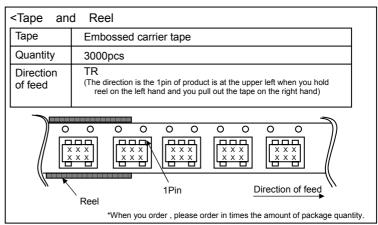
SOP4





VSOF5





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