Clock generator for digital still camera

BU2381FV

BU2381FV is a high-performance 3-channel PLL IC. PLL circuit generates necessary clocks by inputting standard clocks of crystal oscillator from outside. Changing a connection of wire can generate any clocks required for any applications of users. Jitter and S/N characteristic has achieved almost the same high-quality sound and vision as oscillating module because of optimization of PLL. Frequency can be changed by the internal dividing control.

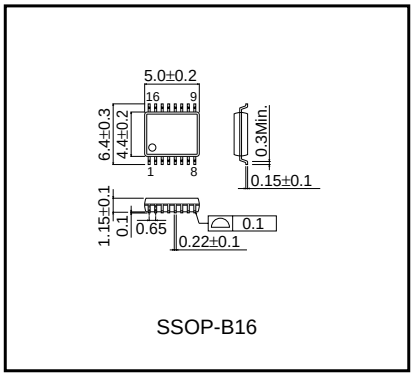
●Applications

Digital still camera

●Features

1) Generate clocks for video output, CDS, USB from standard clock input
2) No external elements required for PLL
3) Standard clocks apply to two kinds of NTSC/PAL
4) Single power supply of 3.3V operating
5) SSOP-B16 small package

●External dimensions (Unit : mm)



SSOP-B16

●Absolute maximum ratings (Ta=25°C)

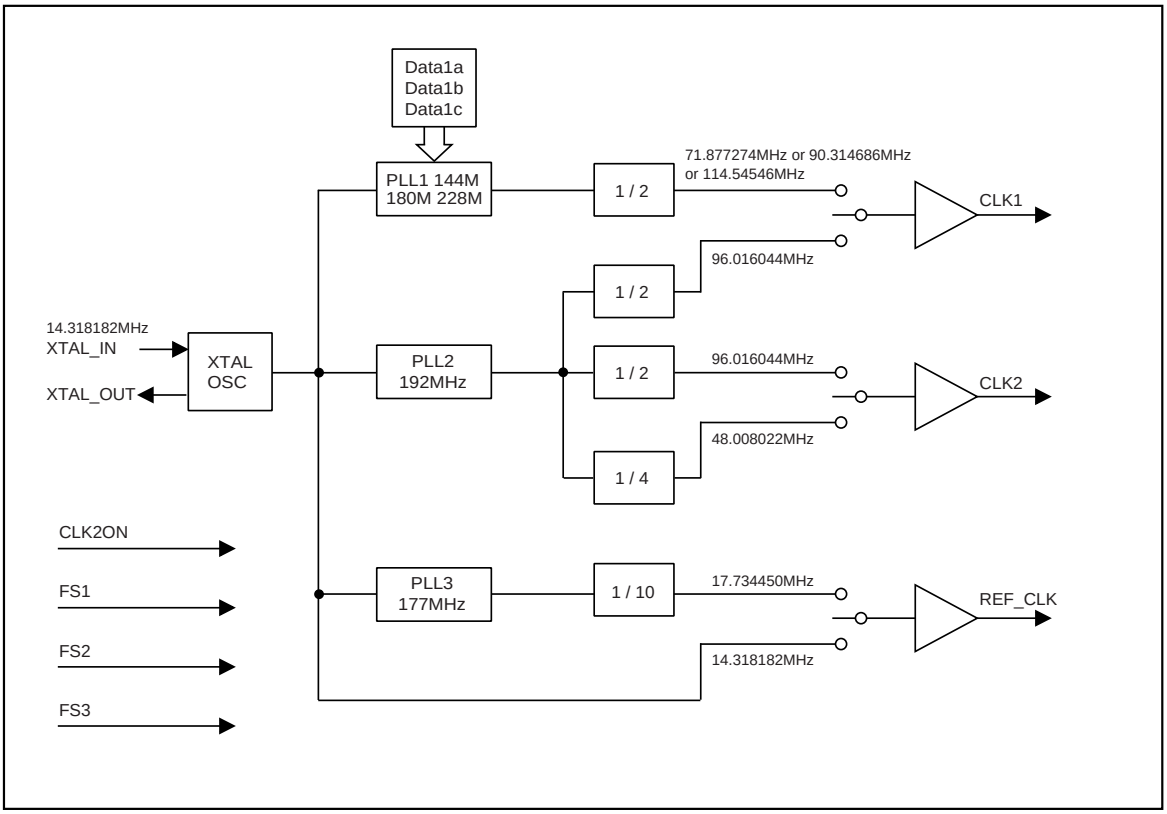
Parameter	Symbol	Limits	Unit
Applied voltage	V_{DD}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{DD}+0.5	V
Storage temperature range	Tstg	–30 to +125	°C
Power dissipation	Pd	450*	mW

*Derating : 4.5mW/°C for operating above Ta=25°C
*An operation is not guaranteed.
*Radiation resistance design is not used.
*Power dissipation is measured when BU2381FV is placed on the board.

●Recommended operating conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.0	–	3.6	V
Input "H" voltage range	V_{IH}	0.8V_{DD}	–	V_{DD}	V
Input "L" voltage range	V_{IL}	0	–	0.2V_{DD}	V
Operation temperature range	Topr	–5	–	70	°C
Output maximum load	C_L	–	–	15	pF

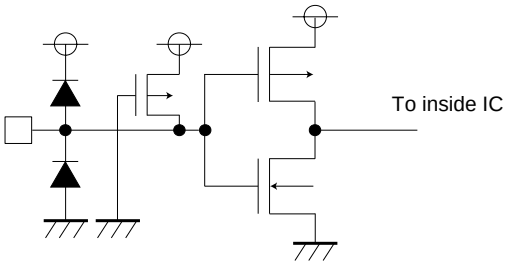
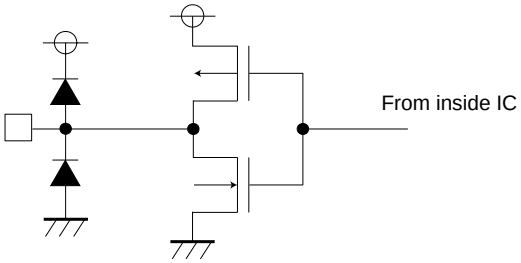
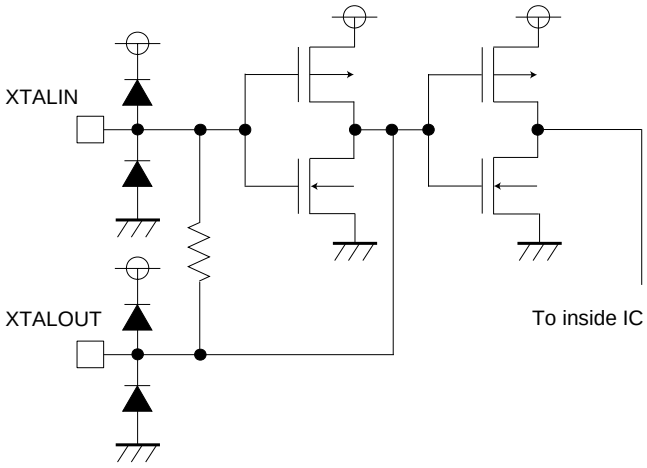
●Block diagram



●Pin descriptions

Pin No.	Pin name	Functions
1	REFCLK	14.3MHz / 17.7MHz clock output
2	V_{DD}	Analog V_{DD}
3	FS3	CLK1, 2 output select with pull up
4	V_{SS}	Analog GND
5	X_{IN}	Standard crystal input
6	TEST	Input for test mode (normally open)
7	X_{OUT}	Standard crystal output
8	FS2	CLK1, 2 output select with pull up
9	$CLK1_{OUT}$	71M / 90M / 96M / 114MHz clock output
10	FS1	REFCLK output select with pull up
11	$CLK2_{ON}$	CLK2 output control with pull up H : enable L : disable
12	V_{SS}	GND for CLK1, 2 clock output and Logic circuit
13	V_{DD}	V_{DD} for CLK1, 2 clock output and Logic circuit
14	$CLK2_{OUT}$	96M / 48M clock output
15	V_{SS}	GND for REFCLK clock output
16	V_{DD}	V_{DD} for REFCLK clock output

●**Input output circuits**

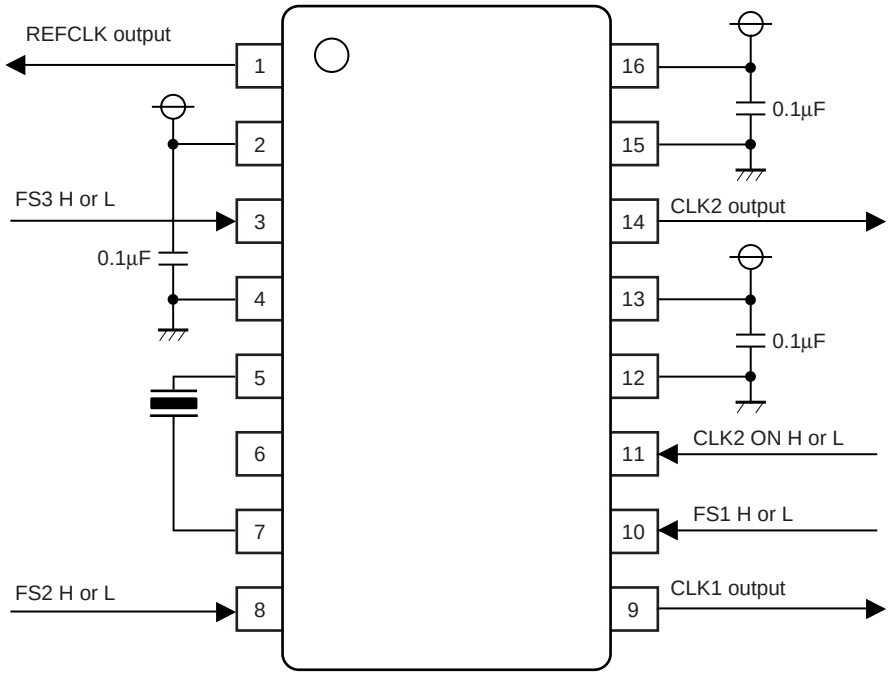
Pin No.	Equivalent circuit
Input PIN 3, 8, 10, 11 with pull–up (PIN6 : TESTpin with pull down)	
OUTPUT PIN 1, 9, 14	
Crystal PIN 5, 7	

●**Electrical characteristics** (Unless specified otherwise Ta=25°C, VCC=3.3V)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply current		IDD	–	40	50	mA	No load
Output frequency		–	–	–	–	–	
CLK1	FS2 : H FS3 : H	Fclk1-1	–	96.016044	–	–	Xtal ∗ (228 / 17) / 2
	FS2 : H FS3 : L	Fclk1-2	–	71.877274	–	–	Xtal ∗ (251 / 25) / 2
	FS2 : L FS3 : L	Fclk1-3	–	114.54546	–	MHz	Xtal ∗ (224 / 14) / 2
	FS2 : L FS3 : H	Fclk1-4	–	90.314686	–	MHz	Xtal ∗ (164 / 12) / 2
CLK2	FS2 : L FS3 : L	Fclk2-1	–	96.016044	–	MHz	Xtal ∗ (228 / 17) / 2
	FS2, 3 : HL / LH / HH	Fclk2-2	–	48.008022	–	MHz	Xtal ∗ (228 / 17) / 4
REFCLK	FS1 : H	Fref1-1	–	14.318182	–	MHz	Crystal direct output
	FS1 : L	Fref1-2	–	17.73445	–	MHz	Xtal ∗ (706 / 57) / 10
Duty1 at 100MHz		Duty1	45	50	55	%	Measured at 1/2 VDD
Duty2 at 100MHz		Duty2	–	50	–	%	Measured at 1/2 VDD
Rise time		tr	–	2.5	–	nsec	Time between 0.2 VDD and 0.8 VDD
Fall time		tf	–	2.5	–	nsec	Time between 0.8 VDD and 0.2 VDD
Period jitter 1σ		P-J1σ	–	30	–	psec	∗1
Period jitter MIN-MAX		P-JMINMAX	–	180	–	psec	∗2
Output Lock time		Tlock	–	–	1	msec	∗3

Note) When input frequency is 14.318182MHz, output frequency is above rated value.
∗1) Period Jitter 1σ : This value is the standard deviation of an output period when using Time Interval Analyzer with 10,000 sampling.
∗2) Period Jitter MIN-MAX : This value is the max range of an output period when using Time Interval Analyzer with 10,000 sampling.
∗3) Output Lock time : This value is the time until the output clock gets stable after the power supply voltage leads to 3.0V.

●**Application example**



Note) The BU2381FV is placed on the board normally.
A decoupling capacitor (0.1µF) needs to be placed between pin2 and pin4, pin13 and pin12, pin16 and pin15.
The decoupling capacitor is an close to the above pins as possible.

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